My BRAVE Journey

Thomas Lange

29/08/2017

ESA UNCLASSIFIED - For Official Use

Parts

1. Preparation of a BRAVE Development Kit Environment
2. Development of a BRAVE Demonstrator Application
3. Open ESA FPGA Benchmark Suite
4. Radiation Test of a Xilinx Kintex-7 FPGA

Git Repositories

- All projects are organized in Git repositories (TEC-EDM Git server)
- Projects are public ➥ accessible within intranet

- BRAVE Development Kit Environment:

  http://mars.ws.estec.esa.nl:8081/Lange/brave-dev-kit

- BRAVE Demonstrator Application:

  http://mars.ws.estec.esa.nl:8081/Lange/fmc-hdmi-cam

- Open ESA FPGA Benchmark Suite:

  https://gitrepos.estec.esa.int/FPGA/open-ESA-FPGA-benchmark-suite

- Radiation Test of a Xilinx Kintex-7:

  http://mars.ws.estec.esa.nl:8081/Lange/kintex-radiation-test

Preparation of a BRAVE Development Kit Environment

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BRAVE Development Kit Environment - Outline

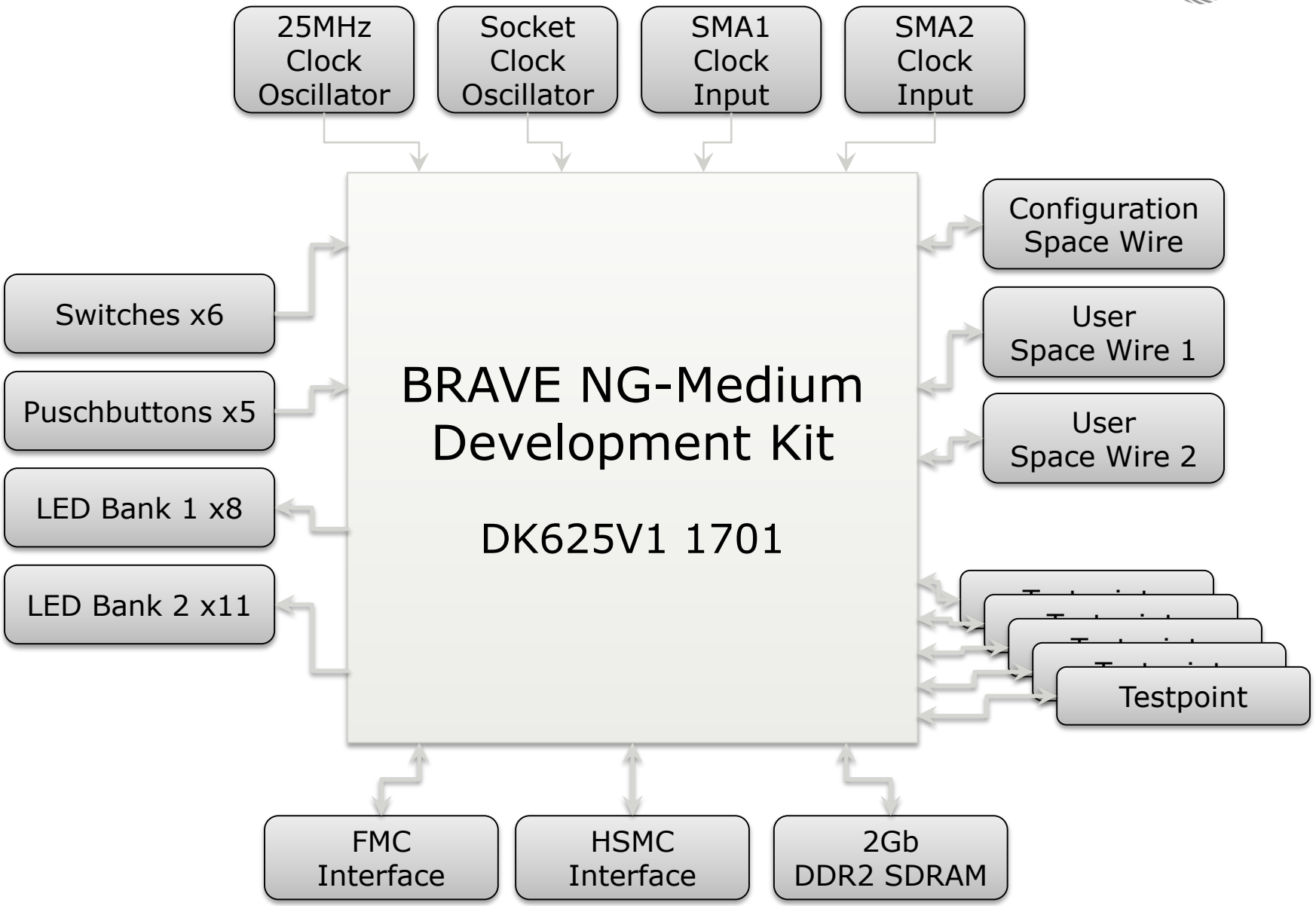
1. Motivation
2. The BRAVE Development Kit
3. Development Environment
4. Example Project/Demo

Motivation

- How to start a project with the BRAVE NG-Medium Development Kit?

➥ Creating a development environment as starting point by providing
  - Documentation
  - Automated design flow
  - Small example project

The BRAVE Development Kit



Development Environment

- The development environment includes:
  - Latest documentation by NanoXplore
  - Script to compile/synthesize a project
  - Script to program the device
  - Makefile which automates the complete process
  - VHDL top module with corresponding pads configuration
    - matches with available connectors on BRAVE Dev-Kit
  - Example project
    - Uses LEDs, switches, pushbuttons, PLL, testpoints (TP)
    - Dedicated UART receiver and transmitter

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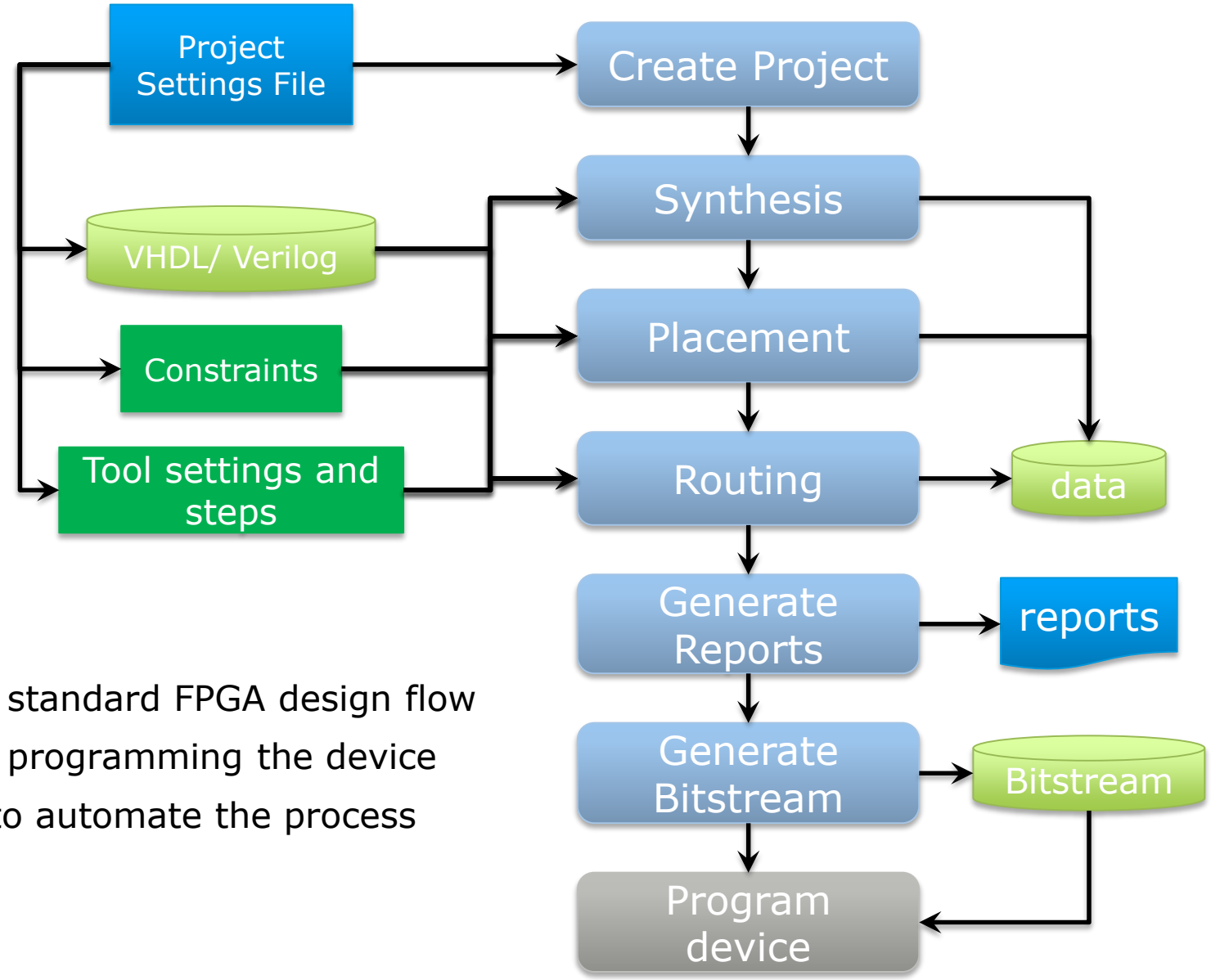
Development Environment – Flow automation



- Script for standard FPGA design flow
- Script for programming the device
- Makefile to automate the process

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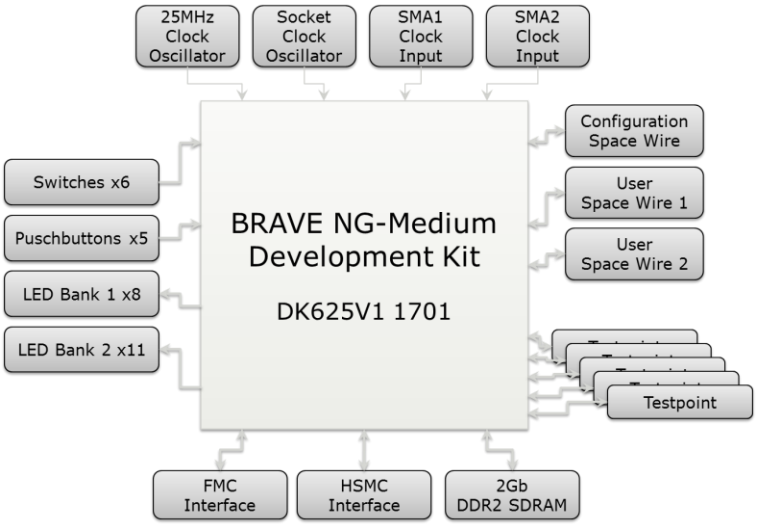
Development Environment – VHDL Top File and Pads Configuration File



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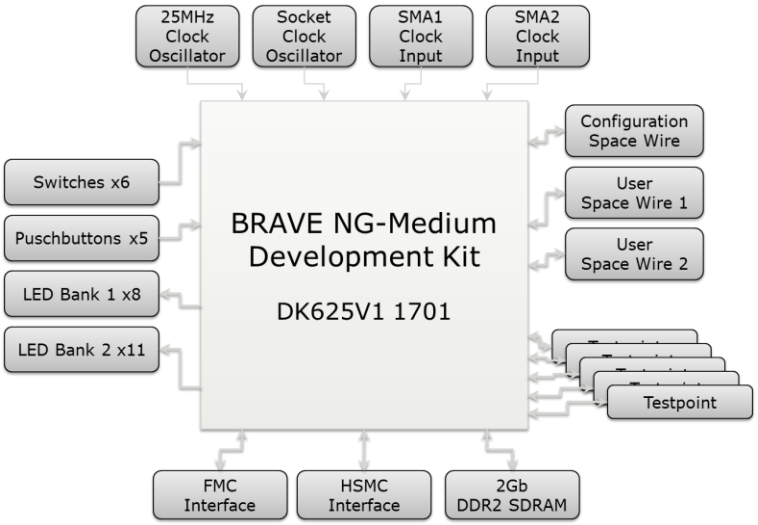

Board Top File (VHDL)

```
27 ----------------------------------------------------------------------------
28
29 entity dk625v1_top is
30
31   port (
32     -- Clock sources
33     in_osc0 : in std_logic;             -- Standard 25MHz clock oscillator
34     in_osc1 : in std_logic;             -- Socket-mounted clock oscillator
35     in_sma0 : in std_logic;             -- External J8 SMA clock input
36     in_sma1 : in std_logic;             -- External J9 SMA clock input
37
38     -- Switches
39     --      in_sw[0] : PA09 (Switch S1)
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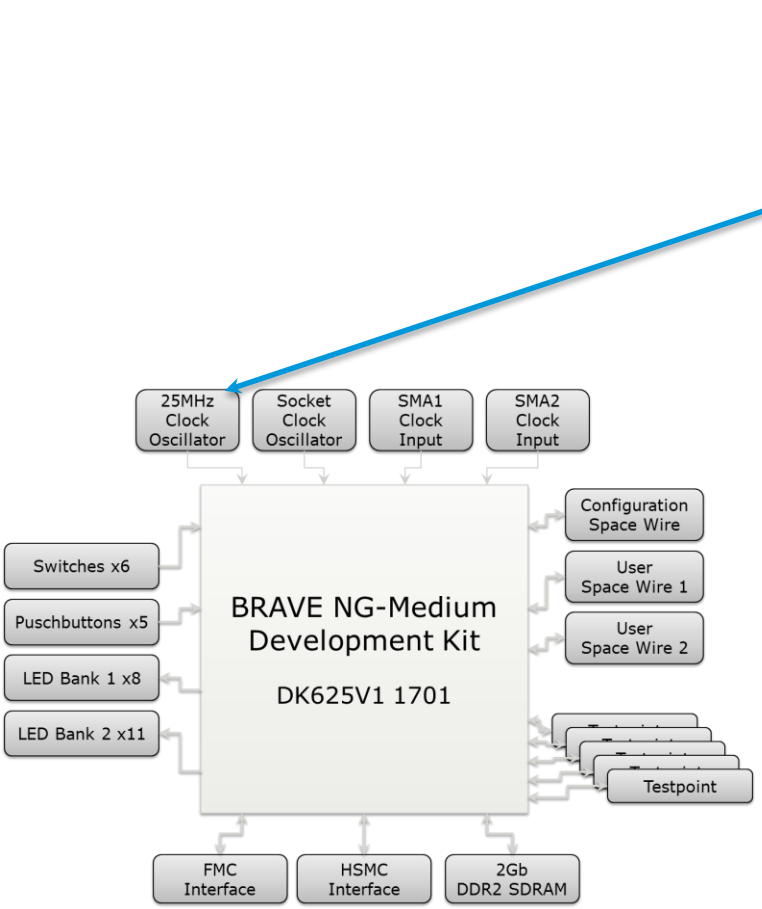

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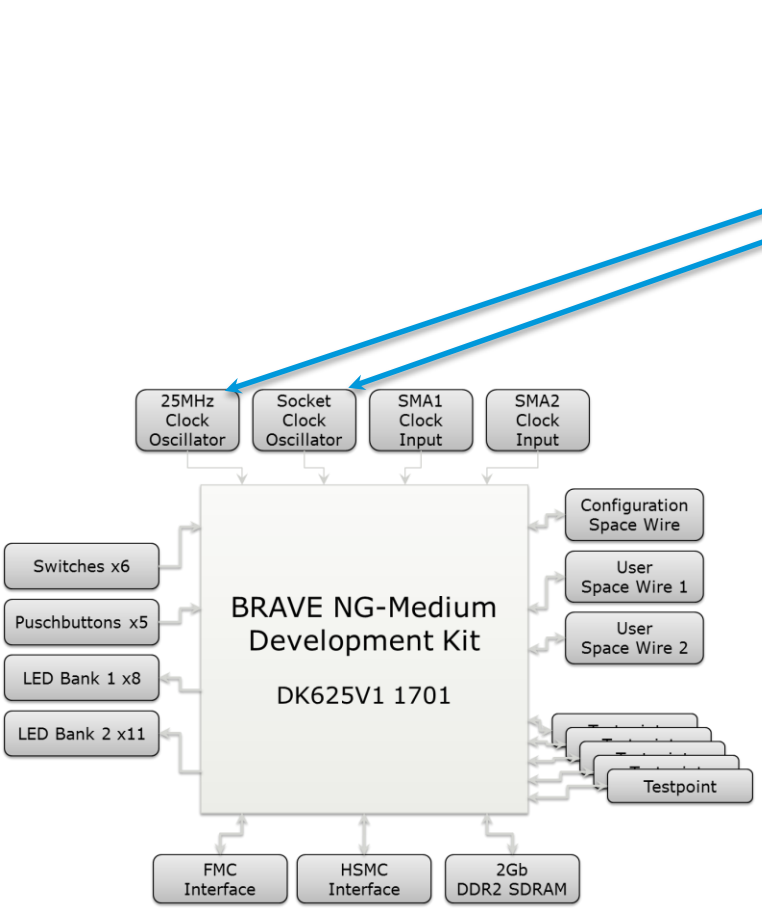

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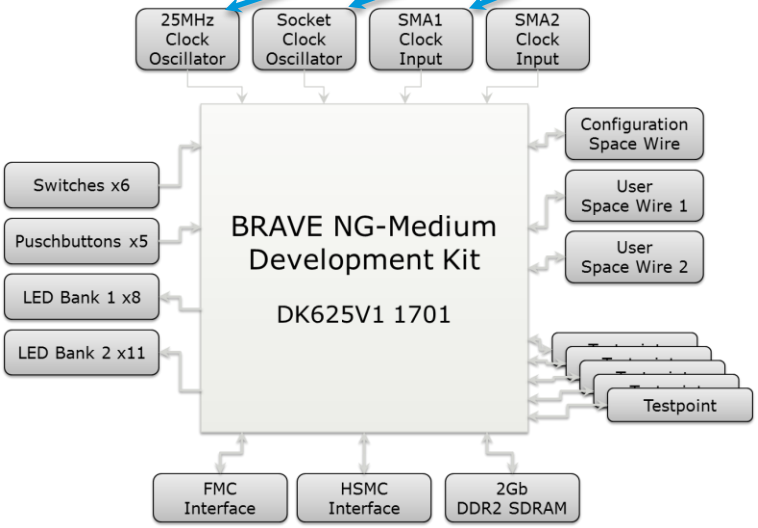


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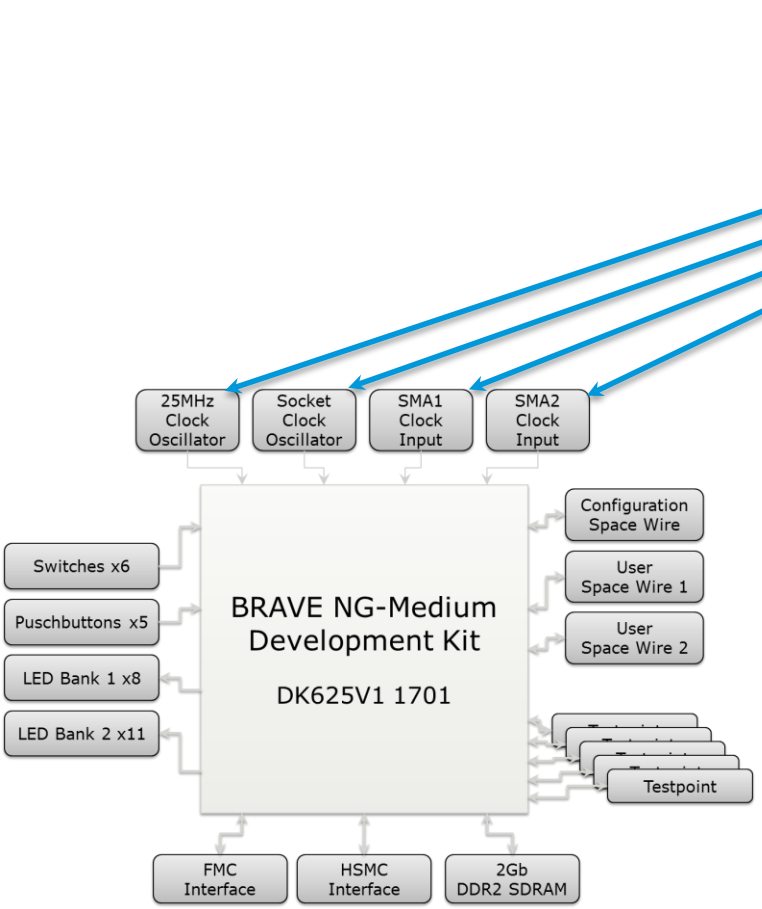


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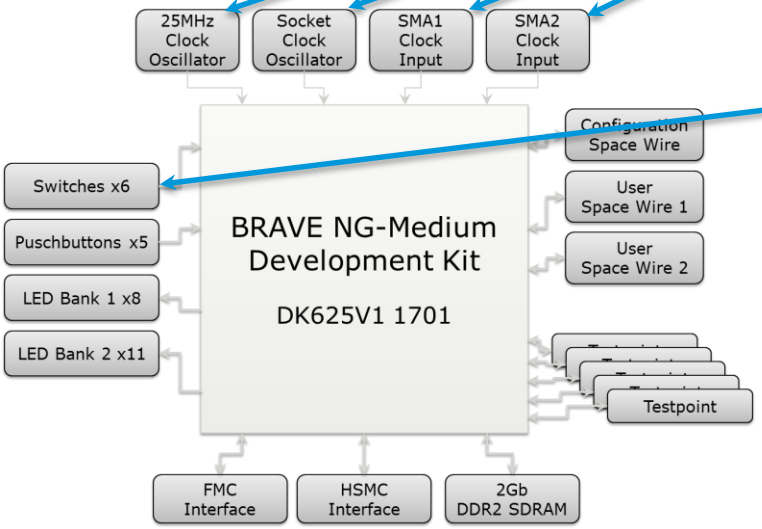

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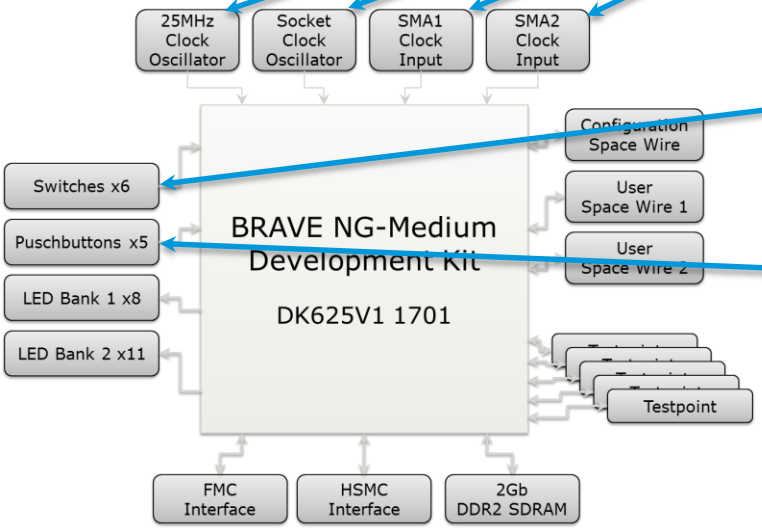

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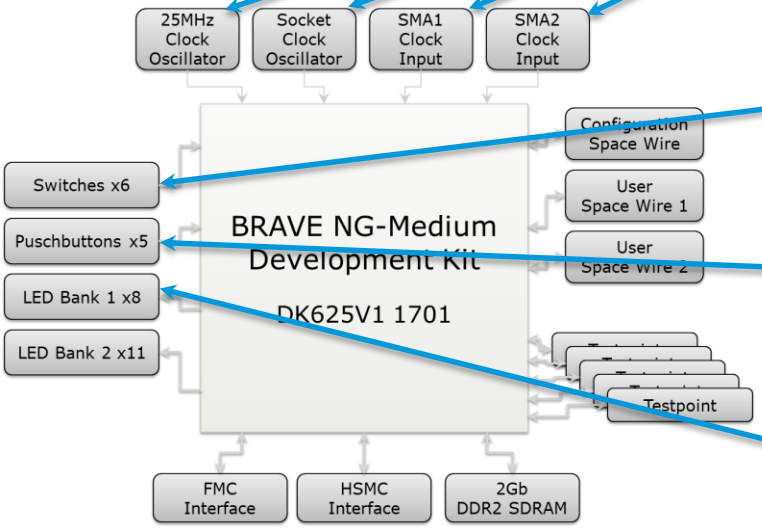

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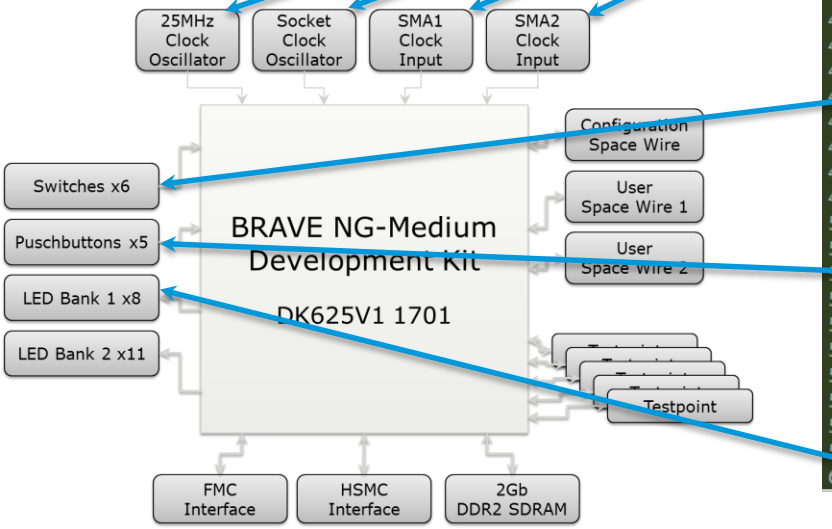


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```

Pads Configuration File (Python)

```
16 dk625v1_pads = {
17     # Clock sources
18       'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19     , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20     , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21     , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23     # # Switches and Pushbuttons
24     , 'in_sw[0]'           : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
25     , 'in_sw[1]'           : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
26     , 'in_sw[2]'           : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27     , 'in_sw[3]'           : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
28     , 'in_sw[4]'           : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
29     , 'in_sw[5]'           : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')
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31     , 'in_pb[0]'           : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
32     , 'in_pb[1]'           : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
33     , 'in_pb[2]'          : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
34     , 'in_pb[3]'          : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
35     , 'in_pb[4]'          : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')
36
37     # User LEDs
38     , 'out_led_n[0]'       : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
39     , 'out_led_n[1]'       : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
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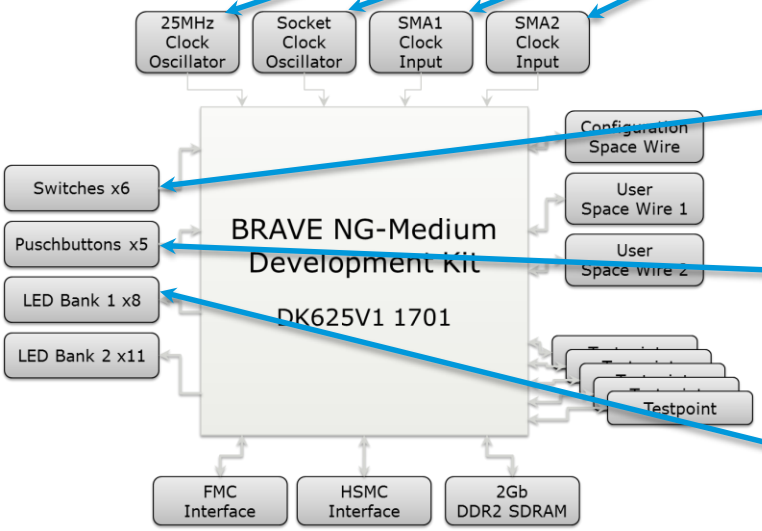
44     , 'out_led_n[6]'       : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
45     , 'out_led_n[7]'       : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')
46
47     #   The LEDs connected to the prog bank need to be define
48     # , 'out_led_prg_n[0]'     : ('D0', 'LVCMOS_3.3V_2mA')
49     # , 'out_led_prg_n[1]'     : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)

Pads Configuration File (Python)

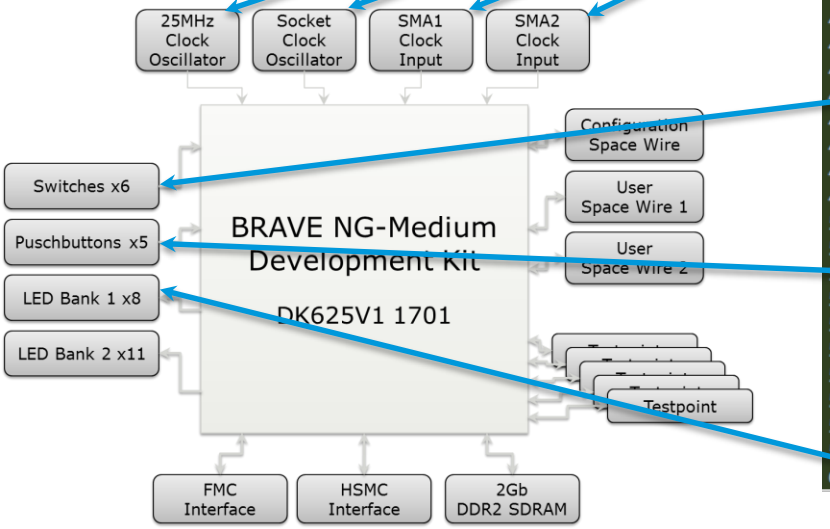



```
27 ----------------------------------------------------------------------------
28
29 entity dk625v1_top is
30
31   port (
32     -- Clock sources
33     in_osc0 : in std_logic;
34     in_osc1 : in st
35     in_sma0 : in st
36     in_sma1 : in st
37
38     -- Switches
39     --      in_sw[0]
40     --      in_sw[1]
41     --      in_sw[2]
42     --      in_sw[3]
43     --      in_sw[4]
44     --      in_sw[5]
45     in_sw : in std_
46     -- Pushbuttons
47     --      in_pb[0]
48     --      in_pb[1]
49     --      in_pb[2]
50     --      in_pb[3]
51     --      in_pb[4]
52     in_pb : in std_
53
54     -- User LEDs
55     --      LEDs cor
56     --          out_
57     --          out_
58     --          ...
59     --          out_
60     out_led_n     :
```

```
16 dk625v1_pads = {
17     # Clock sources
18       'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19     , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20     , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21     , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23     # # Switches and Pushbuttons
24     , 'in_sw[0]'           : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
25     , 'in_sw[1]'           : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
26     , 'in_sw[2]'           : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27     , 'in_sw[3]'           : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
28     , 'in_sw[4]'           : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
29     , 'in_sw[5]'           : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')
30
31     , 'in_pb[0]'           : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
32     , 'in_pb[1]'           : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
33     , 'in_pb[2]'          : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
34     , 'in_pb[3]'          : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
35     , 'in_pb[4]'          : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')
36
37     # User LEDs
38     , 'out_led_n[0]'       : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
39     , 'out_led_n[1]'       : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
40     , 'out_led_n[2]'       : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
41     , 'out_led_n[3]'       : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
42     , 'out_led_n[4]'       : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
43     , 'out_led_n[5]'       : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
44     , 'out_led_n[6]'       : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
45     , 'out_led_n[7]'       : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')
46
47     #   The LEDs connected to the prog bank need to be define
48     # , 'out_led_prg_n[0]'     : ('D0', 'LVCMOS_3.3V_2mA')
49     # , 'out_led_prg_n[1]'     : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)



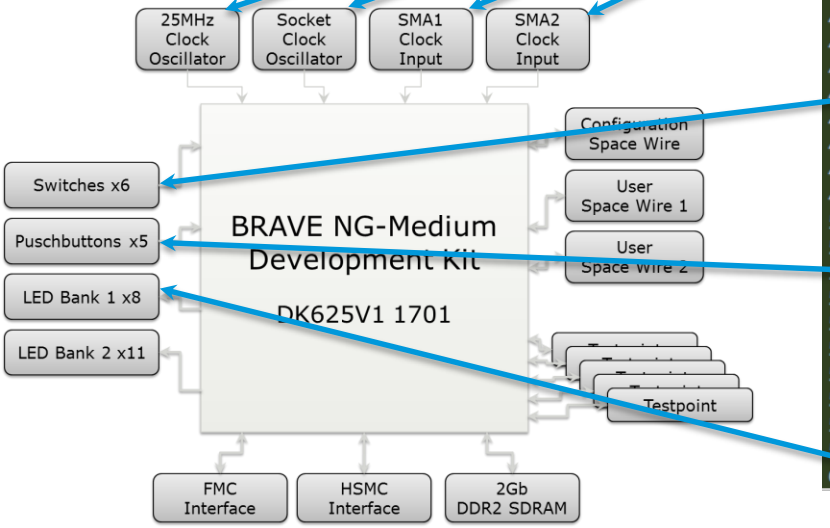

```
27  ----------------------------------------------------------------------------
28
29  entity dk625v1_top is
30
31    port (
32      -- Clock sources
33      in_osc0 : in std_logic;
34      in_osc1 : in st
35      in_sma0 : in st
36      in_sma1 : in st
37
38      -- Switches
39      --      in_sw[0]
40      --      in_sw[1]
41      --      in_sw[2]
42      --      in_sw[3]
43      --      in_sw[4]
44      --      in_sw[5]
45      in_sw : in std_
46      -- Pushbuttons
47      --      in_pb[0]
48      --      in_pb[1]
49      --      in_pb[2]
50      --      in_pb[3]
51      --      in_pb[4]
52      in_pb : in std_
53
54      -- User LEDs
55      --      LEDs cor
56      --          out_
57      --          out_
58      --          ...
59      --          out_
60      out_led_n     :
```

Pads Configuration File (Python)

```
16  dk625v1_pads = {
17      # Clock sources
18      'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19      , 'in_osc1'        : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20      , 'in_sma0'        : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21      , 'in_sma1'        : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23      # # Switches and Pushbuttons
24      , 'in_sw[0]'           : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
25      , 'in_sw[1]'           : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
26      , 'in_sw[2]'           : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27      , 'in_sw[3]'           : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
28      , 'in_sw[4]'           : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
29      , 'in_sw[5]'           : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')
30
31      , 'in_pb[0]'           : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
32      , 'in_pb[1]'           : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
33      , 'in_pb[2]'          : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
34      , 'in_pb[3]'          : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
35      , 'in_pb[4]'          : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')
36
37      # User LEDs
38      , 'out_led_n[0]'       : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
39      , 'out_led_n[1]'       : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
40      , 'out_led_n[2]'       : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
41      , 'out_led_n[3]'       : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
42      , 'out_led_n[4]'       : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
43      , 'out_led_n[5]'       : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
44      , 'out_led_n[6]'       : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
45      , 'out_led_n[7]'       : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')
46
47      #   The LEDs connected to the prog bank need to be define
48      # , 'out_led_prg_n[0]'     : ('D0', 'LVCMOS_3.3V_2mA')
49      # , 'out_led_prg_n[1]'     : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)




```
27  ----------------------------------------------------------------------------
28
29  entity dk625v1_top is
30
31    port (
32      -- Clock sources
33      in_osc0 : in std_logic;
34      in_osc1 : in s
35      in_sma0 : in s
36      in_sma1 : in s
37
38      -- Switches
39      --      in_sw[0]
40      --      in_sw[1]
41      --      in_sw[2]
42      --      in_sw[3]
43      --      in_sw[4]
44      --      in_sw[5]
45      in_sw : in std_
46      -- Pushbuttons
47      --      in_pb[0]
48      --      in_pb[1]
49      --      in_pb[2]
50      --      in_pb[3]
51      --      in_pb[4]
52      in_pb : in std_
53
54      -- User LEDs
55      --      LEDs cor
56      --          out_
57      --          out_
58      --          ...
59      --          out_
60      out_led_n     :
```

Pads Configuration File (Python)

```
16  dk625v1_pads = {
17      # Clock sources
18      'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19    , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20    , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21    , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23    # # Switches and Pushbuttons
24    , 'in_sw[0]'           : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
25    , 'in_sw[1]'           : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
26    , 'in_sw[2]'           : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27    , 'in_sw[3]'           : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
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31    , 'in_pb[0]'           : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
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33    , 'in_pb[2]'          : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
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44    , 'out_led_n[6]'       : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
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47    #   The LEDs connected to the prog bank need to be define
48    # , 'out_led_prg_n[0]'     : ('D0', 'LVCMOS_3.3V_2mA')
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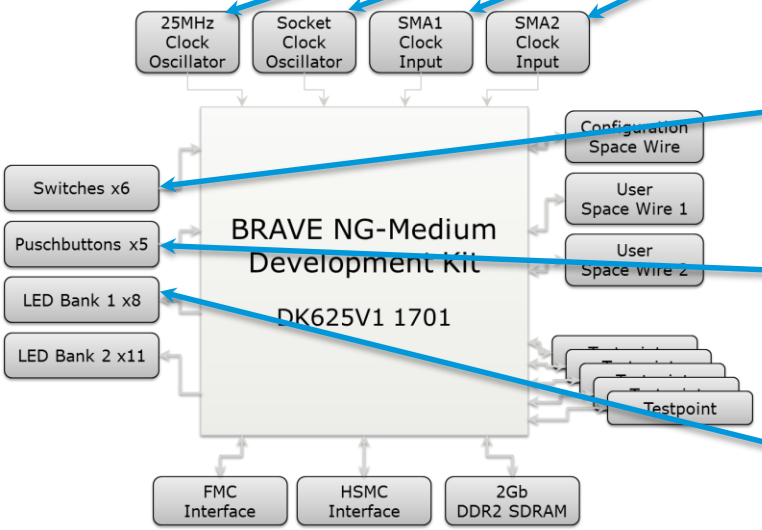
Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)

Pads Configuration File (Python)




```
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43      --      in_sw[4]
44      --      in_sw[5]
45      in_sw : in std_
46      -- Pushbuttons
47      --      in_pb[0]
48      --      in_pb[1]
49      --      in_pb[2]
50      --      in_pb[3]
51      --      in_pb[4]
52      in_pb : in std_
53
54      -- User LEDs
55      --      LEDs cor
56      --          out_
57      --          out_
58      --          ...
59      --          out_
60      out_led_n     :
```

```
16  dk625v1_pads = {
17      # Clock sources
18      'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19    , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20    , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21    , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23    # # Switches and Pushbuttons
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26    , 'in_sw[2]'         : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27    , 'in_sw[3]'         : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
28    , 'in_sw[4]'         : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
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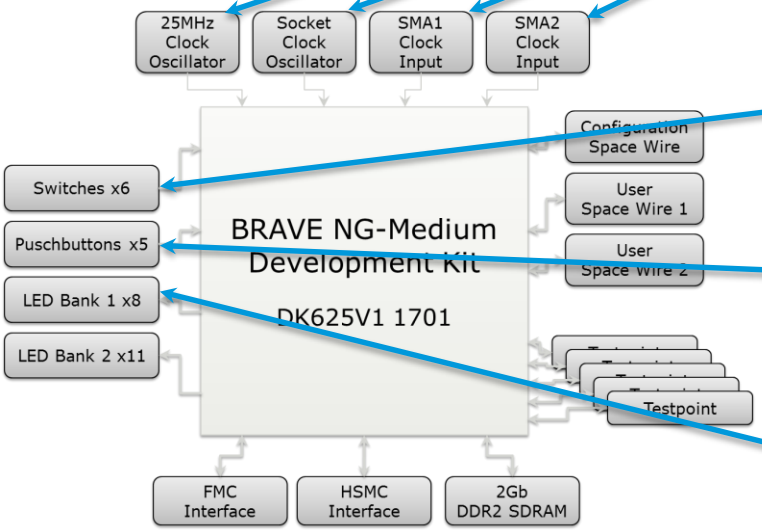
30
31    , 'in_pb[0]'         : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
32    , 'in_pb[1]'         : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
33    , 'in_pb[2]'        : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
34    , 'in_pb[3]'        : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
35    , 'in_pb[4]'        : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')
36
37    # User LEDs
38    , 'out_led_n[0]'     : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
39    , 'out_led_n[1]'     : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
40    , 'out_led_n[2]'     : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
41    , 'out_led_n[3]'     : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
42    , 'out_led_n[4]'     : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
43    , 'out_led_n[5]'     : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
44    , 'out_led_n[6]'     : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
45    , 'out_led_n[7]'     : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')
46
47    #   The LEDs connected to the prog bank need to be define
48    # , 'out_led_prg_n[0]'    : ('D0', 'LVCMOS_3.3V_2mA')
49    # , 'out_led_prg_n[1]'    : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)

Pads Configuration File (Python)




```
entity dk625v1_top is

  port (
    -- Clock sources
    in_osc0 : in std_logic;
    in_osc1 : in std_
    in_sma0 : in std_
    in_sma1 : in std_

    -- Switches
    --      in_sw[0]
    --      in_sw[1]
    --      in_sw[2]
    --      in_sw[3]
    --      in_sw[4]
    --      in_sw[5]
    in_sw : in std_
    -- Pushbuttons
    --      in_pb[0]
    --      in_pb[1]
    --      in_pb[2]
    --      in_pb[3]
    --      in_pb[4]
    in_pb : in std_

    -- User LEDs
    --      LEDs cor
    --          out_
    --          out_
    --          ...
    --          out_
    out_led_n     :
```

```
dk625v1_pads = {
    # Clock sources
    'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
    'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
    'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
    'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #

    # # Switches and Pushbuttons
    , 'in_sw[0]'         : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
    , 'in_sw[1]'         : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
    , 'in_sw[2]'         : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
    , 'in_sw[3]'         : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
    , 'in_sw[4]'         : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
    , 'in_sw[5]'         : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')

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    , 'in_pb[2]'         : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
    , 'in_pb[3]'         : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
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    # User LEDs
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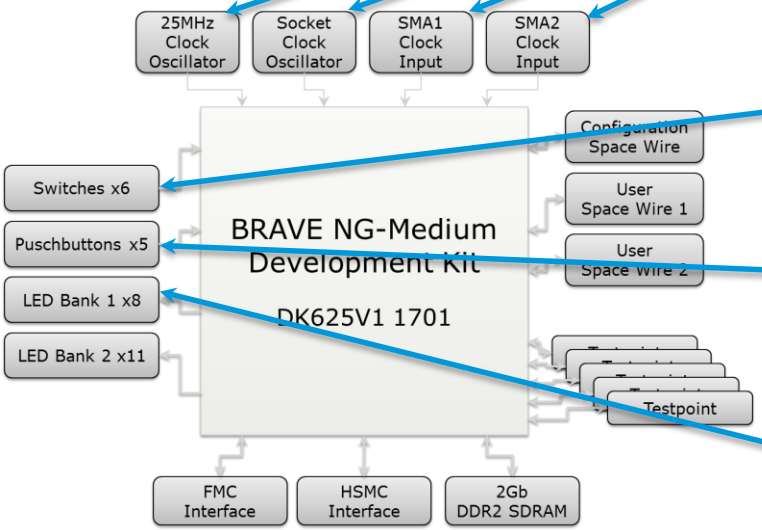
    , 'out_led_n[2]'     : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
    , 'out_led_n[3]'     : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
    , 'out_led_n[4]'     : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
    , 'out_led_n[5]'     : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
    , 'out_led_n[6]'     : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
    , 'out_led_n[7]'     : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')

    #   The LEDs connected to the prog bank need to be define
    # , 'out_led_prg_n[0]'    : ('D0', 'LVCMOS_3.3V_2mA')
    # , 'out_led_prg_n[1]'    : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)

Pads Configuration File (Python)




```
entity dk625v1_top is

  port (
    -- Clock sources
    in_osc0 : in std_logic;
    in_osc1 : in std_logic;
    in_sma0 : in std_logic;
    in_sma1 : in std_logic;

    -- Switches
    --      in_sw[0]
    --      in_sw[1]
    --      in_sw[2]
    --      in_sw[3]
    --      in_sw[4]
    --      in_sw[5]
    in_sw : in std_logic_vector(5 downto 0);
    -- Pushbuttons
    --      in_pb[0]
    --      in_pb[1]
    --      in_pb[2]
    --      in_pb[3]
    --      in_pb[4]
    in_pb : in std_logic_vector(4 downto 0);

    -- User LEDs
    --      LEDs connected to the prog bank need to be defined
    --          out_led_prg_n[0]
    --          out_led_prg_n[1]
    --          ...
    --          out_led_prg_n[7]
    out_led_n : out std_logic_vector(7 downto 0);
```

```
dk625v1_pads = {
    # Clock sources
    'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
  , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
  , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
  , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #

  # # Switches and Pushbuttons
  , 'in_sw[0]'         : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
  , 'in_sw[1]'         : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
  , 'in_sw[2]'         : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
  , 'in_sw[3]'         : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
  , 'in_sw[4]'         : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
  , 'in_sw[5]'         : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')

  , 'in_pb[0]'         : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
  , 'in_pb[1]'         : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
  , 'in_pb[2]'         : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
  , 'in_pb[3]'         : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
  , 'in_pb[4]'         : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')

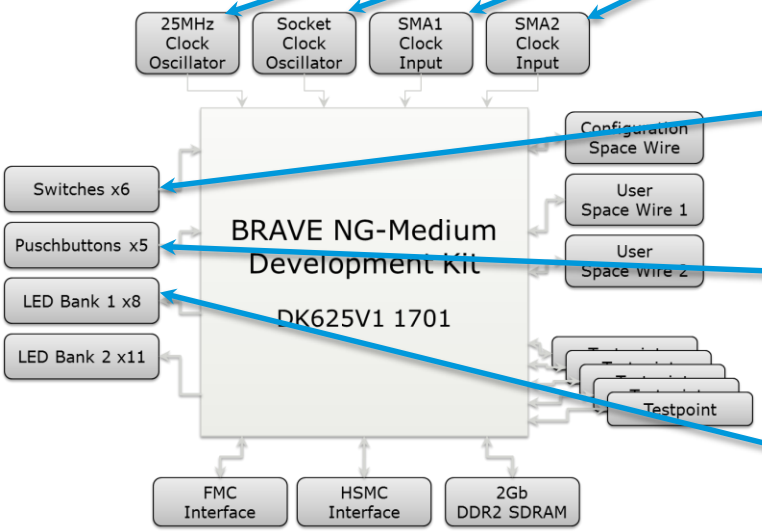
  # User LEDs
  , 'out_led_n[0]'     : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[1]'     : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[2]'     : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[3]'     : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[4]'     : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[5]'     : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[6]'     : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
  , 'out_led_n[7]'     : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')

  #   The LEDs connected to the prog bank need to be define
  # , 'out_led_prg_n[0]'    : ('D0', 'LVCMOS_3.3V_2mA')
  # , 'out_led_prg_n[1]'    : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment – VHDL Top File and Pads Configuration File

Board Top File (VHDL)

Pads Configuration File (Python)



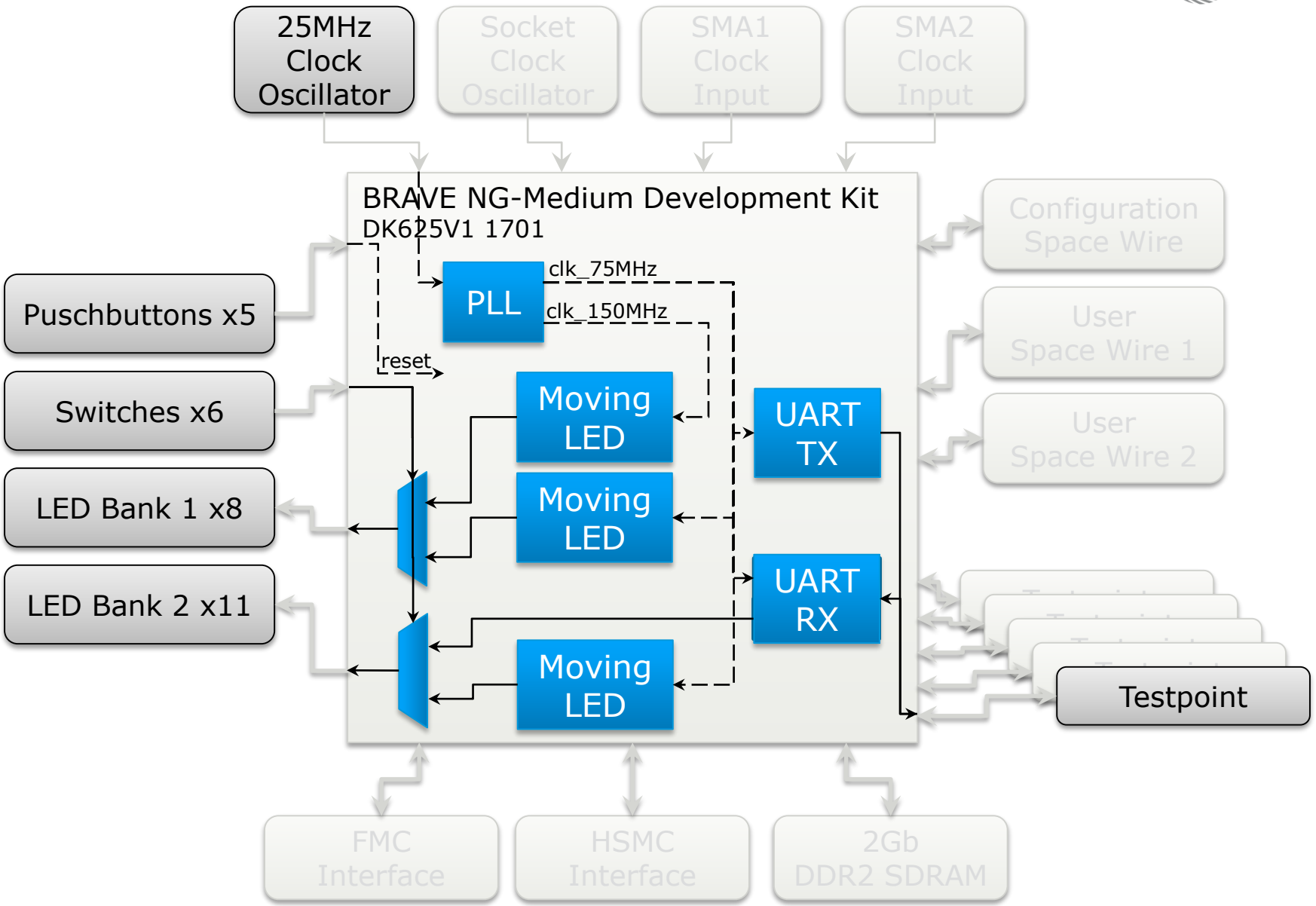

```
27  ----------------------------------------------------------------------------
28
29  entity dk625v1_top is
30
31    port (
32      -- Clock sources
33      in_osc0 : in std_logic;
34      in_osc1 : in s
35      in_sma0 : in s
36      in_sma1 : in s
37
38      -- Switches
39      --      in_sw[0]
40      --      in_sw[1]
41      --      in_sw[2]
42      --      in_sw[3]
43      --      in_sw[4]
44      --      in_sw[5]
45      in_sw : in std_
46      -- Pushbuttons
47      --      in_pb[0]
48      --      in_pb[1]
49      --      in_pb[2]
50      --      in_pb[3]
51      --      in_pb[4]
52      in_pb : in std_
53
54      -- User LEDs
55      --      LEDs cor
56      --          out_
57      --          out_
58      --          ...
59      --          out_
60      out_led_n
```

```
16  dk625v1_pads = {
17      # Clock sources
18      'in_osc0'          : ('IOB12_D09P', 'LVCMOS_2.5V_2mA') #
19    , 'in_osc1'          : ('IOB12_D08P', 'LVCMOS_2.5V_2mA') #
20    , 'in_sma0'          : ('IOB0_D10P', 'LVCMOS_3.3V_2mA')  #
21    , 'in_sma1'          : ('IOB0_D11P', 'LVCMOS_3.3V_2mA')  #
22
23      # # Switches and Pushbuttons
24    , 'in_sw[0]'         : ('IOB10_D09P', 'LVCMOS_1.8V_2mA')
25    , 'in_sw[1]'         : ('IOB10_D03P', 'LVCMOS_1.8V_2mA')
26    , 'in_sw[2]'         : ('IOB10_D03N', 'LVCMOS_1.8V_2mA')
27    , 'in_sw[3]'         : ('IOB10_D04P', 'LVCMOS_1.8V_2mA')
28    , 'in_sw[4]'         : ('IOB10_D09N', 'LVCMOS_1.8V_2mA')
29    , 'in_sw[5]'         : ('IOB10_D04N', 'LVCMOS_1.8V_2mA')
30
31    , 'in_pb[0]'         : ('IOB10_D07P', 'LVCMOS_1.8V_2mA')
32    , 'in_pb[1]'         : ('IOB10_D12P', 'LVCMOS_1.8V_2mA')
33    , 'in_pb[2]'         : ('IOB10_D07N', 'LVCMOS_1.8V_2mA')
34    , 'in_pb[3]'         : ('IOB10_D12N', 'LVCMOS_1.8V_2mA')
35    , 'in_pb[4]'         : ('IOB10_D14P', 'LVCMOS_1.8V_2mA')
36
37      # User LEDs
38    , 'out_led_n[0]'     : ('IOB0_D01P', 'LVCMOS_3.3V_2mA')
39    , 'out_led_n[1]'     : ('IOB0_D03N', 'LVCMOS_3.3V_2mA')
40    , 'out_led_n[2]'     : ('IOB0_D03P', 'LVCMOS_3.3V_2mA')
41    , 'out_led_n[3]'     : ('IOB1_D05N', 'LVCMOS_3.3V_2mA')
42    , 'out_led_n[4]'     : ('IOB1_D05P', 'LVCMOS_3.3V_2mA')
43    , 'out_led_n[5]'     : ('IOB1_D06N', 'LVCMOS_3.3V_2mA')
44    , 'out_led_n[6]'     : ('IOB1_D06P', 'LVCMOS_3.3V_2mA')
45    , 'out_led_n[7]'     : ('IOB1_D02N', 'LVCMOS_3.3V_2mA')
46
47      #   The LEDs connected to the prog bank need to be define
48      # , 'out_led_prg_n[0]'    : ('D0', 'LVCMOS_3.3V_2mA')
49      # , 'out_led_prg_n[1]'    : ('D1', 'LVCMOS_3.3V_2mA')
```

Development Environment

- The development environment includes:
  - Latest documentation by NanoXplore
  - Script to compile/synthesize a project
  - Script to program the device
  - Makefile which automates the complete process
  - VHDL top module with corresponding pads configuration
    - matches with available connectors on BRAVE Dev-Kit
  - Example project
    - Uses LEDs, switches, pushbuttons, PLL, testpoints (TP)
    - Dedicated UART receiver and transmitter

Example Project



Example Project - Demo

Demo

Questions?

?

Development of a BRAVE Demonstrator Application

Thomas Lange

29/08/2017

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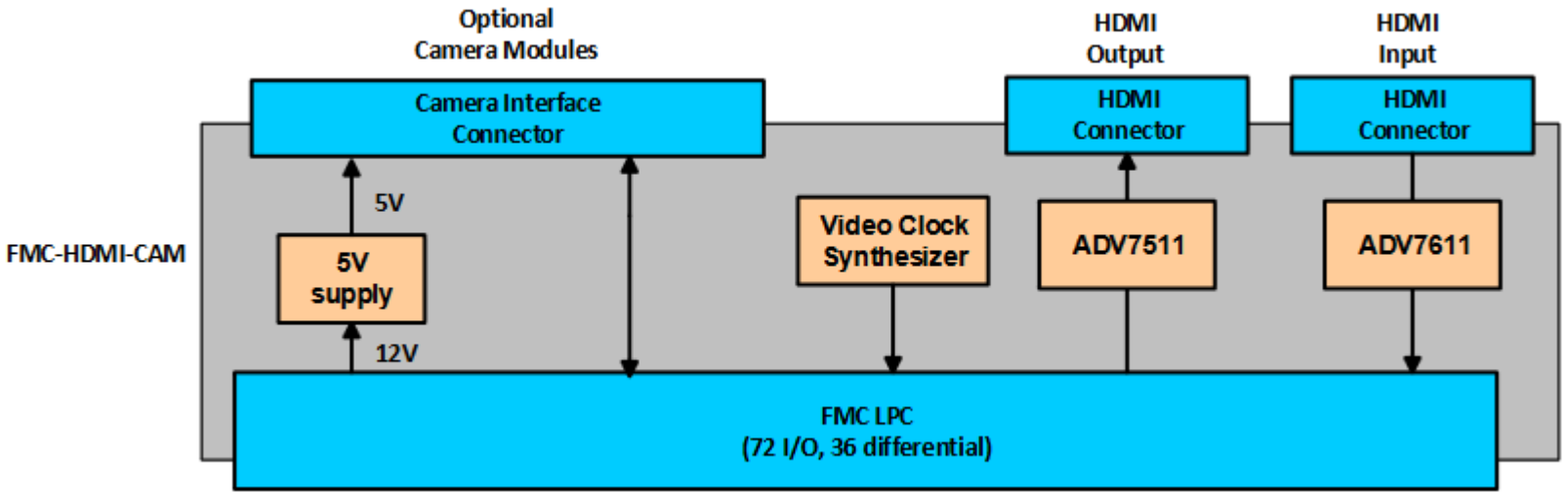
BRAVE Demonstrator Application - Outline

1. Motivation
2. FMC-HDMI-CAM Daughterboard
3. Development Process
4. Demo
5. Summary of Development Status
6. Future Work

Motivation

- Development of a demonstrator application for the BRAVE NG-Medium
- Gets the easily attention
    - ↪ Image/Video application

FMC-HDMI-CAM Daughterboard

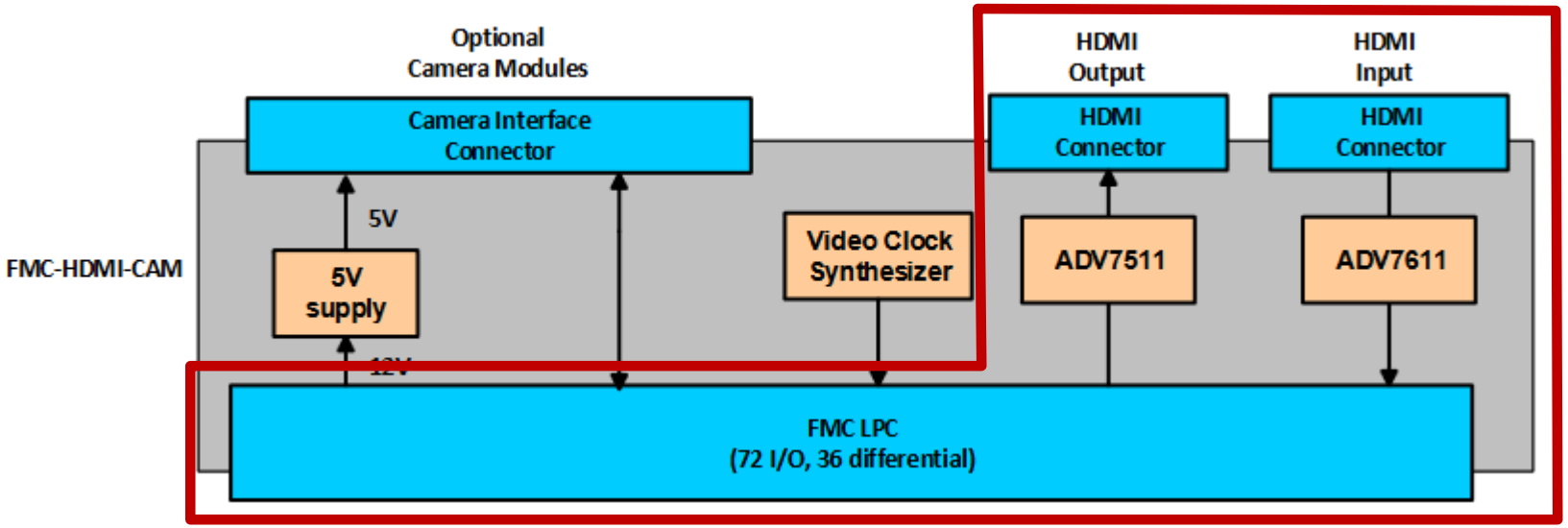


Source: Avnet

- FMC daughterboard by Avnet
  - Using the FMC connector (mezzanine card interface)
  - HDMI Input (based on ADI ADV6711)
  - HDMI Output (based on ADI ADV7511)
  - Video Clock Synthesizer (based on TI CDCE913)
  - Camera Interface (for camera modules)

- Avnet provides reference design (https://github.com/Avnet/hdl)

FMC-HDMI-CAM Daughterboard



Source: Avnet

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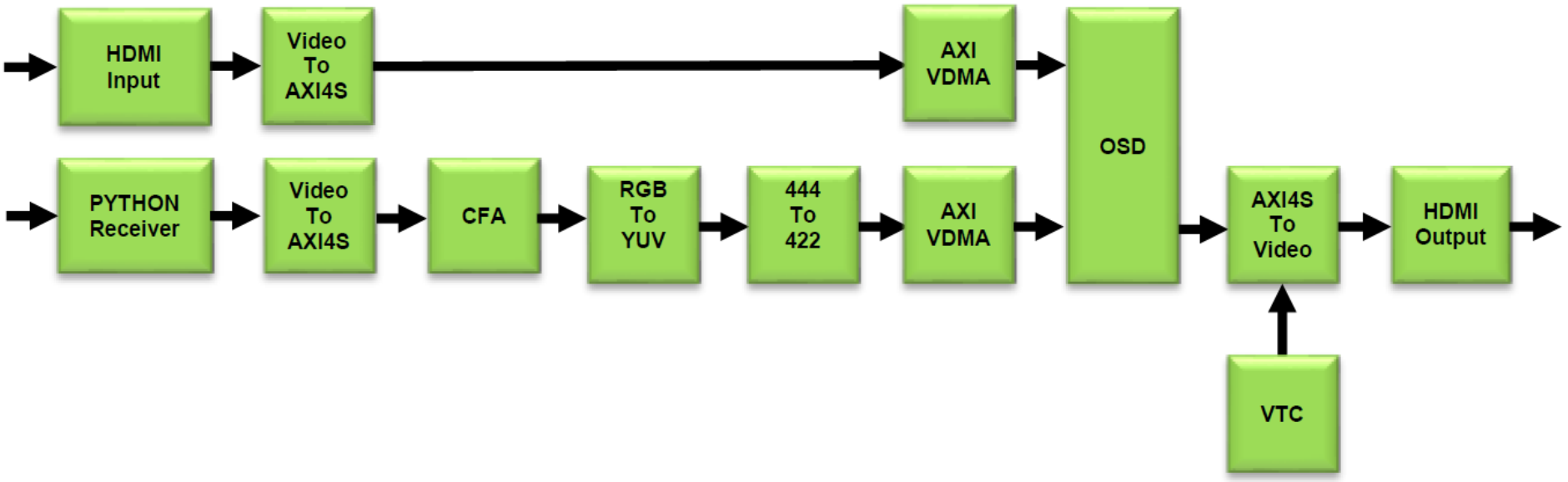
  - HDMI Output (based on ADI ADV7511)
  - Video Clock Synthesizer (based on TI CDCE913)
  - Camera Interface (for camera modules)

- Avnet provides reference design (https://github.com/Avnet/hdl)

FMC-HDMI-CAM Daughterboard – Reference design



Source: Avnet

- Reference design supports Zync-Board or ZedBoard
  - Technology dependent HDL code
  - Some of the used IP cores need licenses
  - I2C configuration of HDMI in-/output chips through embedded ARM core

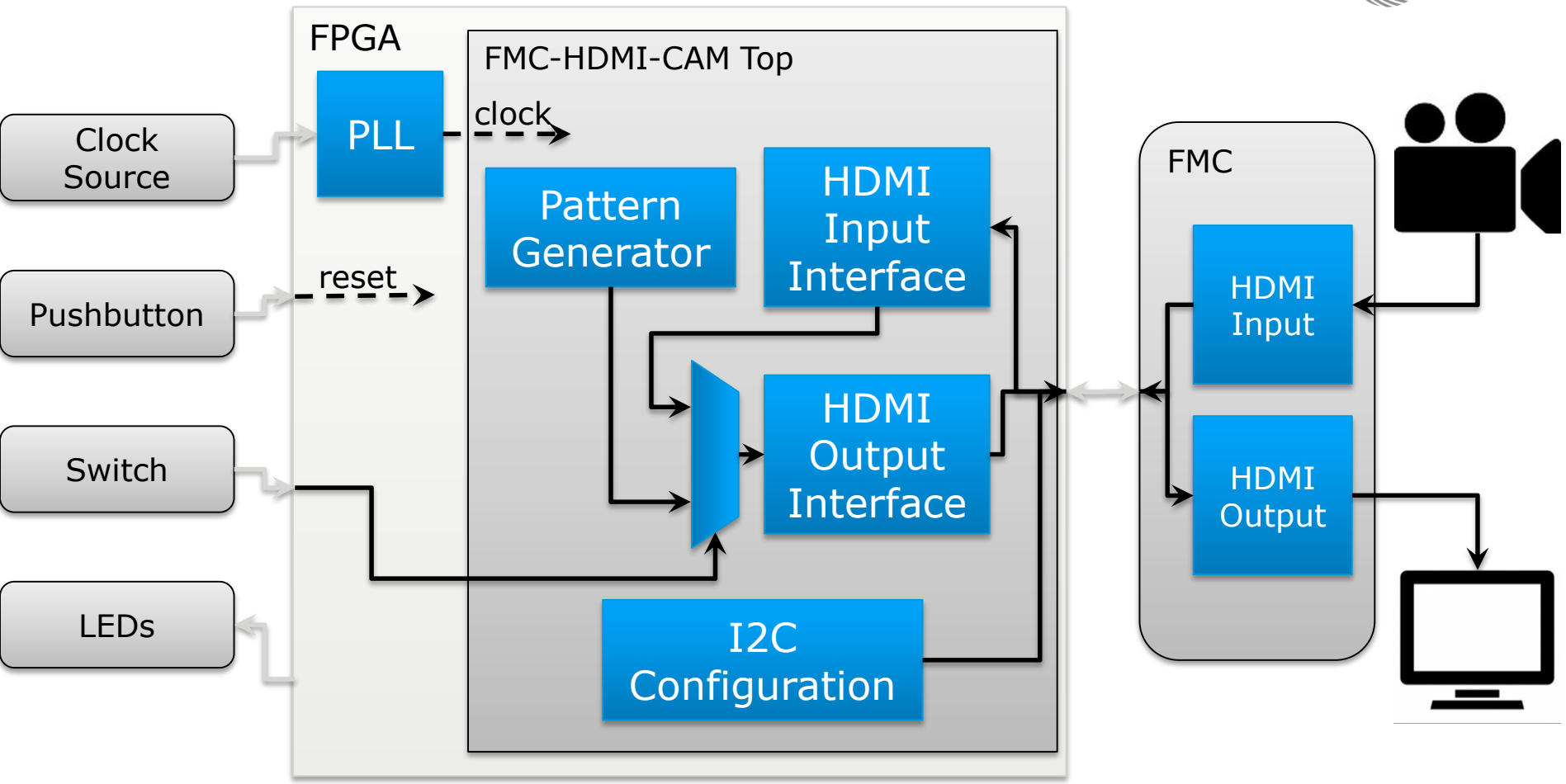
Development Process

- Design porting issues:
  - I2C configuration of HDMI chips is done by embedded ARM core
    - BRAVE NG-Medium does not provide hard-wired processor
  - Technology dependent HDL code
  - Some of the used IP cores need licenses

- Development steps:
  - Simplify design ↪ no licenses for IP cores needed
  - Porting to Xilinx 7-Series FPGA (Kintex-7 KC705)
    - Integrate dedicated I2C IP core
    - Identify required I2C messages
  - Porting to Microsemi RTG4 Dev-Kit
    - Rewrite HDL code technology independent
  - Porting to NanoXplore BRAVE NG-Medium DK625V1
    - Handle not yet supported features
    - Handle issues of current tool versions

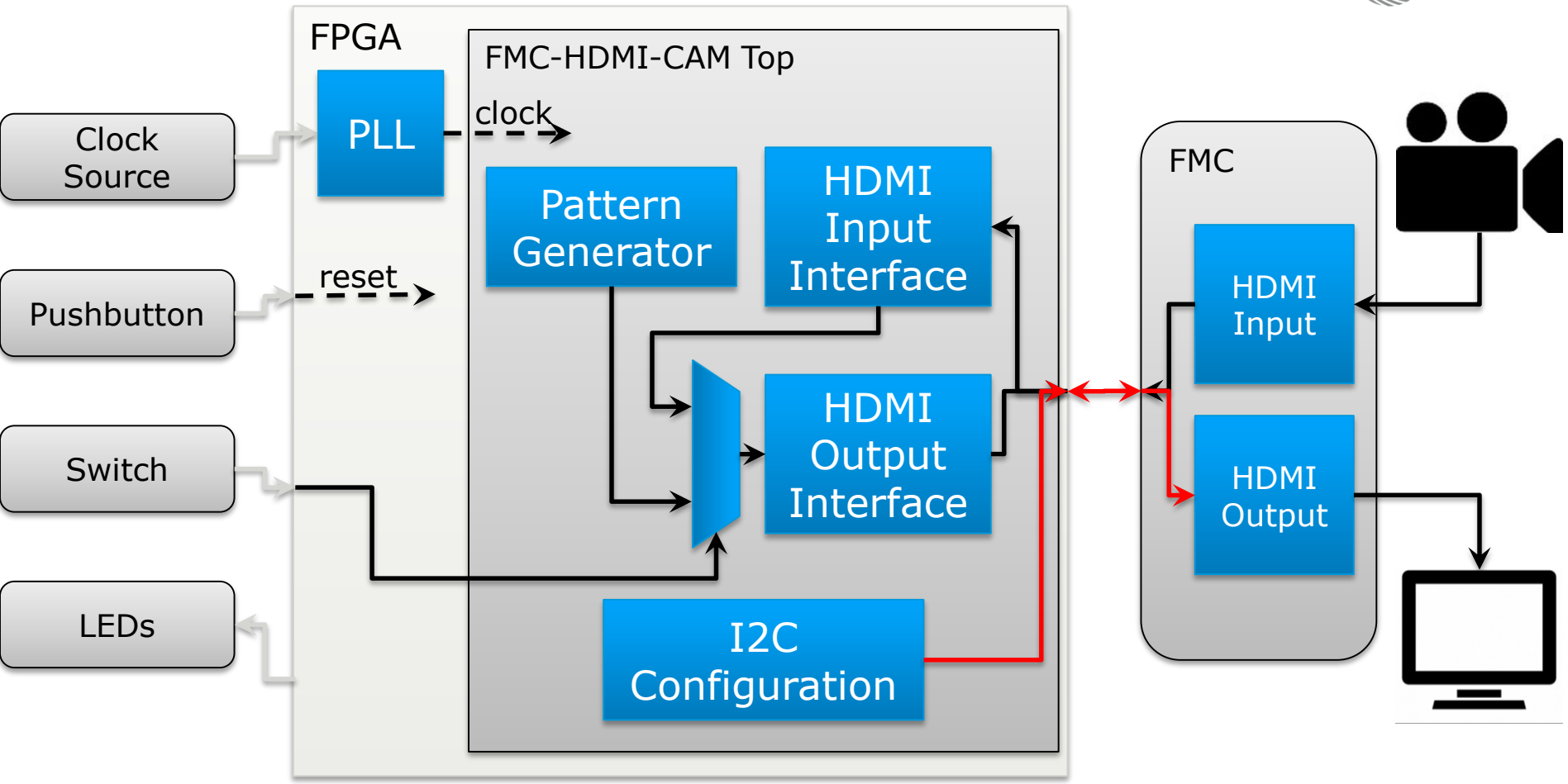
Demo

Demo – Implemented Design (High Level)



- Technology independent design (FMC-HDMI-CAM Top)
  - Configuration via dedicated I2C master
  - HDMI Output stream with Video Pattern Generator
  - HDMI In-/Output stream pass through

Demo – Implemented Design (High Level)



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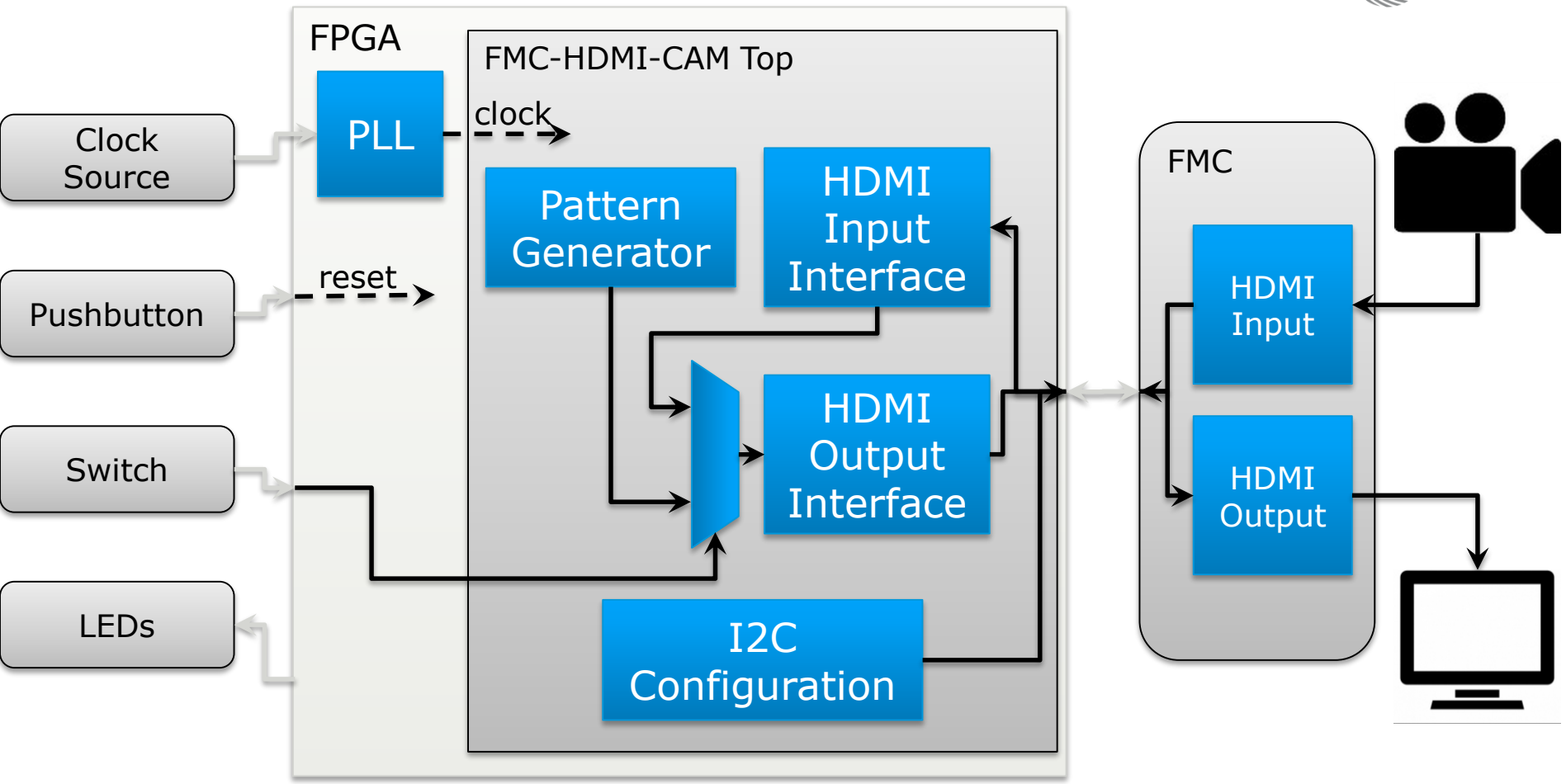
Demo – Implemented Design (High Level)



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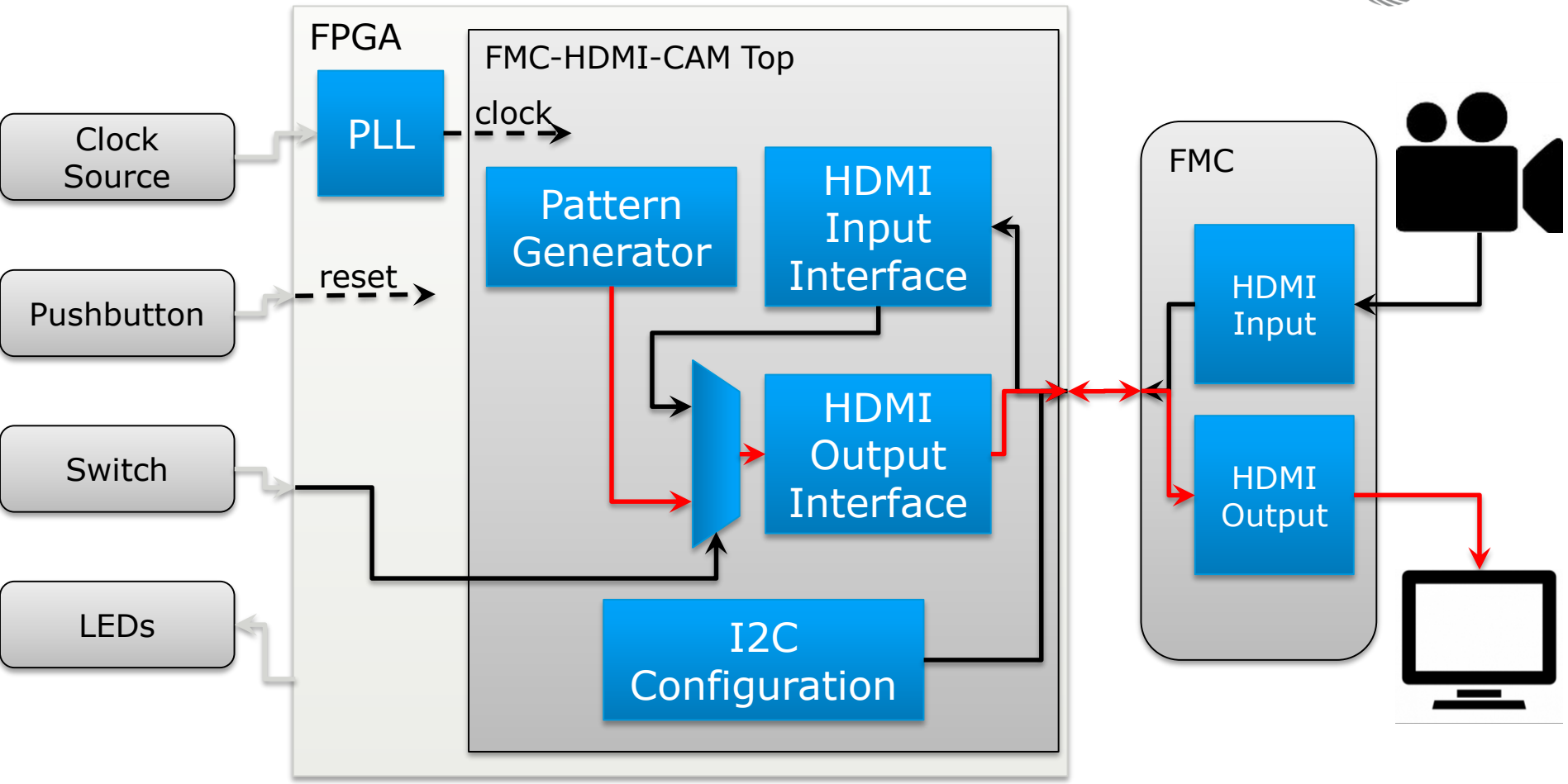
Demo – Implemented Design (High Level)



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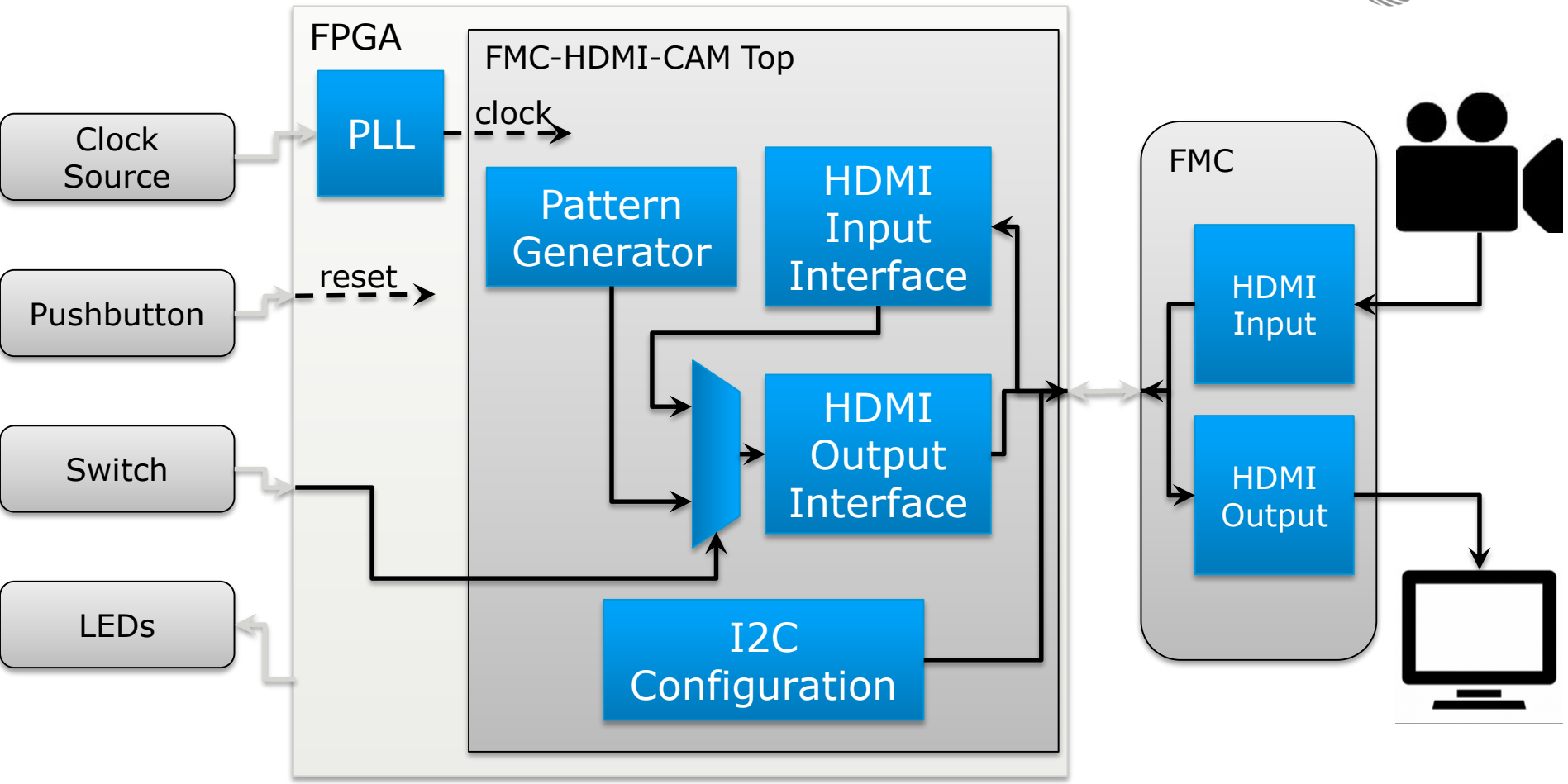
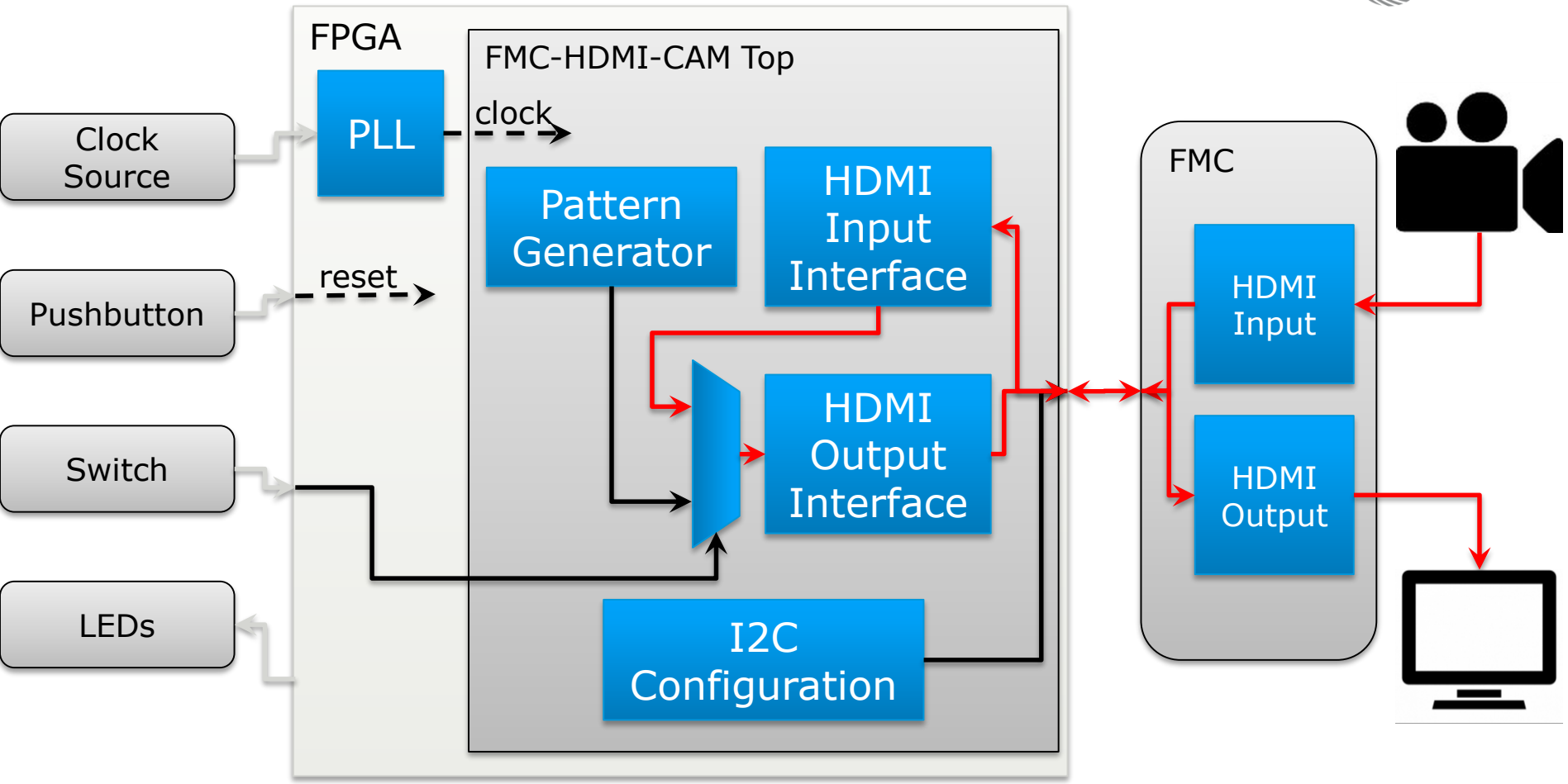
Demo – Implemented Design (High Level)



- Technology independent design (FMC-HDMI-CAM Top)
  - Configuration via dedicated I2C master
  - HDMI Output stream with Video Pattern Generator
  - HDMI In-/Output stream pass through

Demo – Implemented Design (High Level)



- Technology independent design (FMC-HDMI-CAM Top)
  - Configuration via dedicated I2C master
  - HDMI Output stream with Video Pattern Generator
  - HDMI In-/Output stream pass through

Summary of Development Status

- HDMI In-/Output interface is technology independent
- Dedicated I2C Master core is implemented
    - Configuration of HDMI In-/Output through I2C
- Video Pattern Generator is implemented

- Xilinx Kintex-7 KC705:
    - HDMI Output with pattern generator
    - HDMI Input – HDMI Output pass through

- Microsemi RTG4 Dev-Kit:
    - HDMI Output with pattern generator

- NanoXplore BRAVE NG-Medium DK625V1:
    - HDMI Output with pattern generator (with artefacts)

Future Work

- Continue porting to BRAVE NG-Medium Dev-Kit
  - Probably solved with new release of the tool
- Implementation of actual image/video application by Klemen Bravhar
  - Usage of MATLAB HDL coder

Questions?

?

Open ESA FPGA Benchmark Suite

Thomas Lange, David Merodio Codinachs

29/08/2017

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Open ESA FPGA Benchmark Suite - Outline

1. Motivation
2. Methodology
3. Open ESA FPGA Benchmark Suite - Overview
4. Benchmark Circuits
5. Public Availability
6. Current Development Status
7. Conclusion

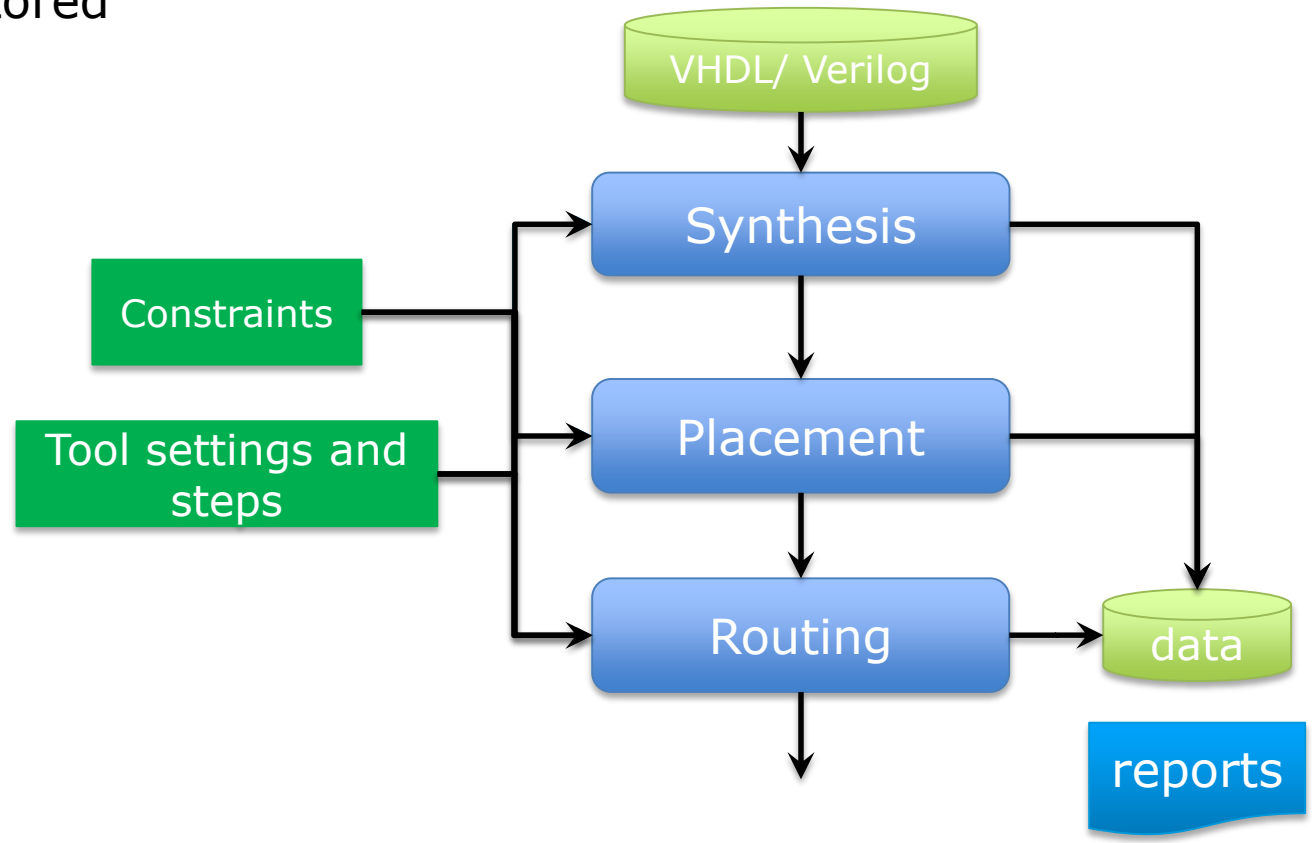
Motivation

- The offer of FPGAs for space is increasing; as well as their complexity
- FPGAs have different architectures and tools
- No industry standard for benchmarking PLDs (as it exists for CPUs)
  - ⮑ Difficult to chose devices for given application
- FPGAs are very versatile
  - ⮑ A flexible benchmark environment is needed which
    - ⮑ addresses many aspects
    - ⮑ can be modified for specific purposes

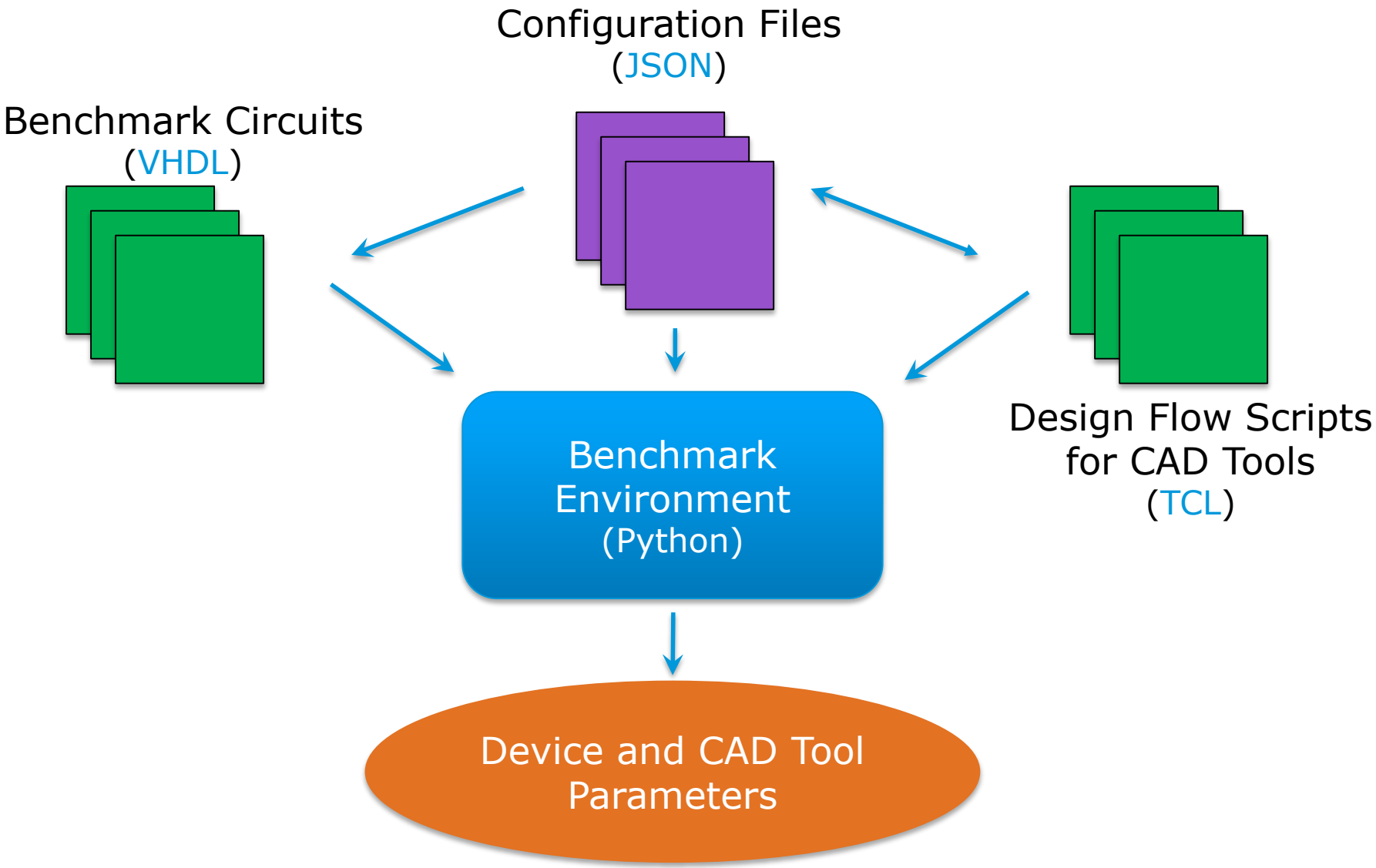
⮑ Large companies have internal benchmarks, methodology and automation. Universities, research institutes and smaller companies might benefit from the benchmarks, data and automation sharing.

Methodology

- The benchmark environment automates the standard FPGA design flow
- The steps are performed on several devices by using the corresponding CAD tools
- After each step in the design flow the parameters are extracted and stored



Open ESA FPGA Benchmark Suite - Overview



Open ESA FPGA Benchmark Suite - Overview

- The Open ESA FPGA Benchmark Suite consists of
  - Benchmark circuits (VHDL)
  - CAD tool specific design flow scripts (TCL)
  - Benchmark Environment (Python)
  - Configuration Files (JSON)

- The device parameters are currently (can be extended):
  - logic capacity
  - speed performance
  - power
- The current CAD tool parameters are (can be extended):
  - compile time
  - memory usage

Public Availability

- The benchmark environment is organized in a Git repository

  https://gitrepos.estec.esa.int/FPGA/open-ESA-FPGA-benchmark-suite.git

- The availability to the public enables
  - Experience can be shared
  - the possibility to add and modify circuits for own purposes, e.g.
    - add new circuits which address different architectural features
  - the possibility to add and modify design flows, e.g.
    - add design flow with special constraints
    - add design flow with different CAD tool settings/versions
    - add design flow for new CAD tools

The use and collaboration of the suite is highly encouraged!

Design flow configuration example

Example of design flow configuration (designFlowSettings.json):

```
1  {
2      "ISE 13.2": {
3          "shellCLI"   : "xtclsh",
4          "toolSetup"  : "tools/xilinx/ise13.2_64_env.csh",
5          "createPrj"  : "tools/xilinx/new_ise_project.tcl",
6          "synPrj"     : "tools/xilinx/syn_ise.tcl"
7      },
8      "ISE 14.7": {
9          "shellCLI"   : "xtclsh",
10         "toolSetup"  : "tools/xilinx/ise14.7_64_env.csh",
11         "createPrj"  : "tools/xilinx/new_ise_project.tcl",
12         "synPrj"     : "tools/xilinx/syn_ise.tcl"
13     },
14     "Libero SoC 11.7": {
15         "shellCLI"   : "libero",
16         "toolSetup"  : [
17             "tools/microsemi/libero_env.csh",
18             "tools/microsemi/synopsys_env.csh"
19         ],
20         "createPrj"  : "tools/microsemi/new_libero_project.tcl",
21         "synPrj"     : "tools/microsemi/syn_libero.tcl"
22     }
23 }
```

Flow name

Shell command

Script to create the Project

Script to perform Synthesis, Place & Route

Scripts to setup the tools

Device configuration example

```
{
    "Virtex-5QV"  : {
        "tools" : "ISE 13.2",
        "deviceSpec"  : {
            "family"  : "Virtex-5QV",
            "die"     : "xqr5vfx130",
            "package" : "cf1752",
            "speed"   : "-1",
        }
    },
    "Kintex-7"    : {
        "tools" : [
            "ISE 13.2",
            "ISE 14.7"
        ],
        "deviceSpec" : {
            "family"  : "Kintex7",
            "die"     : "xc7k70t",
            "package" : "fbg676",
            "speed"   : "-3",
        }
    },
    "RTG4"    : {
        "tools"      : "Libero SoC 11.7",
        "deviceSpec" : {
            "family"     : "RTG4",
            "die"        : "RT4G150",
            "package"    : "1657 CG",
            "speed"      : "STD",
            "dieVoltage" : "1.2"
        }
    }
}
```

Example of device configuration (deviceSettings.json):

Device name

Flow names (see previous slide)

Device definition

Project configuration example

Example of project configuration (prjSettings.json):

```
1  {
2      "name" : "generic_logic_gate",
3      "hdlFiles" : [
4          "../../utils/hdl/io_ff.vhd",
5          "../../utils/hdl/io_reg.vhd",
6          "../../utils/hdl/utils.vhd",
7          "../../utils/hdl/reduce_pack.vhd",
8          "./hdl/generic_logic_gate.vhd"
9      ],
10     "vhdlVersion" : "VHDL1993"
11 }
```

Project name created by the FPGA tool

Benchmark execution example

- Steps to execute the benchmark:
  1. Initialize the environment

```
$ source utilities/set_env.sh  # use with Bash shell
$ source utilities/set_env.csh # use with C shell
```

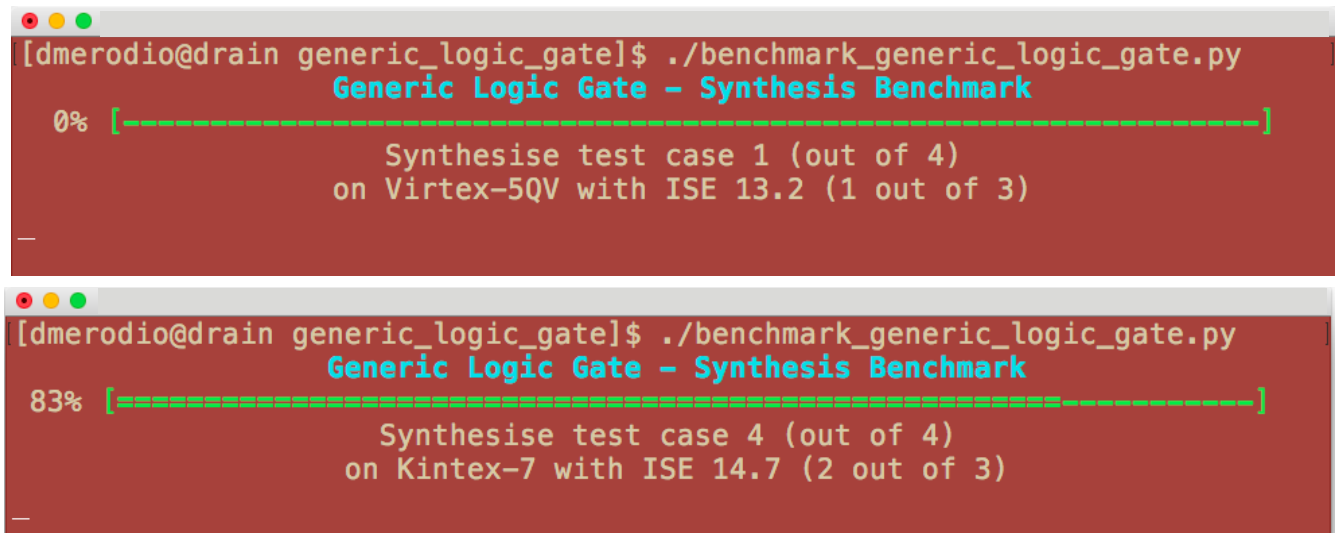
  2. Got to work directory

```
$ cd circuits/basic/generic_logic_gate/
```

  3. Run the benchmark

```
$ ./benchmark_generic_logic_gate.py
```

Output during execution



Benchmark Circuits

- Initial set of benchmark circuits provided
  - inspired by PREP, ITC'99 and IWLS benchmark suites

- Small designs which address only particular architectural features
  - LUTs
  - carry propagation logic
  - DSP-blocks
  - memory cells

- More complex circuits which represent common arithmetic functions
  - e.g. Adder Tree, CORDIC, Moving Average Filter, UART (FSM), …
  - ⮑ resource usage and performance can be estimated for real designs

- The number of benchmark circuits is expected to grow

Current Development Status

- The repository includes an initial set of benchmark circuits
- The integrated CAD tools currently included:
  - Xilinx ISE
  - Microsemi Libero
- Ongoing:
  - Integration of further CAD tools (NanoXmap)
  - Automation to parse reports of the tools to extract parameters

Conclusion

- The Open ESA FPGA Benchmark Suite
  - enables acquire experience of FPGAs by different vendors and their CAD tools
  - is publicly available
    - ➥ transparent results
  - has an "open interface"
    - ➥ integration and modification of additional benchmark circuits, FPGAs and CAD tools is possible

References

1. D. McCarty, D. Faria, and P. Alfke, “PREP Benchmarks for Programmable Logic Devices” in Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993, pp. 7.7.1–7.7.6, May 1993.
2. F. Corno, M. S. Reorda, and G. Squillero, “RT-level ITC’99 benchmarks and first ATPG results” IEEE Design Test of Computers, vol. 17, pp. 44–53, Jul 2000.
3. “White Paper: Guidance for Accurately Benchmarking FPGAs” tech. rep., Altera Corporation, Dec 2007.
4. S. Kliman, “PREP Benchmarks Reveal Performance and Capacity Tradeoffs of Programmable Logic Devices” in Proceedings Seventh Annual IEEE International ASIC Conference and Exhibit, pp. 376–382, Sep 1994.
5. “White Paper: FPGA Performance Benchmarking Methodology” tech. rep., Altera Corporation, Aug 2007.
6. C. Albrecht, “IWLS 2005 Benchmarks.” Online: http://iwls.org/iwls2005/benchmark presentation.pdf (accesed March 2017), Jun 2005.

Radiation Test of a Xilinx Kintex-7

Thomas Lange

29/08/2017

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Radiation test of a Xilinx Kintex-7 - Outline

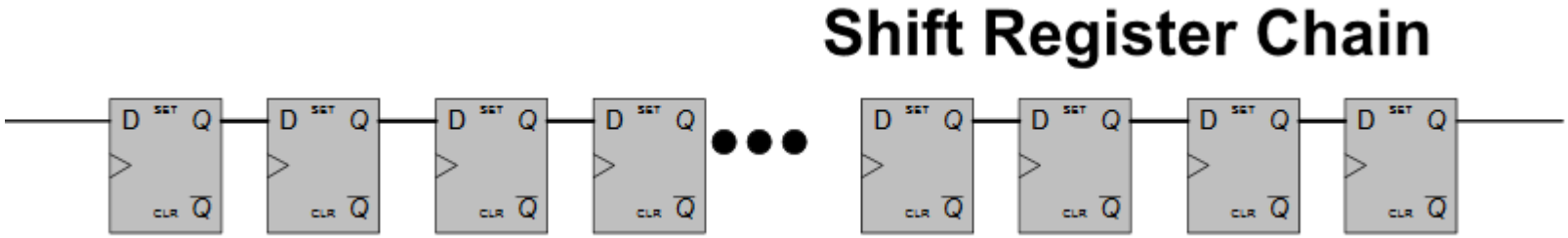
1. Motivation
2. Test Set-Up
3. Device Under Test
4. Summary Test Results

Motivation

- Singe Event Effects (SEE) characterization is used to predict design error rates
- Radiation test experiments common test methodology is shift register based
- Methodology issue: not close to real designs

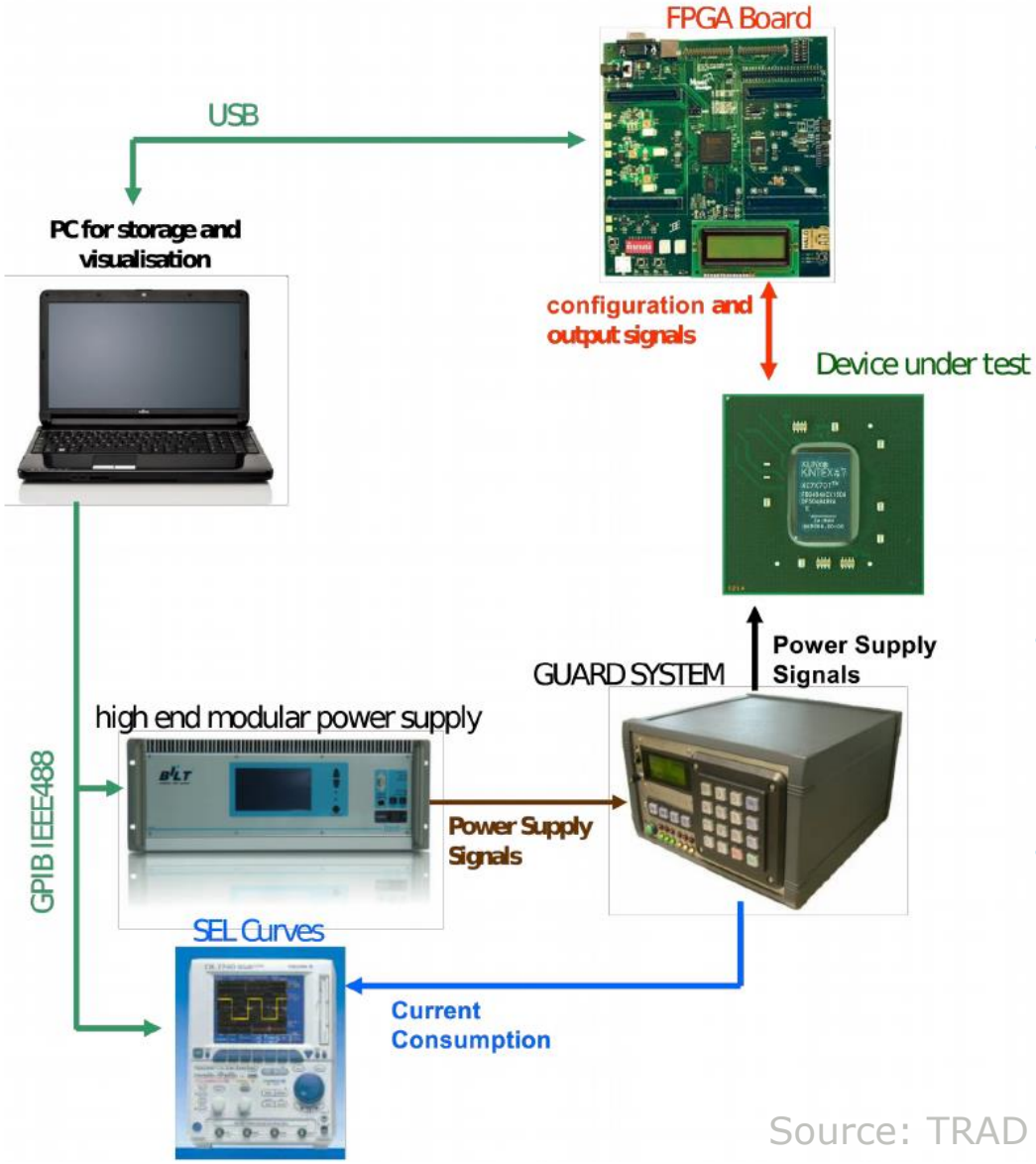
↪ Implementation of more complex designs with
  - Logic cones at inputs and outputs of Flip Flops
  - Realistic combinatorial stages between Flip Flops

- Radiation test of a Kintex-7 by TRAD
  - Irradiation was performed at RADEF with not tilted heavy ions



Source: M. Berg

Test Set-Up

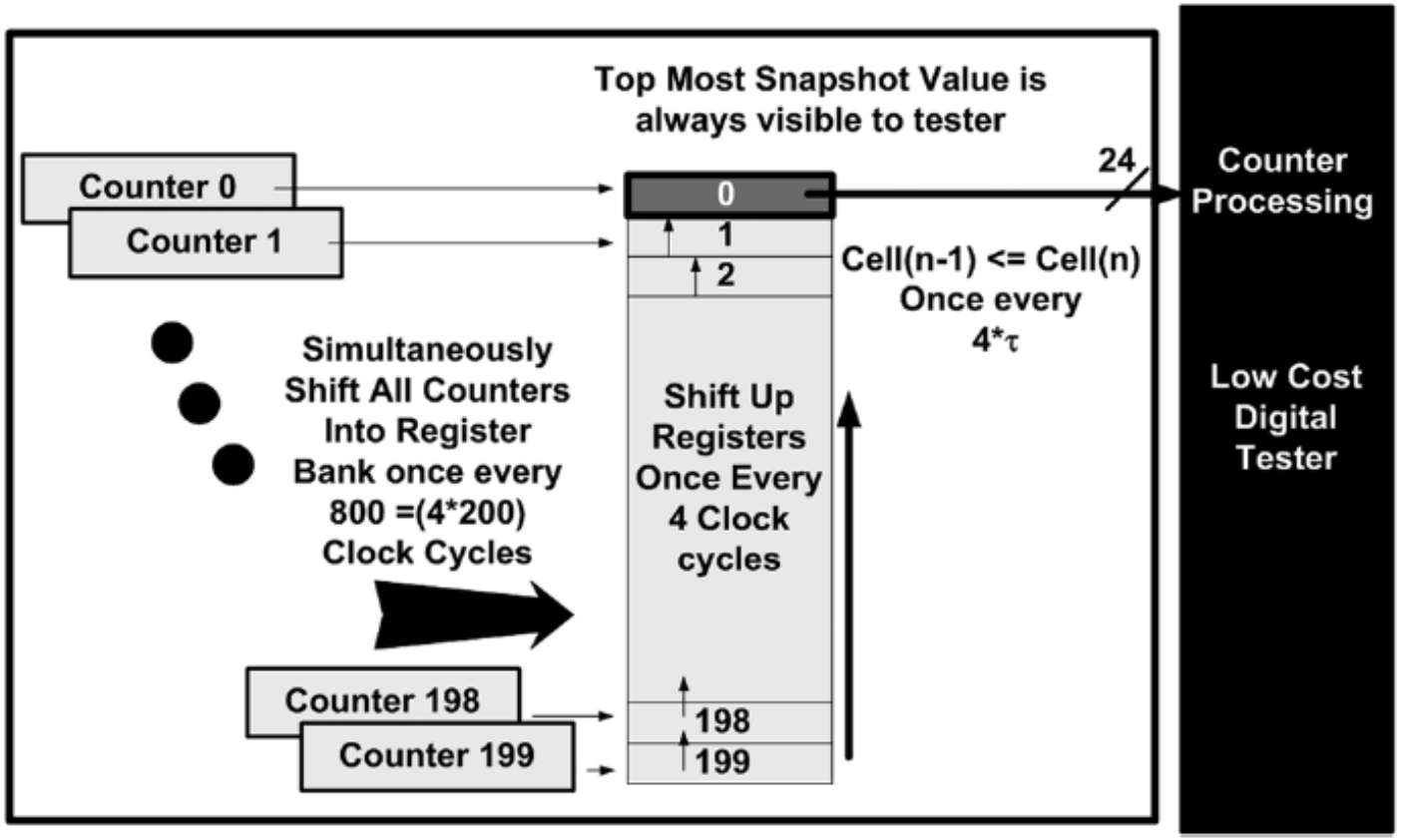


Source: TRAD

- Evaluate SEE sensitivity of Xilinx 7-Series FPGA
  - Single Event Latch-Up (SEL)
  - Single Event Upset (SEU)
  - Multi-Bit Upset (MBU)
  - Single Event Functional Interrupt (SEFI)
- Maximum used LET:

  60.0 MeV.cm²/mg
- Test Vehicles:
  - Shift Register
  - Block Memory
  - ESA dedicated design

Device Under Test – Independent Counter Array

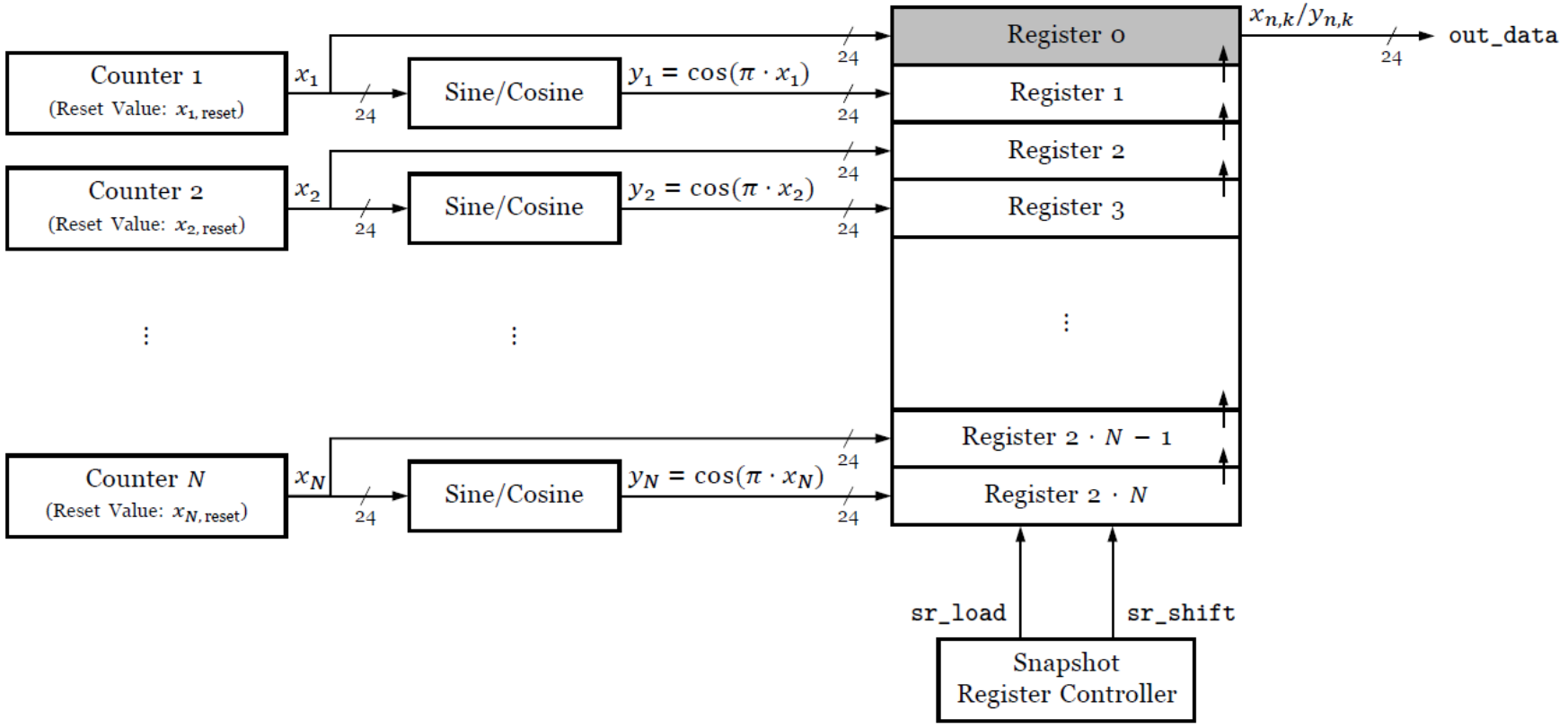


Source: M. Berg

- Design proposed by Melanie Berg, NASA/GSFC
  - "SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA"

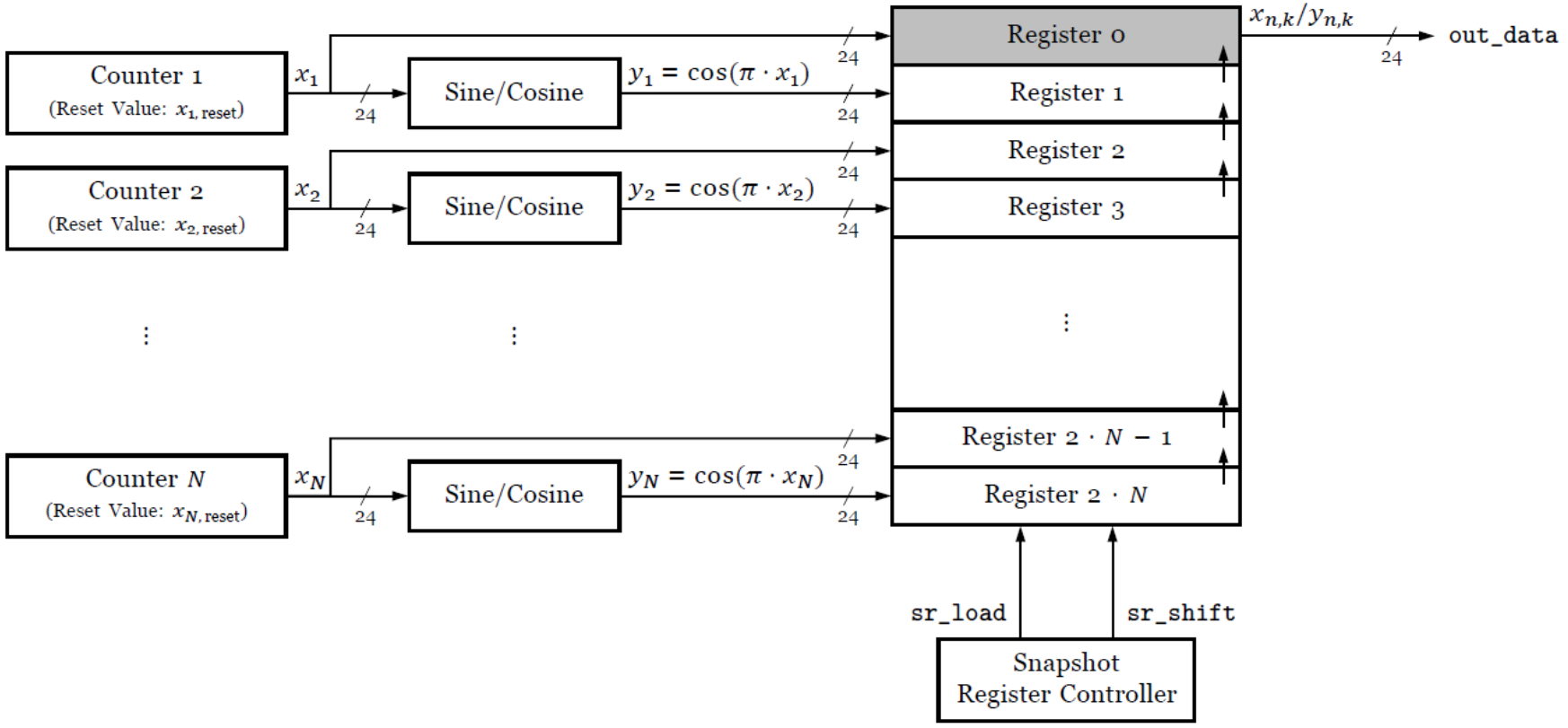
- Aim: increase complexity

Device Under Test – High Level Description



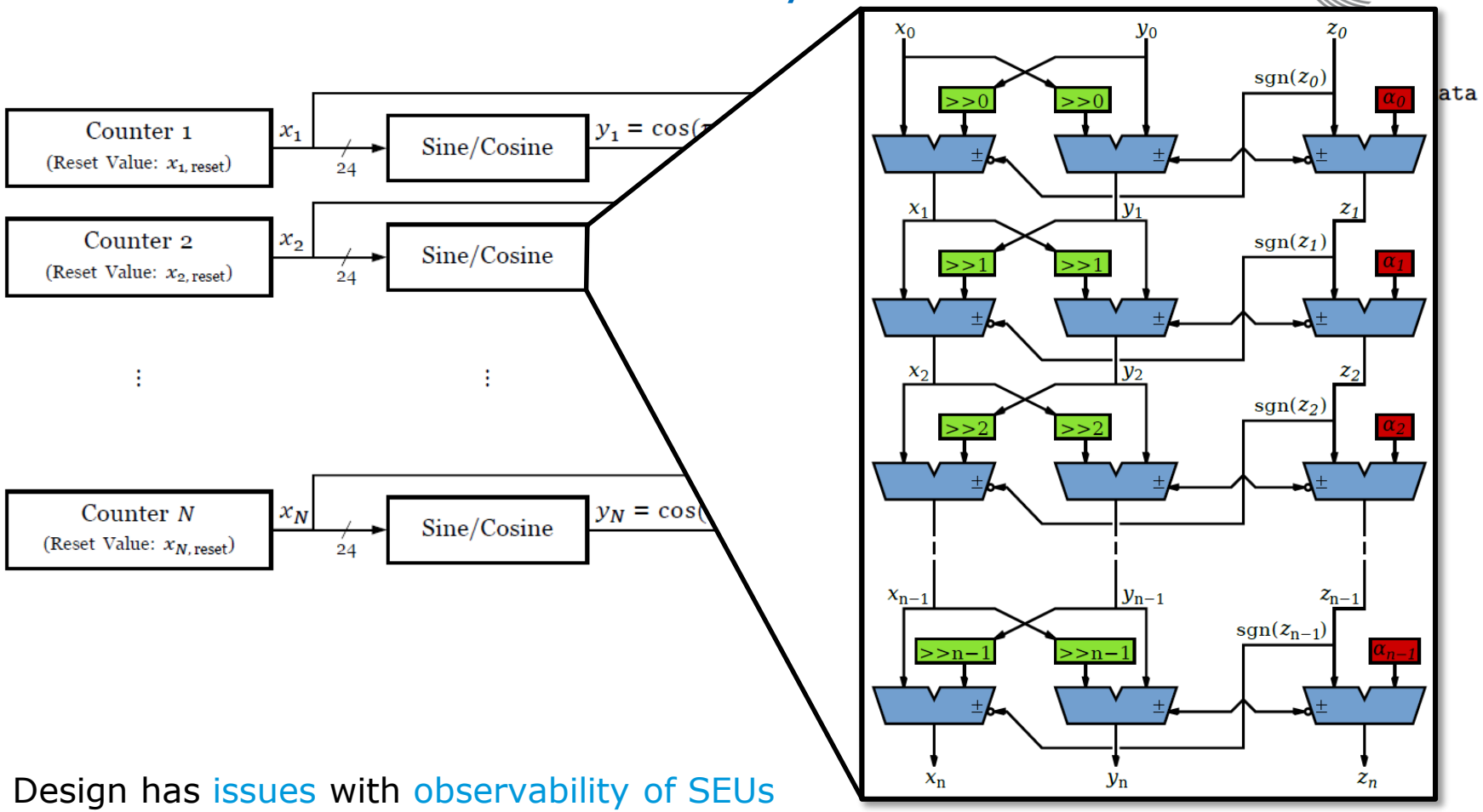
- Extension of Independent Counter Array by adding sine/cosine calculation
- Sine/Cosine calculation is based on CORDIC
- Sine/Cosine can also be calculated by using LUT + multiplication
    - Evaluation of hard-wired multipliers (DSP blocks)

Device Under Test – Observability Issues



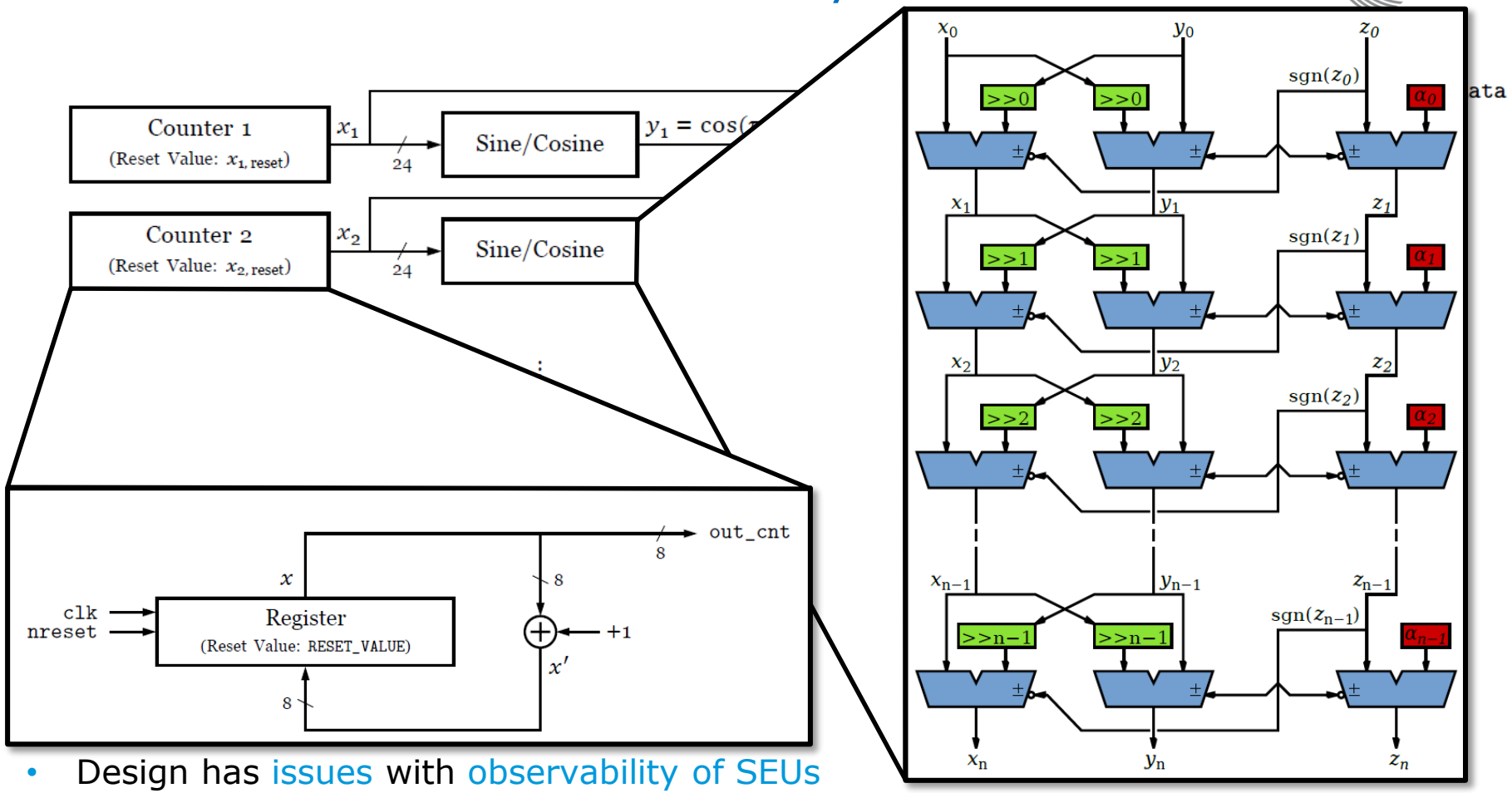
- Design has issues with observability of SEUs
  - SEU in cosine calculation might not be captured by the snapshot register
  - ↪ Not recognized in tester
  - Feedback loop needed
- Step back to original Independent Counter Array

Device Under Test – Observability Issues



- Design has issues with observability of SEUs
  - SEU in cosine calculation might not be captured by the snapshot register
  - ↳ Not recognized in tester
  - Feedback loop needed
- Step back to original Independent Counter Array

Device Under Test – Observability Issues



- Design has issues with observability of SEUs
  - SEU in cosine calculation might not be captured by the snapshot register
  - ↳ Not recognized in tester
  - Feedback loop needed
- Step back to original Independent Counter Array

Summary Test Results

- SEUs, MBUs and SEFIs were observed at minimum LET of 1.83 MeV.cm²/mg

References

1. M. Berg, H. Kim, M. Friendlich, C. Perez, C. Seidleck, K. LaBel and R. Ladbury, “SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices” in IEEE Transaction on Nuclear Science, 2011., pp. 1015–1022, June 2011.

Questions?

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