Memorandum

Reference: TOS-EDD/2004.13/ALRP **Issue:** 1 **Rev.:** 1 **Noordwijk,** 10 March 2004

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To:	Distribution List	
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Subject: **Hardware and Documentation Status of the ATMEL TSC695F Microprocessor (ERC32 Single Chip)**

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1 Scope of the Document

The scope of the present document is to provide the status of both the hardware and the documentation of the TSC695F microprocessor (ERC32 Single Chip) manufactured and commercialised by ATMEL and that is used in ESA projects.

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List of Changes and Additions in the Issue 1 Revision 1

- Addition of the reference to the TSC695F Data Sheet in the Table 1
- Update of the reference to the TSC695F Errata Sheet (new issue of March 2004) in the Table 1

2 Background

The TSC695F is a single chip SPARC V7 32-bit RISC microprocessor that is also known as the ERC32 Single Chip. The TSC695F microprocessor has been developed under the ESA contract 12598/97/NL/FM at the end of the 90's and it is commercialised by ATMEL (formerly MATRA MHS/TEMIC).

The TSC695 microprocessor is the result of the integration on a single chip of the three devices of the ERC32 Chipset (TSC691, TSC692, and TSC693) that were developed under the ESA contract 9848/92/NL/FM at the beginning of the 90's and that was also commercialised by ATMEL and that is now phase out (see the issue 2 of TOS-EDD/2003.22/ALRP for more details about the status of the ERC32 Chipset).

The TSC695F microprocessor is implemented on the 0.5 micron Radiation Tolerant CMOS process of ATMEL.

3 Hardware Status of the TSC695F Microprocessor

3.1 Identification of the Iterations of the TSC695F Microprocessor

During the development phase and the evaluation phase the TSC695 microprocessor has been through several of design revisions in order to correct some deficiencies of the design.

The final iteration of the TSC695 that is presently commercialised by ATMEL is the F iteration.

Although some of the previous E iterations have been in field (and may have been used for some early developments) it is strongly advised to discontinue their use.

3.2 Present Availability of the TSC695F Microprocessor

The TSC695F microprocessor (ERC32 Single Chip) is still presently commercialised by ATMEL.

4 Documentation Status of the TSC695F microprocessor

4.1 Description of the Available Documentation

The present status (2004/03/03) of the documentation for the TSC695F microprocessor is given in the Table 1 below:

Doc Nbr	Title	Issue/Date
1	TSC695F Data Sheet	Rev. 4118H-AERO-06/03
2	TSC695F User's Manual	4148H-AERO-12/03
3	TSC695F Errata Sheet	4280C-AERO-03/04
4	TSC695 Application Note - Trap Generation Under EDAC and Parity Protection - doc4309.pdf	Rev.4309A–AERO–12/03
5	TSC695 Application Note - EDAC Testing Injection of Correctable and Uncorrectable Errors - doc4310.pdf	Rev.4310A–AERO–12/03
6	TSC695 Application Note - Annulled Cycle Management on the TSC695 - doc4326.pdf	Rev. 4326A–AERO–02/04
7	SPARC 7 Instruction Set	Rev. 4168C-AERO-08/01

Table 1

All the above documents are publicly available at the following ATMEL URL address:

http://www.atmel.com/dyn/products/product_card.asp?part_id=2332

It is strongly advised to download the above listed documents and to take knowledge of their contents. The users are also strongly advised to visit regularly the above ATMEL URL address in order to make sure that they have the very last issue of the above listed documents and any new documents that may be published by ATMEL.

Note: With the present layout of the web page corresponding to the above ATMEL URL address make sure to click the link "More App Notes" in order **to display the complete list** of the Application Notes!

I should like particularly to attract your attention on the following documents for which **a new issue has been recently released**: the TSC695F User's Manual and the TSC695F Errata sheet.

4.2 TSC695F Microprocessor ESA Alert

As the result of a detailed review by ESA and ATMEL of the description of the ERC32 handling of the synchronous and the asynchronous faults and the corresponding trap generation it has been found necessary to clarify the description provided in the TSC695F microprocessor User's Manual.

For that purpose ESA has released the following alert:

- **EA-2004-EEE-01-A,**

  Lock-up of the update of the Fault System Register and the Failing Address Register in the ERC32 Chip-set Faults Handling,

with an accompanying technical note:

- **TOS-EDD/2004.1/ALRP, issue 1, revision 2** (09 February 2004)

  Updated Description and Recommendations for the TCS695F Synchronous and Asynchronous Fault Handling and Trap Generation

that clarify the description of the TSC695F microprocessor handling of the synchronous and the asynchronous faults and the corresponding trap generation, and make recommendations in order to guarantee a reliable handling of the TSC695F microprocessor synchronous and asynchronous faults.

The above referenced ESA alert and its accompanying technical note can be found in the ESA Alert System database:

http://www.estec.esa.nl/qq/alerts

Note: **It is required to be registered** to gain access to that database. After completing the registration process you will most likely not be able to gain access immediately to the database, **be patient** and wait for your request to be processed.

> It is strongly recommended to the TSC695F users to download the above identified alert and its accompanying technical note and to take knowledge of their contents in order to be able to write reliable trap handlers.

If you have questions or comments on the above do not hesitate to contact me, see my references below:

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