



Memorandum

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To:	Distribution List	
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Subject: **Hardware and Documentation Status of the ERC32 3-Chipset Microprocessor (ATMEL TSC691, TSC692, and TSC693)**

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1 Scope of the Document

The scope of the present document is to provide the status of both the hardware and the documentation of the ERC32 3-Chipset microprocessor manufactured and commercialised by ATMEL and that are used in several ESA projects.



List of Changes and Additions in the Issue 2 revision 0

- Correction of the erroneous issue and date for the TSC691 Integer Unit User's Manual in the Table 4
- Addition of the reference to the last issue of the ATMEL SPARC 7 Instruction Set description in the Table 4
- Addition of a reference to the ATMEL note on the "Applicability of the TSC695F Application Notes or Errata Sheet to the ERC32 Chipset" in paragraph 4.3
- Addition of a reference to the ESA ALERT **EA-2004-EEE-02-A** "*Lock-up of the update of the Fault System Register and the Failing Address Register in the ERC32 Chip-set Faults Handling*" in paragraph 4.4
- Addition of the list of ESA projects using the various iteration of the ERC32 Chipset in paragraph 5

List of Changes and Additions in the Issue 2 revision 1

- Update of the references for the **new release** of the ATMEL note on the "Applicability of the TSC695F Application Notes or Errata Sheet to the ERC32 Chipset" in 4.3
- Addition in paragraph 4.3 of a warning note about which documents to look at in order to know which "design considerations" and "problems" are applicable to your design

2 Background

The ERC32 3-Chipset microprocessor (ERC32-3CS) is a SPARC V7 32-bit RISC microprocessor. The ERC32-3CS was developed under the ESA contract 9848/92/NL/FM at the beginning of the 90's and was commercialised by ATMEL (formerly MATRA MHS / TEMIC).

The ER32-3CS has been used in several ESA projects such as:

- DMS-R, the main computer of the Russian module of the International Space Station,
- SPC, the main computers of the COLUMBUS module,
- SPLC, the standard payload computers for the space station,
- ERA, the robotic arm computer,
- ATV main computer
- PROBA-1 spacecraft main computer

See the paragraph 5 of this document for more details about the use of the various iterations.



3 Hardware Status of the ERC32 3-Chipset Microprocessor

3.1 Short description of the ERC32 3-Chipset

The ERC32 3-Chipset has been implemented on the 0.8 micron Radiation Tolerant CMOS process of ATMEL.

The ATMEL generic code name for the ERC32-3CS is TSC690E. The chipset is made of the following three devices:

Device Code Name	Description	Short Name
TSC691	Integer Unit	IU
TSC692	Floating Point Unit	FPU
TSC693	Memory Controller	MEC

Table 1

3.2 Identification of the various iterations of the ERC32 3-Chipset devices

During the development phase and the earlier period of commercialisation the ERC32-3CS has been through a certain number of design revisions in order to correct some deficiencies of the design.

The Integer Unit TSC691 has no known design problems and no new iteration has been released during the commercialisation period of the ERC32-3CS. The TSC691 device was commercialised as the iteration C.

The Floating Unit TSC692 has suffered from several design problems and consequently three different iterations have been released during the commercialisation period of the ERC32-3CS. The TSC692 device was successively commercialised as the iterations B, C, and D.

The Memory Controller TSC693 has five known design problems but no new iteration has been released during the commercialisation period of the ERC32-3CS. The TSC693 device was commercialised as the iteration A.

It must be noted that the package marking of the three devices that make the ERC32 3-Chipset does not reflect directly the iteration number of each of the devices as they are identified in the documentation.



The correspondence between the package marking of the three devices of the ERC32-3CS and their iteration numbers is given in the following Table 2:

Device Type	Package Marking	Iteration Number	Number of design considerations
IU	TSC691E	C	0
FPU	TSC692E	B	15
	TSC692F	C	1 (Note 1)
	TSC692G	D	0
MEC	TSC693E	A	5

Table 2

Note 1

This design consideration of the C iteration of the FPU (3.1 in Doc 5 of the Table 4) was left over from the previous B iteration of the FPU (3.15 in Doc 4 of the Table 4) and consequently the design consideration 3.1 of C is identical to the 3.15 of B. This FPU design consideration has been removed in the last D iteration of the FPU. Consequently the last iteration of the FPU is now free of known design considerations

The ERC32-3SC was commercialised successively under the following iteration codes, where the left letter corresponds to the iteration of the IU, the middle letter to the iteration of the FPU, and the right letter to the iteration of the MEC:

ERC32 3-Chipset commercialisation	Package Marking	Iteration Number
1 st	TSC691E, TSC692E , TSC693E	CBA
2 nd	TSC691E, TSC692F , TSC693E	CCA
3 rd	TSC691E, TSC692G , TSC693E	CDA

Table 3

3.3 Present availability of the ERC32 3-Chipset

In March 2002 ATMEL has announced the official phase out of the 0.8 micron Radiation Tolerant ERC32 3Chipset with the last buy on June 28th, 2002 and the last delivery on February 28th, 2003.



4 Documentation Status of the ERC32 3-Chipset Microprocessor

4.1 Description of the Documentation

The documentation of the ERC32-3CS is made of two sets of documents:

- the User's Manuals
- the Design Considerations Lists

The detailed references of these documents are given in the Table 4 below:

Doc Nbr	Title	Issue	Date
1	TSC691E Integer Unit User's Manual	Rev. I	22 Sep. 98
2	TSC692E Floating Point Unit User's Manual	Rev. H	02 Dec. 96
3	TSC693E Memory Controller User's Manual	Rev. D	10 Apr. 97
4	SPARC Radiation Tolerant Processor Chip Set (CBA) Design Considerations List	Rev. E	March 1999
5	SPARC Radiation Tolerant Processor Chip Set (CCA) Design Considerations List	Rev. A	October 1998
6	SPARC Radiation Tolerant Processor Chip Set (CDA) Design Considerations List	Rev. E	March 1999
7	SPARC 7 Instruction Set	Rev. 4168C-AERO-08/01	

Table 4a

NOTE: All the documents that are listed in the above Table 4 have been published by ATMEL (formerly MATRA MHS / TEMIC) and have been checked by ESA with ATMEL (November 2003) to be the last up to date issues that are available.

WARNING

It is strongly recommended to check if you have the last issues of the design considerations lists for the various iterations. In particular some earlier issues of the CBA Design Consideration List may not include the 3.15 design consideration (see Note 1 in 3.2 above) and the description of the 3.14 design consideration may be not up to date.



4.2 Availability of the Documentation

The ATMEL policy about the documentation of the ERC32-3CS is that since the chipset has been phase out (see 3.3) the documentation is not publicly available anymore on their web site.

All the ERC32-3CS documentation that is listed in the Table 4 is available at ESA/ESTEC/TOS-EDD in PDF format and it can be obtained on request by sending me an Email indicating which document(s) you need, your references (your name and the company name), and the ESA project name with which you are involved.

For the persons who are ESA staff it is also possible to access the above identified documents in the ESA TOS-ESD Document Library (estecapps1b/estec/ESA) in the ERC32 folder by double clicking on the following icon:



Notes Link

Note: The TOS-ESD Document Library is only accessible by the ESA staffs that are logged to Lotus Note

4.3 Applicability of the TSC695F Application Notes and Errata Sheets to the ERC32 Chipset

Since the above identified documents are not maintained any more by ATMEL due to the phase out of the ERC32 Chip-set and since there is a strong commonality between the ERC32 Single Chip (TSC695F) and the ERC32 Chip-set, it has been decided in a common agreement between ESA and ATMEL that ATMEL will publish and will maintain a dedicated note that will describe the applicability of all the TSC695F Application Notes and the TSC695F Errata Sheet to the ERC32 Chip-set. The references of that note are provided in the following Table 4b:

Doc Nbr	Title	File	Reference/Date
8	Applicability of TSC695F Application Notes or Errata Sheet to ERC32 Chipset	doc4324.pdf	Rev. 4324C-AERO-03/04

Table 4b

and it can be found at the following ATMEL URL address:

http://www.atmel.com/dyn/products/product_card.asp?part_id=2332

This applicability note is listing all the problems that have been identified on the TSC695F and it identifies the applicability of each individual problem to the ERC32 Chipset.



WARNING

To know all “the design considerations” or “problems” that are applicable to the chipset that is used in a given system you first need to know which chipset iteration that is used (CBA, CCA, or CDA, see the paragraph 3.2 above for more information) and then refer to the following documents:

- The relevant list of design considerations for that chipset iteration: the document 4, 5, or 6 of the Table 4a above
- The “Applicability of TSC695F Application Notes or Errata Sheet to ERC32 Chipset” note (document 8 of the Table 4b above) and find out which one of the listed problems are applicable..

4.4 ERC32 Chipset Alert

As the result of a detailed review by ESA and ATMEL of the description of the ERC32 handling of the synchronous and the asynchronous faults and the corresponding trap generation it has been found necessary to clarify the description provided in the ERC32 Chipset User’s Manuals.

For that purpose ESA has released the alert **EA-2004-EEE-02-A**, *Lock-up of the update of the Fault System Register and the Failing Address Register in the ERC32 Chip-set Faults Handling*, with an accompanying technical note **TOS-EDD/2004.2/ALRP** that clarify the description of the ERC32 Chipset handling of the synchronous and the asynchronous faults and the corresponding trap generation, and make recommendations in order to guarantee a reliable handling of the ERC32 Chip-set synchronous and asynchronous faults.

The above referenced ESA alert and its accompanying technical note can be found in the ESA Alert System database:

<http://www.estec.esa.nl/gg/alerts>

Note that it is required to be registered to gain access to the database.



5 Use of the ERC32 Chip-set in ESA projects

As it is described in 3.2 above, several iterations of the ERC32 Chipset have been commercialised by ATMEL and have been used in the design and the manufacturing of the computer systems of various ESA projects. The following Table 5 summarises to my best knowledge the use of the various ERC32 Chipset iterations in ESA projects:

Project Name	Flights	Flight Spare	EM	Stock
DMS-R	CBA	CBA	CBA	CDA
ATV	CDA	CDA	CDA	CDA
SPC	CBA	-	EM 1to 5: CBA EM 6: CCA	-
ERA	CBA	CBA	CBA	CBA
SPLC	CCA	-	-	-

Table 5

If you have questions or comments do not hesitate to contact me (see my references below).

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