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Memorandum

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From:	A. L. R. Pouponnot	TOS-EDD

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Subject: **Updated Description and Recommendations for the TSC695F Synchronous and Asynchronous Fault Handling and Trap Generation**

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WARNING

The TSC695F User Manual from ATMEL (4148H-AERO-12/03) has precedence over the present document.

European Space Agency
Agence spatiale européenne

ESTEC
Postbus 299 - NL2200 AG Noordwijk - Keplerlaan - NL 2201 AZ Noordwijk ZH -
Tel. (31) 71 565 3685 - Fax (31) 71 565 4295 - Email: Andre-Louis.Pouponnot@esa.int

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List of changes in the issue 1 revision 3

The text of the bullet 3 and the text of the bullet 5 of the paragraph 5 have been updated to match exactly the figure 1. The end statement of the paragraph 5, and the recommendations in the paragraph 6 are left unchanged.

1 Scope of the Document

The purpose of this document is to provide a synthetic description of the TSC695F handling of the synchronous and the asynchronous faults and the trap generation and to make recommendations in order to guarantee a reliable handling of the TSC695F synchronous and asynchronous faults.

2 Reference Document

REF1: TSC695F
SPARC 32-bit Space Processor
User Manual
ATMEL
4148H-AERO-12/03

3 Background

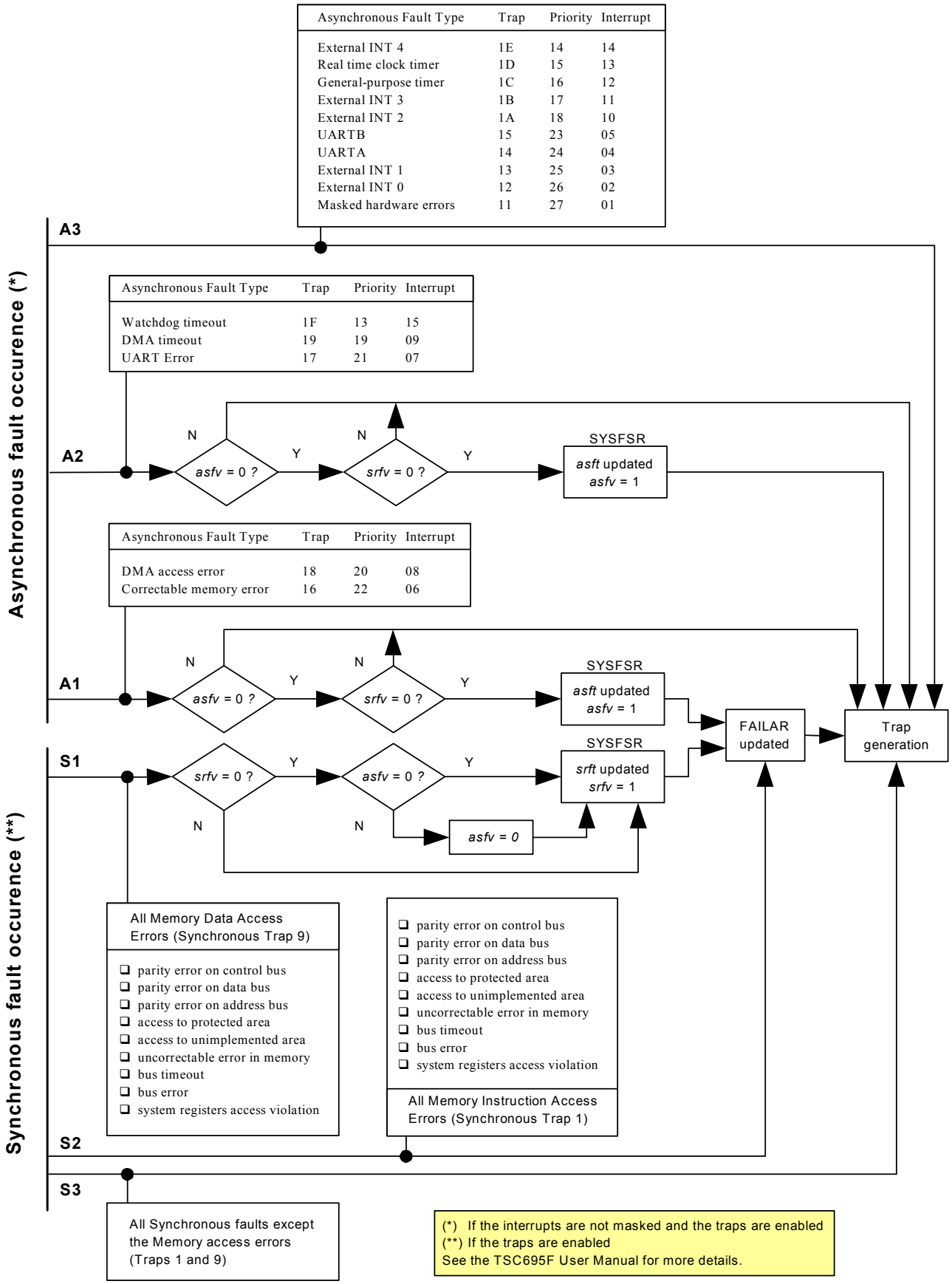
As the result of the detailed review by ESA and ATMEL of the description of the handling of the synchronous and the asynchronous faults and the corresponding trap generation that was provided in a earlier issue of the ATMEL TSC695F User Guide, that later document has been updated as the TSC695F User Manual (REF1) that is now available since 2003/12/18 on the ATMEL web site (www.atmel.com).

4 Description of the TSC695 Handling of the Faults and the Trap Generation

The following Figure 1 presents a synthetic description of the handling of the synchronous and the asynchronous faults and the corresponding trap generation by the TSC695F. The figure is derived from the original Figure 4-2 of the ATMEL TSC695 User Manual (REF1) and it has been complemented to cover all the possible cases. Such augmented diagram allows to get quickly an accurate and a complete overview of how the TSC695F is handling the synchronous and the asynchronous faults and the corresponding trap generation.

Figure 1

TSC695F Diagram for all Synchronous and Asynchronous Faults and Trap Generation



5 Analysis of the TSC695 Handling of the Faults and the Trap Generation

From the previous Figure 1 the following remarks and conclusions can be derived:

***Note**: In the following text the class fault codes make reference to the classes that are identified on the left side of the previous Figure 1.*

- All synchronous and asynchronous faults will generate a trap *but not all of them will update* the System Fault Status Register (SYSFSR) and the Failing Address Register (FAILAR) of the TSC695F

- The faults of the class A3 and the class S3 *never update* the SYSFSR and the FAILAR

- The faults of the class A2 (traps 17, 19, 1F) *will only update* the SYSFSR, *but*:

  - If there was a previous class A1 or A2 faults the SYSFSR *will not be updated*
  - If there was no previous class A1 or A2 faults but there was a previous S1 class faults (trap 9) the SYSFSR *will not be updated*

- The faults of the class S2 (Trap 1) *will always update* the FAILAR *only*

- The faults of the class A1 (traps 16 and 18) *will update both* the SYSFSR and the FAILAR *but*:

  - If there was a previous class A1 or A2 faults the SYSFSR and the FAILAR *will not be updated*
  - If there was no previous class A1 or A2 faults but there was a previous S1 class faults (trap 9) the SYSFSR and the FAILAR *will not be updated*

- The faults of the class S1 (data access, Trap 9) *will always update both* the SYSFSR and the FAILAR independently of the previous class of traps.

Consequently for the A1 and the A2 cases it can be seen that the update of the SYSFSR and the FAILAR can be blocked either by a previous class A1 or A2 faults, or a by previous S1 class faults that will have set the *asfv* or the *srfv* bits to *one* in the SYSFSR.

6 Recommendations

To guarantee the update of the SYSFSR and the FAILAR in all possible fault sequences it is necessary to clear the relevant *asfv* and the *srfv* bits of the SYSFSR. Since the individual clearing of the *asfv* and the *srfv* bits of the SYSFSR is not possible it is necessary to reset the SYSFSR by writing any value to it. The reset value of the SYSFSR is 0x00000078 that corresponds to all the fields being cleared to the *zero* value except for the *srft* field that is set to all *one's* (reset value for the synchronous fault type).

Consequently, in order to guarantee the update of the SYSFSR and the FAILAR in all possible fault sequences, it is recommended to reset the SYSFSR on the exit of the following trap handlers:

9, 16, 17, 18, 19, and 1F.

The TSC695F User Manual from ATMEL (REF1) has been updated to cover the related issues of the handling of the synchronous and the asynchronous faults and the trap generation and it is now available since 2003/12/18 on the ATMEL web site (www.atmel.com). All users of the TCS695F are strongly advised to download the new issue of the TSC695F User Manual and to take knowledge of its new contents. Note that the description of the handling of the synchronous and the asynchronous faults and the corresponding trap generation have been updated in the paragraph 3.6.7 (update of the text, update of the Table 3-4, new Tables 3-5 and 3-6), in text following the Table 4-13, and in the Figure 4-2.