BUILDING BLOCKS FOR SYSTEM ON A CHIP

COO1 : DEVELOPMENT AND INDUSTRIALIZATION OF AN ERC32 VME INTERFACE (EVI32)

EVI32 VMEbus Interface (EVI32)

DATA SHEET

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1. INTRODUCTION

1.1 SCOPE

This document describes the VMEbus Interface EVI32 device.

The EVI32 device is a VME circuit designed to interface the following components :

- TSC695E Single Chip Sparc Processor from ATMEL. [AD6]
- TSC691E/TSC692E/TSC693E Triple Chip Sparc Processor from ATMEL [AD1] [AD2] [AD3]
- TSC21020E DSP associated with the DPC ASIC Companion Chip [AD7] [AD8] [AD9]

This document is divided in the following sections :

- Introduction
- Data Sheet of EVI32 for ERC32 Interface
- Data Sheet of EVI32 for DSP/DPC Interface
- Mechanical Interface and Packaging.

1.2 APPLICABLE DOCUMENTS

AD1 TSC691E: SPARC RT Integer Unit User's Manual, Rev. H, Temic Semiconductors (F), 1996

AD2 TSC692E: SPARC RT Floating Point Unit User's Manual, Rev. H, Temic Semiconductors (F), 1996

AD3 TSC693E: SPARC RT Memory Controller MEC Rev. A, Device Specification, MCD/SPC/0009/SE Issue 4, Saab Ericsson Space (S), 1997

AD4 IEEE Standard for a versatile backplane bus: VMEbus, IEEE 1014-1987

AD5 VMEbus Specification Manual, Rev. C, VMEbus Manufacturers Group, 1985

AD6 Rad-Hard 32 bit SPARC Embedded Processor TSC695E TEMIC – Rev. 003 January 2000

AD7 Spec du DSP TEMIC – Rev. 003 January 2000

AD8 Spec du DPC TEMIC – Rev. 003 January 2000

AD9 Spec du McM TEMIC – Rev. 003 January 2000

Note that AD1, AD2 and AD3 can be obtained via the World Wide Web (WWW) from the ERC32 home page at http://www.estec.esa.nl/wsmwww/erc32. The home page contains also additional documents and information regarding ERC32.

1.3 DEFINITION :

Even parity : The number of bits equal to one including the parity bit is even.

1.4 NOTATION :

The bit 0 is the least significant bit.

1.5 ABBREVIATIONS

AD	Applicable Document
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read Only Memory
ERC32	32-bit Embedded Real-time Computing core indicates both ERC32/SC and ERC32/3C components
ERC32/3C	Triple Chip Version of the ATMEL Sparc Processor TSC691E/TSC692E/TSC693E
ERC32/SC	Single Chip Version of the ATMEL Sparc Processor TSC695E
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
EVI32	ERC32 VMEbus Interface
FPU	Floating Point Unit, for ERC32
IEEE	Institute of Electrical and Electronics Engineers
ID	Identification
I/O	Input/Output
IU	Integer Unit, for ERC32
MEC	Memory Controller, for ERC32
ROAK	Release On Acknowledge
RORA	Release On Register Access
SEL	Single Event Latch-up
SEU	Single Event Upset
SGL	Single level
SRAM	Static Random Access Memory
WWW	World Wide Web

2. FUNCTIONAL DESCRIPTION AND CHARACTERISTICS FOR ERC INTERFACE

2.1 INTRODUCTION

This section presents the EVI32 interface to ERC32/SC and ERC32/3C. The description is mainly focused on the ERC32/SC interface. Compatibility with ERC32/3C which is the older version of the ATMEL microprocessor is given after.

2.2 GENERAL DESCRIPTION

The EVI32 device fully adheres to the IEEE 1014-1987 VMEbus standard (AD4), and is compatible with the commercial VMEbus specification (AD5). EVI32 can act as a system controller and provides both master and slave interfaces.

EVI32 implements the following functions:

- A32/A24/D32/D16/D8 master interface;
- A24/D32/D16/D8 slave interface;
- Interrupt handler;
- Interrupter;
- Single level arbiter (SGL);
- VME bus timer;
- Optimised D16 interface;
- Four mailboxes for multi-processor communication;
- Minimised usage of external buffers;
- On-chip error-detection.

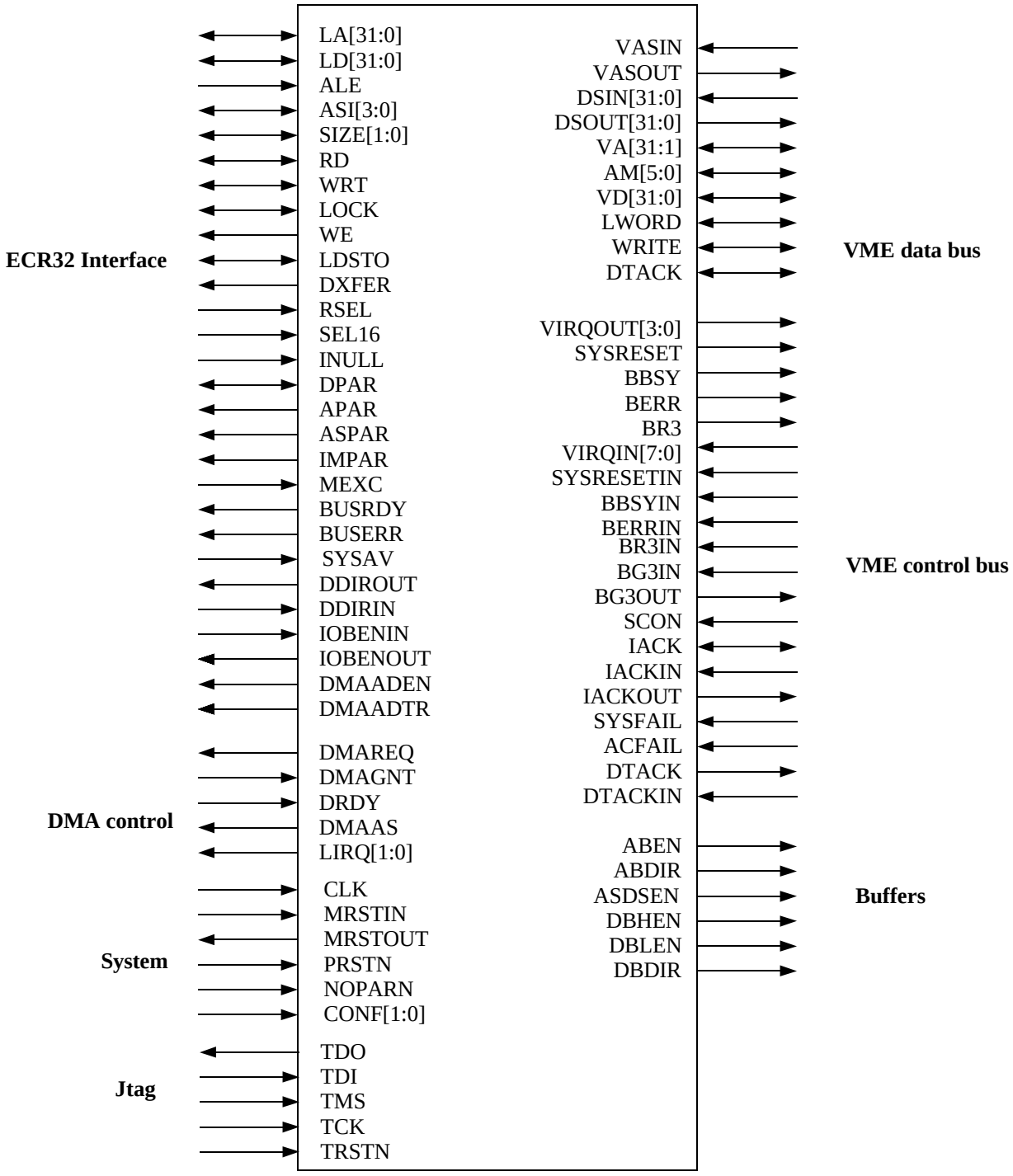


Figure 2.2-1 : EVI32 pin definition

2.2.1 EVI32/ERC32 interface

The EVI32 interfaces directly to the address, data and control bus of the ERC32, requiring no external components. The EVI32 control registers are accessed by asserting RSEL and are typically mapped to one of the ERC32 I/O areas. The VME bus is mapped to the ERC32 extended general area. During slave cycles, the controller performs DMA cycles to and from the ERC32 memory. If EVI32 is connected to a 16 bit VME data bus (D16), 32-bit and 64-bit ERC32 accesses can be transformed to multiple 16-bit transfers.

2.2.2 VME interface

The EVI32 provides signals for the VME control bus, address bus and data bus. These signals do not have adequate driving strength to drive the VME bus directly and therefore need external buffers. Depending on the width of the address and data bus of the attached VME bus, 6 to 11 external buffers are required.

2.2.3 Master cycles

Master cycles are generated by read and write accesses to the extended general area. The ERC32 ASI bits are used to generate the desired VME address modifier. During 8- and 16- bit accesses, the EVI32 performs byte swapping to align ERC32 and VME data. An ERC32 double access (64-bit) will generate two 32-bit accesses.

2.2.4 Slave cycles

During slave accesses, the EVI32 will perform DMA cycles to the ERC32 memory. Both 8-, 16- and 32-bit accesses can be performed. Block access are allowed for all slave accesses. The internal slave select generator is used to select which VME address the controller will respond to.

2.2.5 Mailboxes

Four mailboxes are provided for inter-processor communication. The mailboxes consist of a 16-bit register mapped in the short VME address space. An interrupt can be generated upon reading or writing the mailbox.

2.2.6 Interrupt handler and interrupter

The interrupt handler can handle any of the seven VME interrupts. A VME interrupt will generate a local ERC32 interrupt. VME Interrupt acknowledge cycles are performed by ERC32 by reading the interrupt ID of the interrupting device.

Commanded by the ERC32, the interrupter can generate four VME interrupts. The interrupt ID can be individually programmed for all four interrupts.

2.3 FUNCTIONAL DESCRIPTION

2.3.1 ERC32/SC - EVI32 schematic

Figure 2.3-1 shows how EVI32 should be connected to ERC32/SC, Figure 2.3-2 shows how EVI32 should be connected to ERC32/3C, and Figure 2.3-3 gives the interconnection of EVI32 to VME bus. An option is given in this figure. According to VME standard the AS*, DS1* and DS0* signals shall be driven by tristate buffers. EVI32 allows the use of open collector buffers as drawn, in order to reduce buffer count. But the correctness of the use of open collector buffers with regards to the VME standard is under the responsibility of the user.

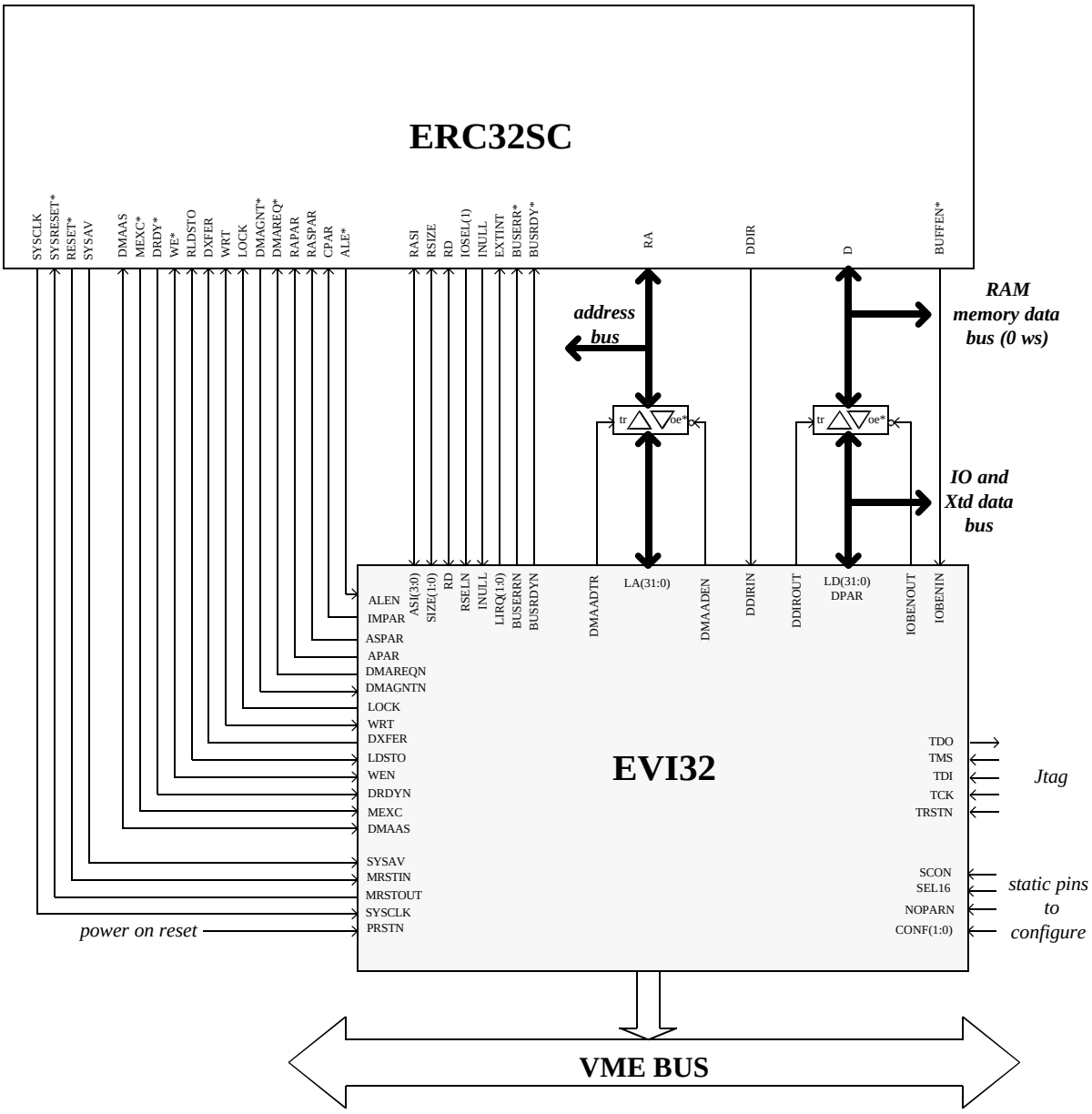


Figure 2.3-1 – ERC/SC - EVI interface drawing

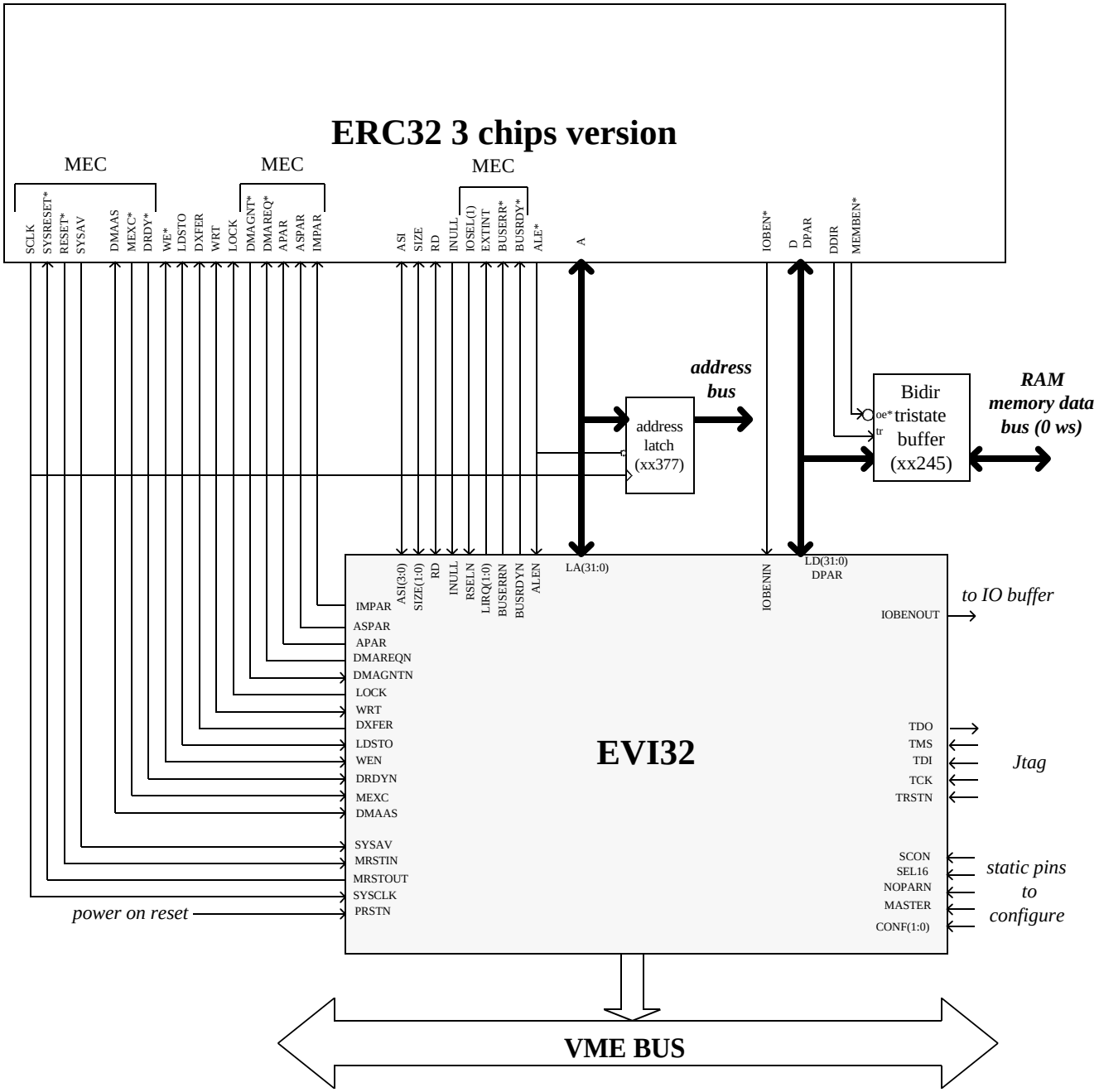


Figure 2.3-2 – ERC/3C - EVI interface drawing

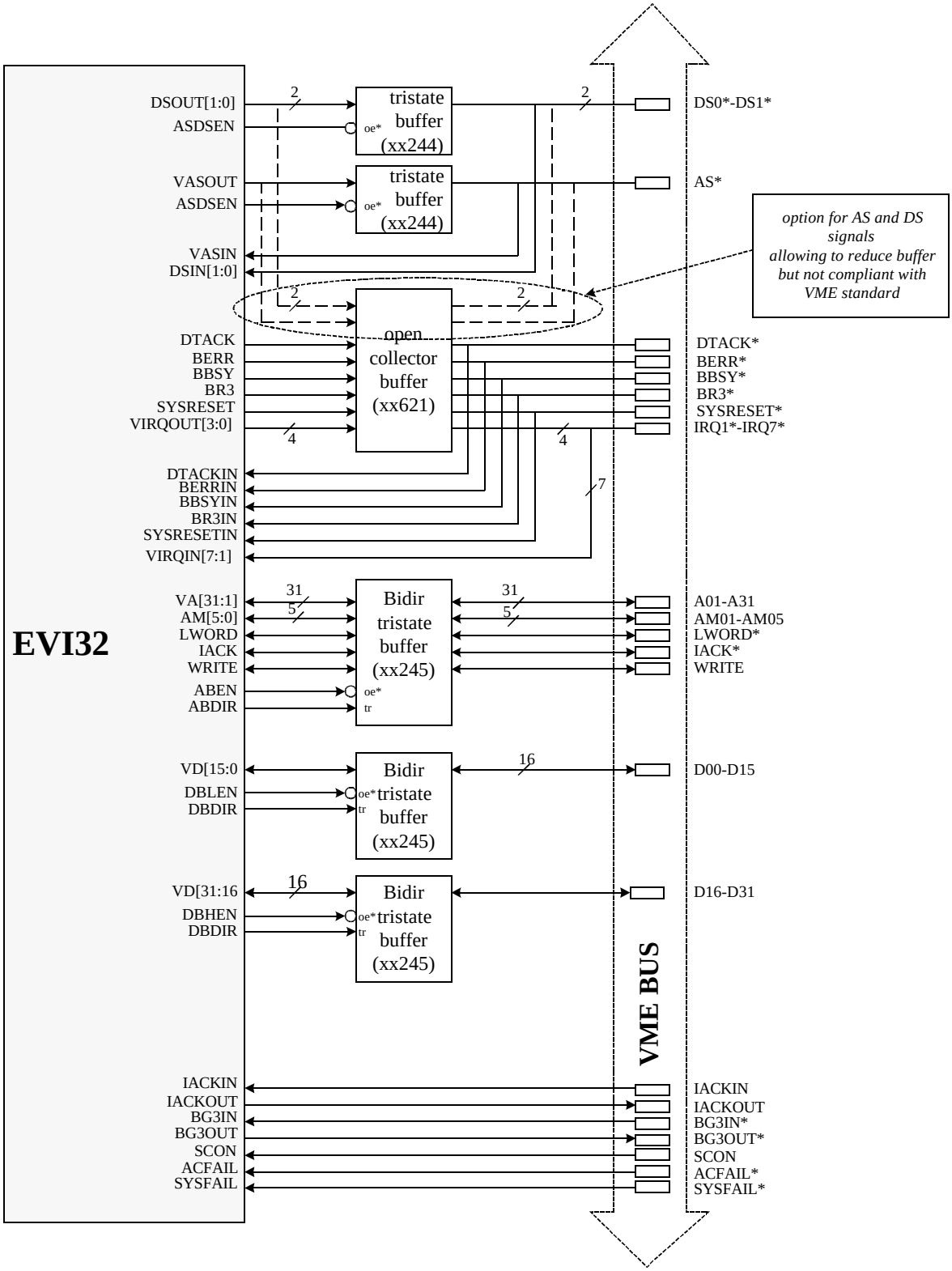


Figure 2.3-3 – EVI32 interface to the VME bus

2.3.2 EVI32 registers

2.3.2.1 General

EVI32 provides 14 internal registers to control the operation. The registers are accessed by asserting RSEL. RSEL should be connected to any of the four I/O select signals on the MEC. The registers can be read with any data size but only written with store word (32 bit wide).

2.3.2.2 Register address map

Table 2-1 shows the EVI32 registers and their corresponding address.

Register	Function	Access	Address
MSTREG	Master control register	Read/Write	0x00
SLVREG	Slave control register	Read/Write	0x04
SLAREG	Slave address register	Read/Write	0x08
ICREG	Interrupt configuration register	Read/Write	0x0C
IDREG0	Interrupt identification register	Read/Write	0x10
CMDREG	Interrupt command register	Write only	0x14
ISTREG	Interrupt status register	Read	0x18
MBCREG	Mailbox control register	Read/Write	0x1C
MB0REG	Mailbox 0 register	Read/Write	0x20
MB1REG	Mailbox 1 register	Read/Write	0x24
MB2REG	Mailbox 2 register	Read/Write	0x28
MB3REG	Mailbox 3 register	Read/Write	0x2C
SSTREG	System status register	Read/Write	0x30
SRREG	System reset register	Read/Write	0x34

Table 2-1 : EVI32 registers

2.3.3 Master interface

2.3.3.1 Operation

A VME cycle is started when an access is performed to the decoded part of the extended general area as defined in the master configuration register. The master interface supports one-, two and four-byte transfers as defined in Table 2-2. Unaligned VME master cycles cannot be generated by ERC32 and are not supported. An ERC32 load (store) double cycle will generate two consecutive quad byte transfers on the VME bus. The VME bus will not be released between the cycles**.** If a VME cycle fails due to BUSERR being asserted, MEXC will be generated at the end of the ERC32 cycle. The error cause will be indicated in the system status register.

ERC32 cycle	VME cycle
load byte	read byte
store byte	write byte
load halfword	read double byte
store halfword	write double byte
load word	read quad byte
store word	write quad byte
load double	read quad byte (twice)
store double	write quad byte (twice)
load-store byte	read-modify-write byte
swap	read-modify-write quad word

Table 2-2 ERC32 versus VME cycles

The fields IOS[4:0] and MVA[7:0] in the master configuration register control show how ERC32 addresses are mapped on VME addresses. The VME bus is mapped on the ERC32 extended general area starting at address 0x80000000. The IOS field indicates how much of the extended general area is used. The VME address is generated from the ERC32 address and the MVA field. The MVA field contains the most significant part of the VME address which is not derived from the ERC32 address. The decoded I/O area can be from 16M (IOS=000) to 2G (IOS=111), programmable in binary steps. Table 2-3 shows the use of the MVA field in relation to the IOS field.

IOS	Used bits in MVA	Used I/O area
000	7:0	16 M
001	7:1	32 M
010	7:2	64 M
011	7:3	128 M
100	7:4	256 M
101	7:5	512 M
110	7:6	1024 M
111	7	2048 M

Table 2-3 Extended general area mapping

The VME address modifier (AM) is derived from the ERC32 address space identifier (ASI). Table 2-4 shows the mapping between the ERC32 ASI codes and the VME address modifier during master access. Two user-defined AM codes can be used as defined in the master configuration register.

ASI[3:0]	AM[5:0]	VME Cycle type
0x0	0x29	short non-privileged access
0x1	0x2D	short supervisory access
0x2	0x3F	interrupt acknowledge cycle
0x3	AM0	user defined
0x4	AM1	user defined
0x8	0x3A	standard non-privileged program access
0x9	0x3E	standard supervisory program access
0xA	0x39	standard non-privileged data access
0xB	0x3D	standard supervisory data access
0xC	0x0A	extended non-privileged program access
0xD	0x0E	extended supervisory program access
0xE	0x09	extended non-privileged data access
0xF	0x0D	extended supervisory data access

Table 2-4 Master ASI versus AM mapping

2.3.3.2 D16 access

The EVI32 includes accelerated D16 access. This is done by converting single or double ERC32 access to multiple double byte VME accesses. This feature is enabled in two ways; if the D16 bit is set in the master configuration register then all single and double ERC32 accesses are converted to D16 VME accesses. If D16 is not set, then the SEL16 input has to be asserted when accelerated D16 access is required. SEL16 can be connected to an unused ASI signal or to an address signal. The accelerated D16 accesses are not possible for quad-byte read-modify-write cycles (ERC32 swap instruction) or interrupt acknowledge cycles.

2.3.3.3 Block transfer

VME bus block transfers will be performed if the BT bit is set in the master control register and an ERC32 cycle would result in more than one VME cycle. As an example, a double load ERC32 access will result in a block transfer of two quad-bytes if the BT bit is set, or four double-bytes if accelerated D16 access is set. Block transfer will only be performed when the ERC32 ASI is set to 0x8 - 0xF (standard and extended address access)**.**

2.3.3.4 ERC32 bus time-out control

An ERC32 access to an I/O area will be aborted by the MEC if BUSREADY have not been generated within 255 clocks after the start of the access. To avoid aborting a VME transaction due to MEC time-out, the master interface includes a time-out counter.

The time-out counter will terminate the ERC32 VME access by generating BUSERR if:

- Timeout 1 : the VME bus have not been granted to the master interface. Enabling and duration of Timeout 1 is controlled by ET12 and ETD bits of the Master Configuration Register.
- Timeout 2 : he VME bus have been granted but the previous slave did not released the bus. . Enabling and duration of Timeout 2 is controlled by ET12 and ETD bits of the Master Configuration Register.
- Timeout 3 : the addressed slave did not respond within 248 clocks. . Enabling and duration of Timeout 3 is controlled by ET3 and ETD bits of the Master Configuration Register.

If the VME access is aborted due to the last case, the VME BERR signal will also be asserted.

In addition, the EVI32 contains a VME timer that starts when VASIN is activated and that stops counting when VASIN is released. Its duration and enabling is controlled by the VT bit of the Master Configuration Register.

2.3.3.5 Master control register

The master configuration register controls the master interface. The register is set to 00000000H during reset.

31	30	29	28 27	26	25	24	23	22 17	16 11	10 8	7 0
ETD	ET3	ET12	VT[1:0]	RR	ME	D16	BT	AA0[5:0]	AA1[5:0]	IOS[2:0]	MVA[7:0]

ETD : Timeout 1 2 and 3 duration

	Timeout 1	Timeout 2	Timeout 3
ETS = 0	128	160	248
ETS = 1	512	640	992

ET3 : Enable Timeout 3

ET12 : Enable Timeout 1 and Timeout 2

VT : VME Timer Duration :

00 disabled, 01 : 256 clock cycles, 10 : 512 clock cycles, 11 : 1024 clock cycles

RR : Release bus on request

ME : Master interface enable

D16 : Accelerated D16 access enable

BT : Block transfer enable

AA1 : Alternative AM codes

AA0 : Alternative AM codes

IOS : I/O area size

MVA : Most significant part of VME address

Table 2-5 Master configuration register

2.3.4 Slave interface

2.3.4.1 Operation

The slave interface provides access to the ERC32 local memory from an external VME master. The slave address is programmed in the EVI32 slave configuration register. The following cycle types are supported:

VME cycle
address only (no action)
read single, double & quad byte
read single, double & quad byte block
write single, double & quad byte
write single, double & quad byte block
read-modify-write single, double &quad byte
read & write unaligned

Table 2-6 Supported slave cycles

On single and double byte write accesses, the slave interface will perform a read-modify-write cycle to the ERC32 since the DMA interface only allows 32-bit accesses.

Slave decoding is done using the slave address (SA) field in the slave address register and the slave size fields (ESZ & SSZ) in the slave configuration register. During standard address (A24) accesses, SA[6:0] is compared to bit [23:17] of the VME address. If equal, the slave is selected. The size field (SSZ) defines how many of the bits (starting from the left-most bit) shall be compared. In this way, the size of the slave is between 128k and 16M, and mappable anywhere in the VME A24 address space on an aligned block boundary. The extended area (A32) is decoded in the same way but using SA[14:0] and VME address bits [31:17]. The most significant part of the local address is generated in similar fashion and taken from the LMA field in the slave address register. The mapped VME area can thereby be mapped on any block aligned address in the full ERC32 address space.

If a master access selects its own slave area, the cycle is terminated with a bus error (BUSERR) and the error type is indicated in the system status register. Likewise, if a slave access is done to the part of the extended general area which is used for master VME access, the VME access will be terminated with a bus error (BERR). The ST, EX, SV, NP, PE and DE bits in the slave configuration register defines which address modifiers the slave will respond to. Table 2-7 shows how the ASI is generated for different address modifiers.

If the keep bus bit (KB) in the slave configuration register is set, then the ERC32 DMA request will be kept during a whole block transfer and during a complete read-modify-write cycle. If KB is not set, the local bus will be released to ERC32 between each bus access. The KB bit increases the transfer rate but halts the ERC32 for a longer time.

ASI[3:0]	AM[5:0]	VME slave access type	ERC32 cycle type
0x8	0x3A, 0x0A	non-privileged program access	user program access
0x9	0x3E, 0x0E	privileged program access	supervisor program access
0xA	0x39, 0x3B	0x09, 0x0B	non-privileged data access
user data access	0xB	0x3F, 0x3D	0x0F, 0x0D
privileged data access	supervisor data access		

Table 2-7 Slave Access ASI versus AM mapping

2.3.4.2 Slave configuration register

The slave configuration register defines the operation of the slave interface. The register is set to 00000000H during reset.

15	14	13	12	11	10	9	8	7	6 4	3 0
KB	SE	NP	PE	SV	BE	EX	ST	DE	SSZ[2:0]	ESZ[3:0]

ESZ : decoded slave area size for extended addressing
SSZ : decoded slave area size for standard addressing
DE : data access enable
ST : enable standard address decoding
EX : enable extended address decoding
BE : block transfer enable
SV : enable supervisor access
PE : program access enable
NP : enable non-privileged access
SE : slave enable
KB : keep bus during block and RMW cycles

ESZ	A32 size	see Note 1	SSZ	A24 size	see Note 1
0000	128 k	15	000	128 k	7
0001	256 k	14	001	256 k	6
0010	512 k	13	010	512 k	5
0011	1 M	12	011	1 M	4
0100	2 M	11	100	2 M	3
0101	4 M	10	101	4 M	2
0110	8 M	9	110	8 M	1
0111	16 M	8	111	16 M	0
1000	32 M	7			
1001	64 M	6			
1010	128 M	5			
1011	256 M	4			
1100	512 M	3			
1101	1 G	2			
1110	2 G	1			
1111	4 G	0			

Table 2-8 Slave configuration register

Note1 : Number of bits compared between SA field and address to decide if slave is selected.

2.3.4.3 Slave address register

The slave address register defines the address selection and generation of the slave interface. The register is set to 00000000H during reset.

29 15	14 0
LMA[14:0]	SA[14:0]

SA : slave address
LMA : local address (most significant part)

Table 2-9 Slave address register

2.3.5 Mailboxes and VME status register

2.3.5.1 General

The four mailboxes provide a mean for inter-processor communication over the VME bus. Each mailbox consist of a 16- bit register mapped into the short VME address space (A16). The mailbox registers can be accessed with A16/D8/D16 transfers. The mailbox configuration register controls the operation of the mailboxes. The mailbox address field (MBA) defines at which address the mailboxes appear in address space, aligned at 256-byte blocks. The SU and NP bits enable supervisor (AM = 0x2D) and non-privileged (AM=0x29) access. Interrupts can optionally be generated to the local processor when the individual mailboxes are read or written. The RI field enables interrupt generation after the mailbox has been read while the WI field enables interrupt generation after write. Pending mailbox interrupts can be read from the Interrupt status register. A mailbox interrupt is cleared when the local processor reads or writes the corresponding mailbox register.

17	16	15 8	7 4	3 0
NP	SU	MBA[7:0]	WI[3:0]	RI[3:0]

RIn : enable read access interrupt for mailbox n
WIn : enable write access interrupt for mailbox n
MBA : mailbox start address(256-byte block)
SU : enable supervisor access (1M=0x2D)
NP : enable non-privileged access (AM=0x29

A16 address	Register
0000	Mailbox 0
0002	Mailbox 1
0004	Mailbox 2
0006	Mailbox 3
0008	System Status

Table 2-10 Mailbox configuration register

2.3.5.2 VME status register

The VME status register is readable from the VME bus and contains two status bits from the local ERC32 system. It is mapped at address 0x8 (A16/D8/D16) directly after mailbox register 3.

1	0
MR	SA

SA : ERC32 SYSAV pin

MR : MRSTIN pin

Table 2-11 System Reset register

2.3.6 Interrupt handling

2.3.6.1 Interrupt controller

The EVI32 contains an interrupt controller that generates two local interrupts to the ERC32, LIRQ0 and LIRQ1. The two local interrupts are generated by the interrupt controller from 13 internal sources. Table7 shows the interrupt allocation. The two local interrupts are asserted as long as any pending interrupts are present, the corresponding MEC interrupts should therefore be programmed level-sensitive for correct operation.

Interrupt #	Interrupt source
13	ACFAIL
12	Mailbox 3
11	Mailbox 2
10	VME interrupt 7
9	VME interrupt 6
8	VME interrupt 5
7	VME interrupt 4
6	SYSFAIL
5	Mailbox 1
4	Mailbox 0
3	VME interrupt 3
2	VME interrupt 2
1	VME interrupt 1

Table 2-12 Interrupt numbering

The interrupt level for each interrupt is programmed in the interrupt configuration register.

25 13	12 0
IL[13:1]	IE[13:1]

IEn : interrupt enable for interrupt n (0=disabled, 1= enabled)
ILn : interrupt enable for interrupt n (0=level 0, 1= level 1)

Table 2-13 Interrupt configuration register

The status of pending interrupts can be read from the interrupt status register.

24 21	20 17	16 13	12 0
PGI[3:0]	MI1[3:0]	MOI[3:0]	PI[13:1]

PIn : pending interrupt n
MI0 : highest priority pending interrupt in level 0
MI1 : highest priority pending interrupt in level 1
PGIn : pending generated VME interrupt n – bit 21 corresponds to irq#1, bit 22 to irq#2…

Table 2-14 Interrupt status register

2.3.6.2 VME interrupt handler

The VME interrupt handler can handle all seven VME interrupts. The handling of a VME interrupt is enabled by enabling the corresponding bit in the interrupt configuration register. When an interrupt is detected, the corresponding interrupt pending bit is set in the interrupt status register and a local interrupt is generated to the ERC32. To acknowledge the VME interrupt, an interrupt acknowledge cycle needs to be performed to read the interrupter's STATUS/ID. This is done by doing a read cycle with ASI equal to 0x2 to an arbitrary location in the VME area. The read value contains the STATUS/ID of the interrupter that generated the interrupt. During the interrupt acknowledge cycle, address bits 4 - 2 of the local address bus are used to generate bits 3 - 1 of the VME address and are use to identify which interrupt is being acknowledged. The following sequence shows how a VME interrupt is handled:

- A VME interrupt is generated by asserting VIRQOUT.
- A local ERC32 interrupt is generated by asserting LIRQ.
- ERC32 takes an interrupt trap, disabling further interrupts (at this level).
- The ERC32 interrupt routine reads the EVI32 status register to identify the pending interrupt.
- The ERC32 interrupt routine generates a VME interrupt acknowledge cycle by reading the VME area with ASI=0x02. At this point, any VME ROAK interrupts will de-assert VIRQOUT.
- The ERC32 interrupt routine will read the interrupting device's register. At this point, any RORA interrupts will de-assert VIRQOUT.

It should be noted that for RORA interrupts, the interrupt service routine must allow at least 2 ms between the last step above and re-enabling of the corresponding MEC interrupt (VME specification rule

4.8).

A D08 interrupt acknowledge cycle must be performed with the least significant bit (A0) of the ERC32 address equal to one, since D08 interrupters respond only to DS(0).

If the VME acknowledge cycle is terminated with a bus error (BERR asserted), then the ERC32 load cycle will be terminated with BUSERR asserted.

2.3.6.3 VME interrupter

The interrupter is capable of generating four VME interrupts. Interrupts are generated by writing to the Interrupt command register. Monitoring of generated interrupts is done through the interrupt status register. The VME STATUS/ID for each of the generated interrupts is programmed in the Interrupt identification register and is 7 bits long for VME interrupts 2 - 7, and 8 bits for VME interrupt 1. The VME interrupt number a generated interrupt is mapped on is defined by the interrupt select (IS) bits in the interrupt identification register. Pending generated interrupts (not yet acknowledged) can be cleared by writing to the interrupt command register. When a generated interrupt is acknowledged through a VME interrupt acknowledge cycle, the interrupter responds with the STATUS/ID, clears the pending bit and releases the interrupt line. This corresponds to a VME ROAK interrupter.

The interrupter will only respond to an interrupt acknowledge cycle when a generated interrupt is pending for that interrupt. The interrupter will respond to D8/D16/D32 acknowledge cycles, but only provide the least significant 7/8 bits. The remaining data bits will be high, as specified in the VME specification (AD4).

2.3.6.4 Interrupter identification register

The interrupt identification registers contains the STATUS/ ID value for each generated interrupt. The registers are set to 00000000H during reset.

31	30 24	23	22 16	15	14 8	7 0
IS3	ID3[6:0]	IS2	ID2[6:0]	IS1	ID1[6:0]	ID0[7:0]

ID0[6:0] : STATUS/ID code for generated interrupt 0 (VME irq# 1)
ID1[6:0] : STATUS/ID code for generated interrupt 1 (VME irq# 2/3)
ID2[6:0] : STATUS/ID code for generated interrupt 2 (VME irq# 4/5)
ID3[6:0] : STATUS/ID code for generated interrupt 3 (VME irq# 6/7)
ISn : Isn = 0 generate even VME interrupt, else odd

Table 2-15 Interrupt identification register

2.3.6.5 Interrupt command register

The interrupt generate register is write-only register used to generate and clear interrupts.

9	8	7 4	3 0
CS	CA	CI[3:0]	GI[3:0]

GIn : generate interrupt Idn
CIn : clear pending generated interrupt IDn
CA : clear ACFAIL interrupt
CS : clear SYSFAIL interrupt

Table 2-16 Interrupt command register

2.3.7 System status register

The system status register indicates the bus error cause and the status of some VME signals. A write to this register will only affect the RBE, SBE and MBE fields.

16 15	14	13 11	10	9	8	7	6 0
RBE	SBE	MBE[2:0]	SC	0	AC	SF	VIRQ[7:1]

VIRQn : complemented value of VME IRQn signal
AC : complemented value of ACFAIl signal
SF : complemented value of SYSFAIL signal
SC : value of SCON signal
MBE : bus error related to master access (ERC32 or VME) see table below
SBE : Slave bus error : VME access to own slave area
RBE : bus error caused by register access see table below

MBE[2:0]	Master Bus error cause
000	No error
001	VME bus grant not received (time-out 1)
010	Unused
011	Unused
100	VME bus time-out (slave did not release bus Timeout 3)
101	VME access terminated with BUSERR
110	Unused
111	Unused
RBE[1:0]	Register Bus error cause
00	No error
01	Wrong write in register (size error)
10	Access to non-existing EVI32 register
11	Both previous errors

Table 2-17 EVI32 status register

2.3.8 VME system controller functions

The arbiter, bus timer and IACK daisy-chain driver are only enabled if EVI32 acts as a system controller (when the SCON input is asserted).

2.3.8.1 Arbiter

The arbiter is a single level (SGL) arbiter as defined in the VME specification. To improve latency, bus parking can be enabled by setting the RR bit in the master configuration register, which will keep BBSY asserted between consecutive accesses until there is a bus request from another master.

2.3.8.2 Bus timer

A VME bus timer is provided in the EVI32. It consists of an 8-bit counter clocked by the system clock. The timer is reset and started when VASIN is asserted, indicating a bus access. If DTACK is not asserted before the counter reaches 248, BERR is asserted, indicating a bus error. During block transfers, the counter is reset after each DTACK.

2.3.8.3 IACK daisy-chain driver

The IACK daisy-chain driver generates a falling edge on the IACKOUT output when any interrupt handler on the VME bus acknowledges an interrupt.

2.3.9 Reset operation

2.3.9.1 General

EVI32 has three reset inputs; power-on reset (PRSTN), MEC reset (MRSTIN) and VME reset (SYSRESETIN). Two reset outputs are provided, one for the MEC (MRSTOUT) and one for the VME bus (SYSRESET).

EVI32 is internally reset when any of the following conditions are true:

- the MRSTIN input is asserted and the MRSTOUT output is not asserted;

- the PRSTN input is asserted;
- the SYSRESETIN input is asserted while the SR bit in the system reset register has the value zero (see section 2.3.9.2);
- the ER bit in the system reset register is set to the value 1 (in this case, neither SYSRESET nor MRTSOUT is asserted). This can for example be used after a hardware error has been detected, or similar.

During the internal EVI32 reset, all registers are cleared to their default zero values and all outputs (except the MRSTOUT output) are placed in their inactive state.

The MRSTOUT output is asserted on any of the following conditions:

- the PRSTN input is asserted;
- the SYSRESETIN input is asserted while the SR bit in the system reset register has the value 0 (see section 2.3.9.2).

The VME SYSRESET output is asserted on any of the following conditions:

- the PRSTN input is asserted;
- SR bit in the system reset register is set to the value 1 while the SCON input is being asserted;

If the VME SYSRESET is generated by setting the SR bit in the system reset register, the minimum assertion time of 200ms for the SYSRESET signal (as per AD4) must be controlled via software.

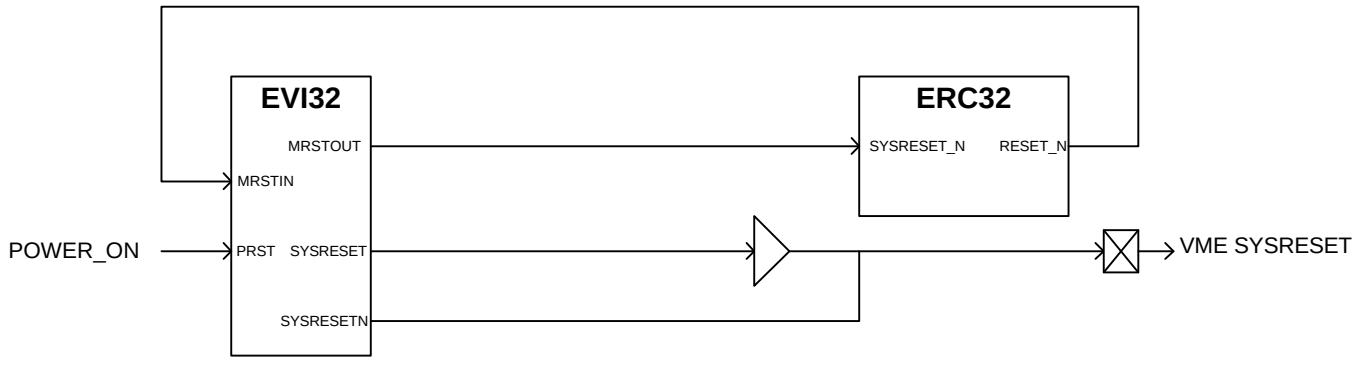


Figure 2.3-4 Reset Management

2.3.9.2 System reset register

The system reset register is used to either generate VME SYSRESET or to reset EVI32. The PO bit can be written with any value, but will only be reset when PRSTN is asserted. PO hit is not cleared in case of reset generated by setting ER bit at 1.

2	1	0
PO	ER	SR

SR : generate VME SYSRESET (see section 2.3.9.1)

ER : reset EVI32 (see section 2.3.9.1)

PO : cleared on power-on-reset

Table 2-18 VME status register

2.3.9.3 Register reset values

All EVI32 registers are cleared to `all zeros' during reset.

2.3.10 Error detection

The EVI32 uses SEU hardened D flip-flop internally. Thus no parity protection is provided on internal registers.

When NOPARN input is unasserted, EVI32 shall generate the following signals :

- APAR odd parity over the LA[31:0] address bus
- ASPAR odd parity over the ASI[3:0] and SIZE[1:0) signals
- IMPAR odd parity over the LDSTO, DXFER, LOCK, WRT, RD, and WEN signals
- DPAR odd parity over the LD[31:0] data bus in case of write access of EVI32 on the local bus.

APAR, ASPAR, and IMPAR are only generated during a DMA access performed by EVI, otherwise they are tristated.

EVI never checks the parity on incoming data on the LD data bus. In case of error detected by ERC32, MEXC signal is raised, and the VME access is terminated by BUSERR.

2.4 EVI32 SIGNAL DESCRIPTION

2.4.1 EVI32 signal summary

The EVI32 device shall have 32 input signals, 34 output signals, 146 bidirectional signals, as specified in Table 2-19, Table 2-20, Table 2-21 and Table 2-22. Together with 27 power pins as specified in Table 2-23, this gives a total pin count of 239 (TBC).

Name	Type	Function	Active polarity
ALE	Input	Address latch enable	Low
ASI[3:0]	Bidir	IU address space identifier	High
APAR	Tristate output	Address parity	High
ASPAR	Tristate output	ASI and Size parity	High
BUSERR	Output	Bus error	Low
BUSRDY	Output	Bus ready	Low
CLK	Input	MEC SYSCLK	High
CONF[1:0]	Input	EVI32 configuration	
DDIRIN	Input	I/O buffer direction input	High
DDIROUT	Output	I/O buffer direction output	High
DPAR	Bidir	Data bus parity	High
DMAADEN	Output	AD Buffer Enable	Low
DMAADTR	Output	AD Buffer Direction	High
DMAAS	Tristate output	DMA address strobe	High
DMAGNT	Input	DMA bus grant	Low
DMAREQ	Output	DMA bus request	Low
DRDY	Input	DMA data ready	Low
DXFER	Tristate output	Data transfer strobe	High
IMPAR	Tristate output	Control signals parity	High
INULL	Input	Integer unit nullify	High
IOBENIN	Input	I/O buffer enable input	Low
IOBENOUT	Output	I/O buffer enable output	Low

Table 2-19 ERC32 interface

Name	Type	Function	Active polarity
LA[31:0]	Bidir	Address bus	High
LD[31:0]	Bidir	Data bus	High
LDSTO	Bidir	Load/store strobe	High
LIRQ[1:0]	Output	Local interrupt	Low
LOCK	Tristate output	Locked access	Low
MEXC	Input	Memory exception	Low
MRSTIN	Input	Reset input (connect to MEC RESET)	Low
MRSTOUT	Output	Reset output (connect to MEC SYSRESET)	Low
NOPAR	Input	Disable parity generation	Low
PRSTN	Input	Power-on reset	Low
RD	Bidir	Read strobe	High
RSEL	Input	EVI32 register select	Low
SEL16	Input	Enable accelerated 16 bit access	High
SIZE[1:0]	Bidir	SIZE indicator	High
SYSAV	Input	System available	High
TDO	Tristate output	JTAG TDO pin	High
TDI	Input	JTAG TDI pin	High
TMS	Input	JTAG TMS pin	High
TCK	Input	JTAG TCK pin	High
TRSTN	Input	JTAG TRSTN pin	low
WRT	Bidir	Early write strobe	High
WE	Tristate output	Write strobe	Low

Table 2-20 ERC32 interface (con't)

Name	Type	Function	Active polarity
ACFAIL	Input	Power failure	Low
AM[5:0]	Bidir	Address modifier	High
BBSY	Output	Bus busy	Low
BBSYIN	Input	Bus busy	Low
BERR	Output	Bus error	Low
BERRIN	Input	Bus error	Low
BG3IN	Input	Bus grant in	Low
BG3OUT	Output	Bus grant out	Low
BR3	Output	Bus request	Low
BR3IN	Input	Bus request	Low
DSIN[1:0]	Input	Data strobes	Low
DSOUT[1:0]	Output	Data strobes	Low
DTACK	Output	Data acknowledge	Low
DTACKIN	Input	Data acknowledge	Low
IACK	Bidir	Interrupt acknowledge	Low
IACKIN	Input	Interrupt ack in	Low
IACKOUT	Output	Interrupt ack out	Low
LWORD	Bidir	Long word	Low
SCON	Input	System controller	Low
SYSFAIL	Input	System failure	Low
SYSRESET	Output	System reset	Low
SYSRESETIN	Input	System reset	Low
VA[31:1]	Bidir	Address bus	High
VASIN	Input	Address stable	Low
VASOUT	Output	Address stable	Low
VD[31:0]	Bidir	Data bus	High
VIRQIN[7:1]	Input	Interrupts	Low
VIRQOUT[3:0]	Output	Interrupts	Low
WRITE	Bidir	Write strobe	Low

Table 2-21 VME interface

Name	Type	Function	Active polarity
ABEN	Output	VME address buffer enable	Low
ABDIR	Output	VME address buffer direction	Low
ASDSEN	Output	VME AS DS buffer enable	Low
DBLEN	Output	VME data buffer enable (low 16 bits)	Low
DBHEN	Output	VME data buffer enable (high 16 bits)	Low
DBDIR	Output	VME data buffer direction	Low

Table 2-22:VME Buffer control

Name	Function		
VCC[10:0]	Power input		
GND[15:0]	Ground		

Table 2-23: Power pins

2.4.2 EVI32 detailed signal description

2.4.2.1 Clock , reset and configuration signals

CLK (input) – System Clock

This pin shall be connected to SYSCLK of the ERC32. It is the master clock of the EVI32.

PRSTN (input) – Power-on reset

Reset input activated at power up.

CONF[1:0] (input) – Configuration of EVI32

CONF pins are used to program EVI32 for ERCSC, ERC 3 chips, DSP/DPC configuration.

Configuration	CONF[1]	CONF[0]
ERC32 SC	1	1
ERC32 3C	1	0
DSP DPC	0	1
Reserved for Test Mode	0	0

A wrong configuration may damage the chip.

MRSTIN (input) – Reset input

This pin shall be connected to the RESET* output of the ERC32.

MRSTOUT (output) – Reset output

This pin shall be connected to the SYSRESET* input of the ERC32/SC.

NOPARN - No Parity (input)

This pin shall be connected to the NOPAR* input of the ERC32. Assertion of this signal will disable the parity checking of all signals related to the ERC32 local buses. This is a static signal and shall not change when running.

SEL16 – Enable accelerated 16 bit access (input)

This configuration pin enables accelerated 16 bit accesses on the VME bus.

SCON – System Controller Enable (input)

This configuration pin configures the EVI32 in System Controller for the VME bus.

SYSAV - System Availability (input)

This pin shall be connected to the SYSAV output of the ERC32/SC. This signal is asserted whenever the system is available.

2.4.2.2 ERC32/SC interface

ALEN - Address Latch Enable (input)

This signal is used to latch the RD input in ERC32/SC mode. In ERC32/3C mode it is used also to latch the Address provided by the IU.

ASI[3:0] - Address Space Identifier (bi-directional)

These pins shall be connected to the RASI signals of the ERC32/SC (or to the ASI signals of the ERC32/3C).These four bits constitute the Address Space Identifier (ASI), which identifies the memory address space to which the memory access is being directed. The ASI bits are latched by the EVI32 and are used to detect supervisor mode, instruction or data access, etc. In case of DMA this signal must be driven by the EVI32.

APAR - Address Bus Parity (tristate output)

This pin shall be connected to the RAPAR signal of the ERC32/SC (or to the APAR signals of the ERC32/3C). This signal is the odd parity over the AL[31:0] signal. In case of Direct Memory Access this signal must be driven by the EVI32 in case DMA parity is enabled.

ASPAR - ASI and SIZE Parity (tristate output)

This pin shall be connected to the RASPAR signal of the ERC32/SC (or to the ASPAR signals of the ERC32/3C). This signal is the odd parity over the ASI[3:0] and the SIZE[1:0] signals. In case of Direct Memory Access this signal must be driven by the EVI32 in case DMA parity is enabled

BUSERRN - Bus Error (output)

This pin shall be connected to the BUSERR* signal of the ERC32. BUSERRN is to be generated together with BUSRDYN by the EVI32 if an error is detected during an access.

BUSRDYN - Bus Ready (output)

This pin shall be connected to the BUSRDY* signal of the ERC32. BUSRDYN is to be generated by the EVI32 during an exchange, since it is connected to the ERC32 extended general area.

DMAADEN – Address Buffer Enable (output)

This signal is used only for ERC32/SC configuration. This signal shall be connected to the Enable input of the bidirectional buffer controlling the Address bus. In non-DMA mode, DMAADEN is always active and low. It is inactive (high) only when DMAADTR is switching.

DMAATR – Address Buffer Direction (output)

This signal is used only for ERC32/SC configuration. This signal shall be connected to the Direction input of the bidirectional buffer controlling the Address bus. In non-DMA mode, DMAADTR is always low, since address are provided by ERC32/SC. In DMA mode DMAADTR is activated.

DDIRIN - IO Buffer Direction In (input)

This signal is used only for ERC32/SC configuration. This signal shall be connected to the DDIR signal of the ERC32/SC.

DDIROUT - IO Buffer Direction Out (output)

This signal is used only for ERC32/SC configuration. This signal shall be connected to the Direction input of the bidirectional buffer controlling the data bus. In non-DMA mode, DDIROUT is the copy of DDIRIN. In DMA mode, polarity is changed to allow DMA access from ERC32/SC.

DPAR - Data Bus Parity (bi-directional)

This pin shall be connected to the DPAR signal of the ERC32. This signal is the odd parity over the DL[31:0] signals. This signal is checked by EVI32 when the DL data bus is read, and generated by the EVI32 when EVI32 drives the DL data bus if parity generation is enabled.

IMPAR – Control Signal Parity (tristate output)

This pin shall be connected to the CPAR signal of the ERC32. This signal is the odd parity over the LDSTO, DXFER, LOCK, WRT, RD, and WE* signals. In case of Direct Memory Access this signal must be driven by the EVI32 in case DMA parity is enabled

INULL - Integer Unit Nullify Cycle (input)

This pin shall be connected to the INULL signal of the ERC32. INULL is output from the IU to indicate that the current memory access is nullified.

IOBENIN - IO Buffer Enable In (input)

This signal shall be connected to the BUFFEN* signal of the ERC32/SC or this signal shall be connected to the IOBEN* signal of the ERC32/3C.

IOBENOUT - IO Buffer Enable Out (output)

In the ERC32/SC configuration, this signal shall be connected to the Enable input of the bidirectional buffer controlling the data bus. In non-DMA mode, IOBENOUT is the copy of IOBENIN. In DMA mode, polarity is changed to allow DMA access from ERC32/SC.

In the ERC32/3C configuration, this signal is used to enable the data buffers for other than EVI32 I/O and exchange memory.

LA[31:0] - Address Bus (bi-directional)

These pins shall be connected to the address bus RA of the ERC32/SC SC (or to the A bus of the ERC32/3C). The address bus is generated by the ERC32/SC in normal mode. In DMA mode this bus must be driven by the EVI32.

LD[31:0] - Data Bus (bi-directional)

These pins shall be connected to the data bus of the ERC32. These pins form a 32-bit bi-directional data bus that serves as the interface between the ERC32 and the EVI32. It is driven by the EVI32 only during read of its internal registers and when making read accesses on the VME bus. In case of Direct Memory Access, it is driven or read by EVI32.

LIRQ[1:0] – Local Interrupt Request(output)

These pins shall be connected to the EXTINT signals of the ERC32. These 2 signals are two local interrupts to the ERC32/SC.

LOCK -Bus Lock (output)

This pin shall be connected to the LOCK signal of the ERC32. LOCK is asserted by the processor when it needs to retain control of the bus (address and data) for multiple cycle transactions (Load Double, Store Single and Double, Atomic Load-Store). The bus will not be granted to another bus master as long as LOCK is asserted. Note that BHOLD* should not be asserted in the processor clock cycle which follows a cycle in which LOCK is asserted. EVI32 must supply this signal during a DMA session.

RD - Read Access (bi-directional)

This pin shall be connected to the RD signal of the ERC32. RD is used in conjunction with SIZE[1:0], ASI[3:0] and LDSTO to determine the type of transfer and to check the write access rights of bus transactions. EVI32 must supply this signal during a DMA session, deasserted low for write and asserted high for read accesses.

RSELN – Register Select (input)

This input is used to enable read or write in the EVI32 internal registers. It is connected to on of the IOSEL*(x) signals generated by the ERC32.

SIZE[1:0] - Bus Transaction Size (bi-directional)

These pins shall be connected to the RSIZE signals of the ERC32/SC (or to the SIZE bus of the ERC32/3C). The coding on these pins specifies for the EVI32 the size of the data being transferred during a memory access. In case of DMA, the EVI32 must drive these bits to '10', since only word transfers are allowed in DMA mode.

The following signals of the ERC32 interface of the EVI32 are only used when DMA mode is activated.

DMAAS - DMA Address Strobe (tristate output)

This pin shall be connected to the DMAAS signal of the ERC32. During DMA transfers (when the EVI32 is bus master) this output is used to inform the CPU that the address from the DMA is valid and that the access cycle shall start. DMAAS can be asserted multiple times during DMA grant.

DMAGNTN - DMA Grant (input)

This pin shall be connected to the DMAGNT* signal of the ERC32. DMAGNT* is generated by the MEC as a response to a DMAREQN.

DMAREQN - DMA Request (output)

This pin shall be connected to the DMAREQ* signal of the ERC32. DMAREQN is to be issued by the EVI32 when requesting the access to the processor bus as a master.

DRDYN - Data Ready during DMA access (input)

This pin shall be connected to the DRDY* signal of the ERC32. During DMA read transfers (when the EVI32 is bus master) this output is used to inform the EVI32 that the data are valid. During DMA write transfers this signal indicates that data have been written into memory.

DXFER - Data Transfer (tristate output)

This pin shall be connected to the DXFER signal of the ERC32. DXFER is used to differentiate between the addresses being sent out for instruction fetches and the addresses of data fetches. DXFER is asserted by the processor during the address cycles of all bus data transfer cycles, including both cycles of store single and all three cycles of store double and atomic load-store. EVI32 unit must supply this signal during a DMA session.

LDSTO - Atomic Load-Store (bidirectional)

This pin shall be connected to the LDSTO signal of the ERC32. This signal is used to identify an atomic load-store to the system and is asserted by the integer unit during all the data cycles (the load cycle and both store cycles) of atomic load-store instructions. EVI32 must supply this signal during a DMA session.

MEXC – Memory Exception (input)

This pin shall be connected to the MEXC* signal of the ERC32. This signal is used indicate a memory exception during a DMA transfer.

WEN - Write Enable (tristate output)

This pin shall be connected to the WE* signal of the ERC32. EVI32 must supply this signal during a DMA session, asserted low for write and deasserted high for read accesses. WEN is asserted by EVI32 during the cycle in which the store data is on the databus. For a store single instruction, this is during the second store address cycle; the second and third store address cycles of store double instructions, and the third load-store address cycle of atomic load-store instructions.

WRT - Advanced Write (bidirectional)

This pin shall be connected to the WRT signal of the ERC32. WRT is an early write signal, asserted by the processor during the first store address cycle of integer single or double store instructions, the first store address cycle of floating-point single or double store instructions, and the second load-store address cycle of atomic load-store instructions. WRT is sent out unlatched. EVI32 must supply this signal during a DMA session, deasserted low for read and asserted high for write accesses.

2.4.2.3 VME signal interface

ABEN - VME address buffer enable (Output)

This signal shall be connected to the enable pin of the bidirectional buffer driving the VME address bus.

ABDIR - VME address buffer direction (Output)

This signal shall be connected to the direction pin of the bidirectional buffer driving the VME address bus.

ACFAIL – AC failure (input)

This signal that indicated when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.

AM[5:0] – Address Modifier (bi-directional)

Signals that are used to broadcast information such as address size, cycle type, or master identification or a combination of these.

ASDSEN - VME AS DS buffer enable (output)

This signal shall be connected to the enable pin of the bidirectional buffer driving the VME AS and the DS signals.

BBSYIN – Bus Busy (input)

BBSY – Bus Busy (output)

A signal that indicates that the master is using the Data Transfer Bus.

BERRIN – Bus Error (input)

BERR – Bus Error (output)

A signal generated by the bus timer function or the slave function. This signal indicates to the master that the data transfer was not completed.

BG3IN – Bus Grant (Input)

The BG3IN and BG3OUT signals are part of the bus grant daisy chain. The BG3IN signal indicates to the EVI32 receiving it that it has been granted the Data Transfer Bus.

BG3OUT – Bus Grant Out (Output)

The BG3OUT signal indicated to the next board in the daisy chain that it may use the Data Transfer Bus.

BR3IN – Bus Request Number 3 (Input)

BR3 – Bus Request Number 3 (Ouput)

This signal is generated by an interrupter in case of Interrupt Request.

DBLEN - VME data buffer enable Low (Output)

This signal shall be connected to the enable pin of the bidirectional buffer driving the 16 LSB bits of the VME data bus.

DBHEN - VME data buffer High Enable (Output)

This signal shall be connected to the enable pin of the bidirectional buffer driving the 16 MSB bits of the VME data bus.

DBDIR - VME data buffer direction (Output)

This signal shall be connected to the enable pin of the bidirectional buffer driving the VME data bus.

DSIN[1:0] – Data Strobe Zero, One (Input)

DSOUT[1:0] – Data Strobe Zero, One (Output)

The Data Strobe signals are used with LWORD to defined the size of the data exchanged on the VME bus.

DTACKIN - Data Transfer Acknowledge (Input)

DTACK - Data Transfer Acknowledge (Output)

DTACK signal indicates that the addressed slave have successfully completed the exchange.

IACKIN - Interrupt Acknowledge In (Input)

IACKOUT - Interrupt Acknowledge Out (Output)

The IACK daisy chain is used during an interrupt acknowledge cycle to determine the interrupter

IACK - Interrupt Acknowledge (bi-directional)

IACK signal is driven by the interrupt handler during an interrupt acknowledge cycle.

LWORD – Long Word (bi-directional)

LWORD indicates the data size during a VME exchange in association with DSIN[1:0].

SYSFAIL – System Failure (input)

A signal that indicated when a system failure on the VME bus.

SYSRESETIN – System reset (input)

SYSRESET – System reset (output)

SYSRESET manages the Reset on the VME bus.

VA[31:0] – Address Bus (bi-directional)

Address lines that are used to broadcast a short, standard, or extended address.

VASIN – Address Strobe (Input)

VASOUT – Address Strobe (Output)

A signal that indicates when a valid address has been placed on the address bus

VD[31:0] – Data Bus (bi-directional)

Signals used to transfer data between the master and the slaves, and status/ID from interrupters to interrupt handlers.

VIRQIN[7:1] – Interrupts (Input)

VIRQOUT[3:0] – Interrupts (Outputs)

Interrupt signals are activated by the interrupt requester, and are handled by interrupt handlers.

WRITE (bi-directional)

WRITE signal when activated indicates a write exchange on the VME bus.

2.5 CHARACTERISTICS

2.5.1 Electrical interfaces

2.5.1.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Vdd	Supply voltage	-0.5	6	V
Vi	Input voltage	-0.5	Vdd + 0.5V	V
Ts	Storage temperature	-65	150	°C
Tj	Maximum junction temperature		165	°C
Rqjc	Thermal resistance		10	°C/W

2.5.1.2 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Supply voltage	4.5	5.0	5.5	V
To	Operating temperature	-55	25	125	°C
Vi	Input Voltage	0	Vdd	Vdd	V
Vo	Output Voltage	0	Vdd	Vdd	V

2.5.1.3 DC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Vil	Input low voltage			0.8	V
Vih	Input high voltage		2.2		V
Vol	Output voltage low level	Vdd = Min Iol = 3 mA		0.4	V
Voh	Output voltage high level	Vdd = Min Ioh = -3 mA	2.4		V
Ioz	Output leakage current	Vdd = Max 0 ≤ Vout ≤ Vdd	-5	5	uA
Iiz	Input leakage current	Vdd = Max 0 ≤ Vin ≤ Vdd	-5	5	uA
Isc	output short circuit current (one output at a time during 1s max)	Vdd = Max Vout = 0v		48	mA
Iccop	Dynamic Supply current	Vdd = Max f = 40MHz (ClkIn)		350	mA

2.5.1.4 Capacitance ratings

Parameters	Description	Max (pF)
Cin	Input capacitance	5
Cout	Output capacitance	7
Cio	Input/output bus capacitance	10

2.5.1.5 AC characteristics for the ERC32/SC configuration

The following markers are used in the chronograms to reference timing values :

- Master configuration :
  - E1 : rising edge of CLK that precede BBSY falling edge
  - E2 : rising edge of CLK for which DTACKIN has been sampled low for the first time

- Slave configuration :
  - H1 : falling edge of CLK used by ERC to generate DRDY
  - H2 : rising edge of CLK for which DS* has been sampled high at the end of the access

ref	parameter	symbol	min	max
c1	CLK period in master mode	T	40 ns	
c2	CLK period in slave mode	T	56 ns	

ref	I/F	pin	dir	type	ref edge	min	max
EVI REGISTER INTERFACE							
r1	ERC	LA	in	setup time	CLK+	11,5	
r2	ERC	LA	in	hold time	CLK+	0	
r3	ERC	LD	in	setup time	CLK+	3,1	
r4	ERC	LD	in	hold time	CLK+	0	
r5	ERC	SIZE RD	in	setup time	CLK+	10,9	
r6	ERC	SIZE RD	in	hold time	CLK+	0	
r7	ERC	RSEL	in	setup time	CLK+	7	
r8	ERC	RSEL	in	hold time	CLK+	0	
r9	ERC	BUSDRY BUSERR	out	output delay	CLK+		25,6
r10	ERC	RSEL to LD invalid	out	output delay	RSEL -	0	
r11	ERC	RSEL to LD valid	out	output delay	RSEL-		24
r12	ERC	LD	out	hold time	CLK+		0
r13	ERC	RSEL to LD Hi-Z	out	output delay	RSEL +		24
r14	ERC	VIRQOUT	out	output delay	CLK+		21,3
EVI VME MASTER INTERFACE SINGLE WRITE							
m1	ERC	LA	in	setup time	CLK+	11,5	
m2	ERC	LA	in	hold time	CLK+	0	
m3	ERC	LD to VD valid	in	output delay	LD	0	16,8
m4	ERC	LD	in	hold time	CLK+	0	
m5	ERC	ASI SIZE	in	setup time	CLK+	11	
m6	ERC	ASI SIZE	in	hold time	CLK+	0	
m7	ERC	RD	in	setup time	CLK+	8,8	
m8	ERC	RD	in	hold time	CLK+	0	
m9	ERC	INULL	in	setup time	CLK+	3,8	
m10	ERC	INULL	in	hold time	CLK+	0	
m11	ERC	ALE	in	setup time	CLK+	6,7	
m12	ERC	ALE	in	hold time	CLK+	0	
m14	ERC	E1 to VASOUT	out	output delay	E1 CLK+	2T	2T + 21,4
m15	ERC	E2 to VASOUT	out	output delay	E2 CLK+	3T	3T + 21,4
m16	ERC	E1 to DSOUT	out	output delay	E1 CLK+	3T	3T + 21,0
m17	ERC	E2 to DSOUT	out	output delay	E2 CLK+	1T	1T + 21,0
m18	ERC	E1 to AM	out	output delay	E1 CLK+	1T	1T + 25,8
m19	ERC	E2 to AM	out	output delay	E2 CLK+	3T	3T + 25,8
m20	ERC	E1 to LWORD	out	output delay	E1 CLK+	1T	1T + 25,1
m21	ERC	E2 to LWORD	out	output delay	E2 CLK+	3T	3T + 25,1
m22	ERC	E1 to WRITE	out	output delay	E1 CLK+	1T	1T + 25,1
m23	ERC	E2 to WRITE	out	output delay	E2 CLK+	3T	3T + 25,1
m26	ERC	E1 to VA	out	output delay	E1 CLK+	1T	1T + 27,8
m27	ERC	E2 to VA	out	output delay	E2 CLK+	3T	3T + 27,8
m28	ERC	E1 to VD	out	output delay	E1 CLK+	2T	2T + 22,0
m29	ERC	E2 to VD	out	output delay	E2 CLK+	3T	3T + 22,0
m30	ERC	ABDIR	out	output delay	CLK-		16
m32	ERC	ABEN	out	output delay	CLK+		23,9
m34	ERC	ASDSEN	out	output delay	CLK+		18,2

m36	ERC	DBDIR	out	output delay	CLK+		16,3
m38	ERC	DBHEN DBLEN	out	output delay	CLK+		17,9

ref	I/F	pin	dir	type	ref edge	min	max
EVI VME MASTER INTERFACE - SINGLE READ							
m40	ERC	LD	out	Hi-Z to Invalid	CLK+	0	
m41	ERC	LD	out	Valid to Hi-Z	CLK+		22
m42	ERC	VD to LD Valid	out	output delay	VD		20,9
EVI VME MASTER INTERFACE - SINGLE WRITE ending with VME Bus error							
m43	ERC	IOBENIN to IOBENOUT	out	output delay	IOBENIN		14
m44	ERC	DDIRIN to DDIROUT	out	output delay	DDIRIN		11
EVI VME MASTER INTERFACE - LOAD STORE							
m45	ERC	LDSTO	in	setup time	CLK+	9,8	
m46	ERC	LDSTO	in	hold time	CLK+	0	
EVI VME MASTER INTERFACE - STORE DOUBLE							
m44	ERC	VD valid to LD valid	out	output delay	VD		20,9
EVI ARBITRATION							
a1	VME	BR3	out	output delay	CLK+		22,1
a2	VME	BR3(L) to BBSY(L)	out	output delay	BR3		1T + 3,0
a3	VME	BBSY	out	output delay	CLK+		21,4
a4	VME	BBSY(L) to BBSY(H)	out	duration	BBSY	4T	
a5	VME	BR3IN(L) to BG3OUT(L)	out	output delay	BR3IN		1T + 21,2
a6	VME	BR3IN(L) to BBSY(H)	out	output delay	BR3IN	1T + 0,0	
a7	VME	BG3IN(L) to BG3OUT(L)	out	output delay	BG3IN		2T + 21,2
EVI INTERRUPT MANAGEMENT							
i1	VME	IACKIN(L) to IACKOUT(L)	out	output delay	IACKIN		16,6
i2	VME	VRIQINx(L) to LIRQy(L)	out	output delay	VIRQIN		1T + 30,3
i3	VME	F1 to IACK(L)	out	output delay	E1 CLK+		1T + 25,7
i4	VME	F2 to IACK Hi-Z	out	output delay	E2 CLK+		4T + 25,7

EVI SLAVE INTERFACE							
s1	ERC	DMAREQ	out	output delay	CLK+		22,5
s2	ERC	DMAGNT	in	setup time	CLK+	6,7	
s3	ERC	DMAGNT	in	hold time	CLK+	0	
s4	ERC	LA+Control Hi-Z to Active	out	output delay	CLK-	0	
s5	ERC	LA+Control Active to Hi-Z	out	output delay	CLK-		27,3
s6	ERC	DMAAS low to high	out	output delay	CLK-		16
s7	ERC	DMAAS high to low	out	output delay	CLK-		12
s8	ERC	DRDY	in	setup time	CLK+	6,2	
s9	ERC	DRDY	in	hold time	CLK+	5	
s10	ERC	H1 to DTACK(L)	out	output delay	CLK-		2,5T + 21,5
s11	ERC	H2 to DTACK(H)	out	output delay	CLK+		1T + 21,5
s12	ERC	LD Hi-Z to Active	out	output delay	CLK+	0	
s13	ERC	LD Active to Hi-Z	out	output delay	CLK+		26,6
s15	ERC	IOBENOUT	out	output delay	CLK-		20,4
s16	ERC	DDIROUT	out	output delay	CLK+		22,9
s17	ERC	DMAADEN	out	output delay	CLK+		20,2
s18	ERC	DMAADTR	out	output delay	CLK-		19,1
s19	VME	VD	out	setup time	DTACK-	1,5T + 0,8	
s20	VME	VD	out	hold time	DS+	1T + 17,2	
s21	ERC	LD	in	setup time	CLK-	4,8	
s22	ERC	LD	in	hold time	CLK-	0	

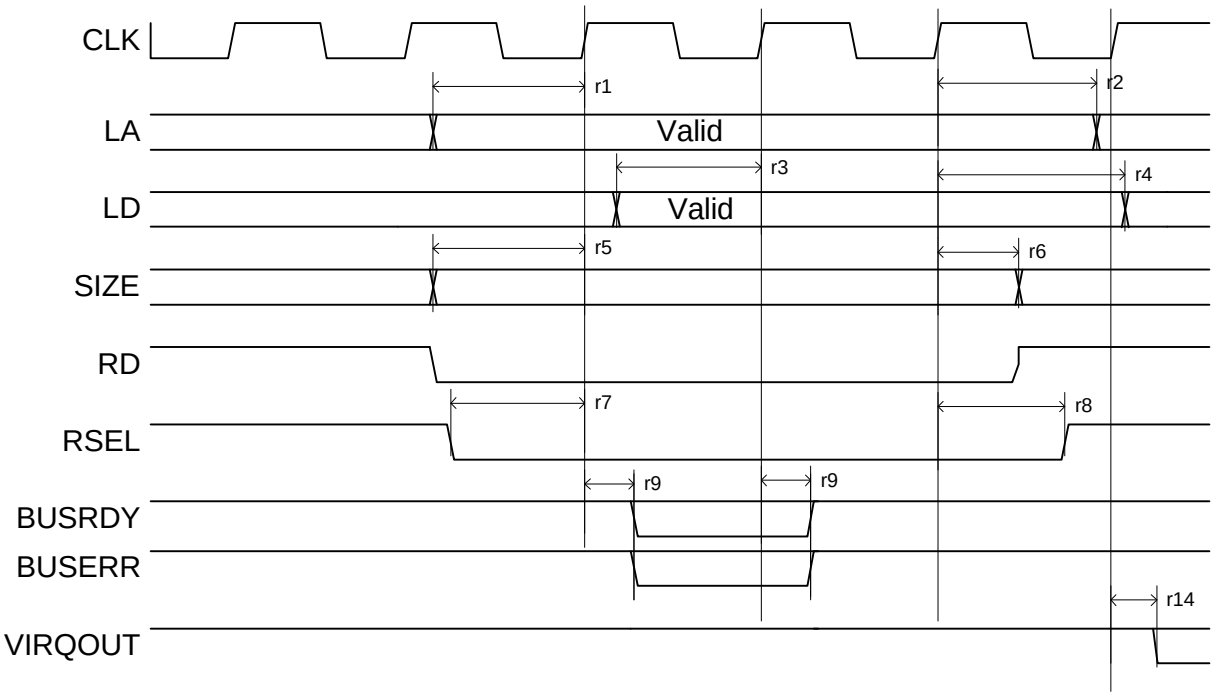


Figure 2.5-1 EVI Register write

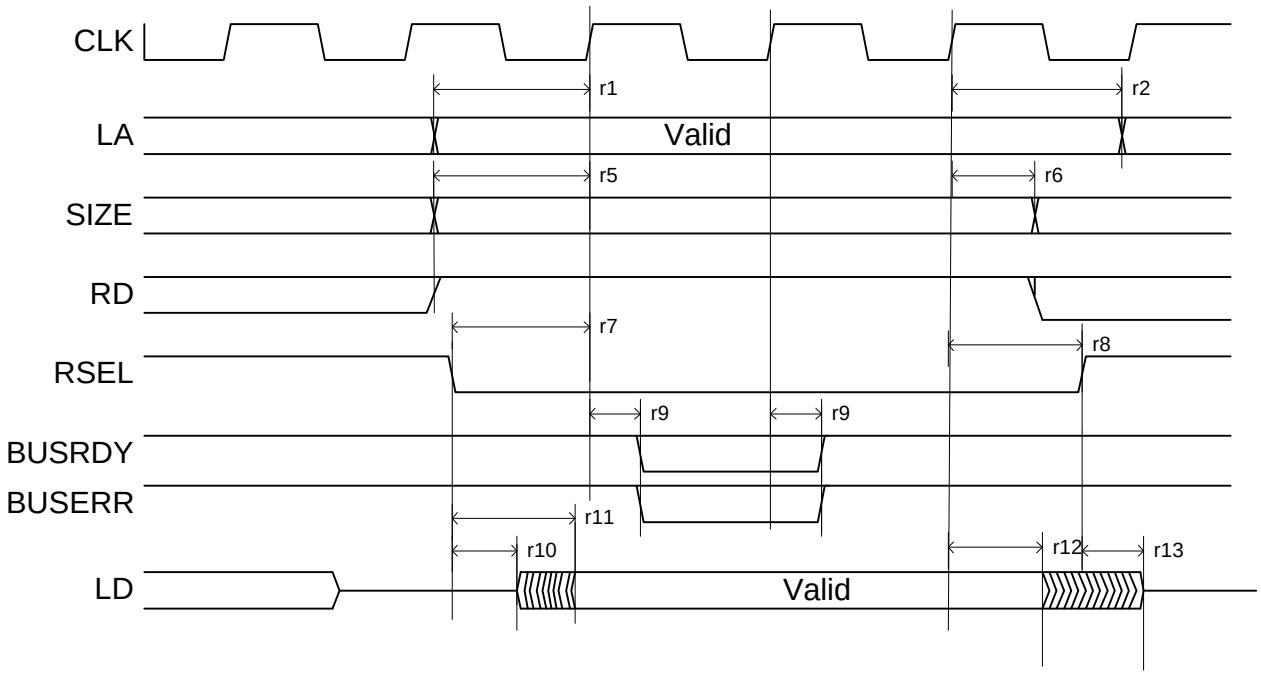


Figure 2.5-2 EVI Register read

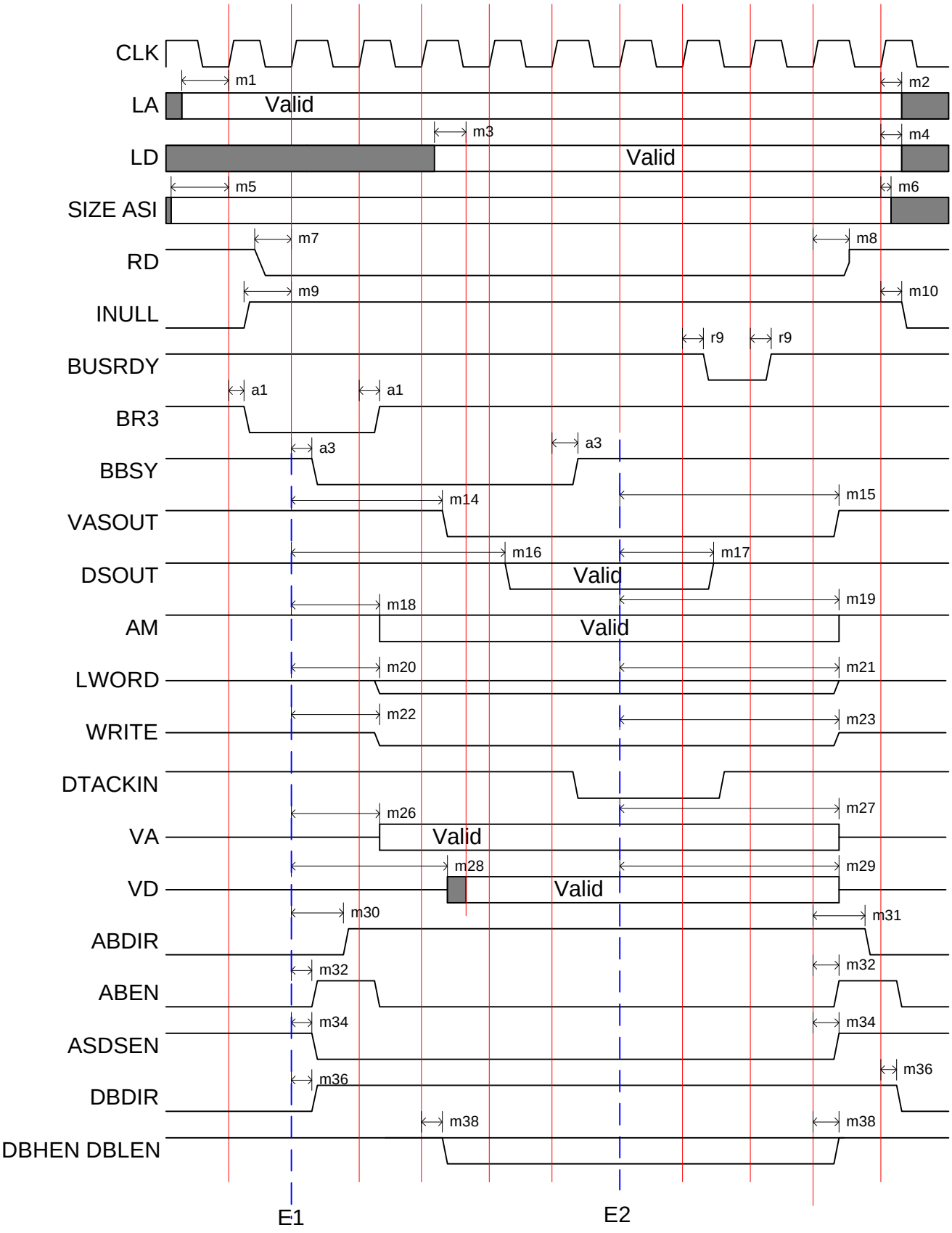


Figure 2.5-3 EVI Master : single access write

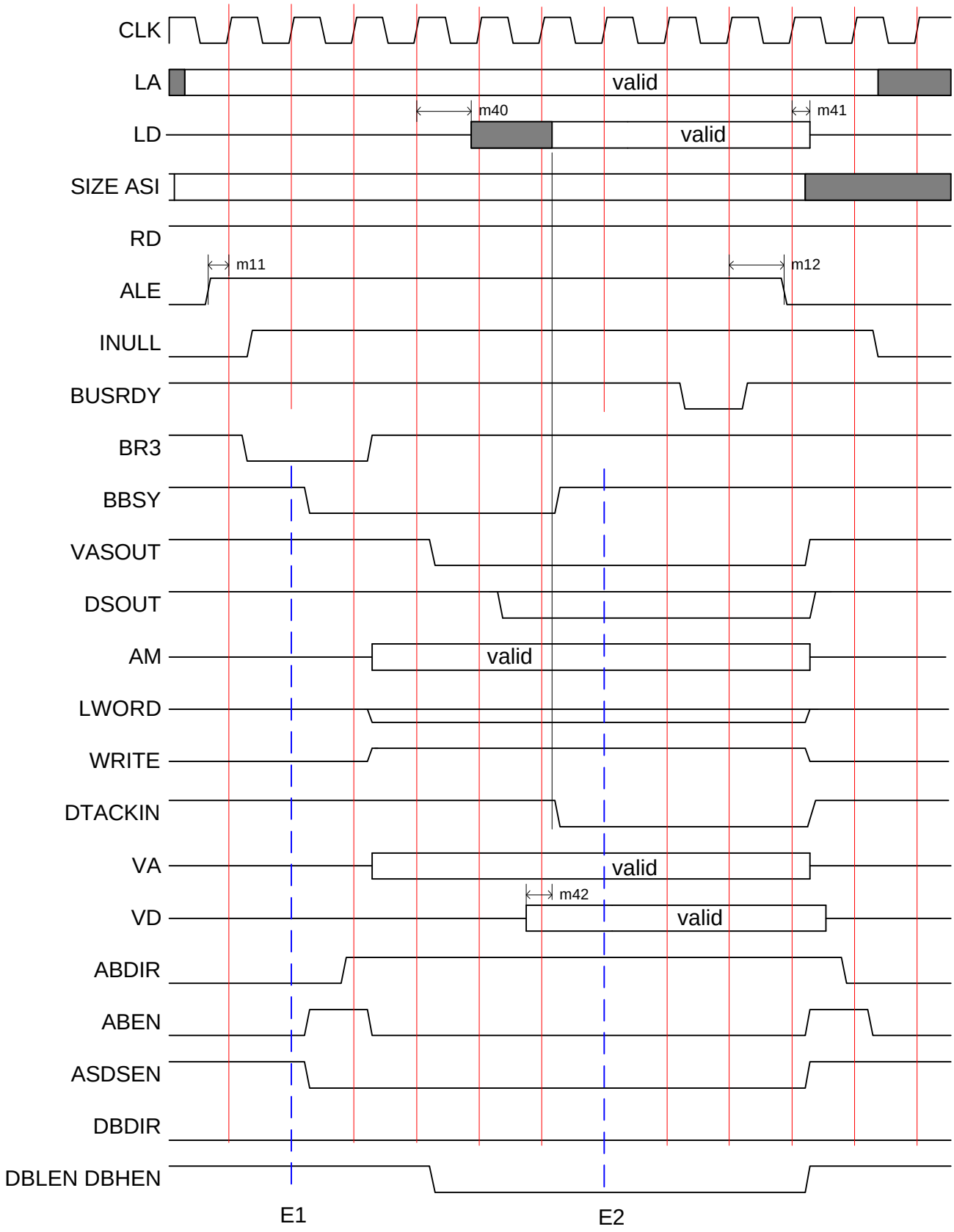


Figure 2.5-4 EVI Master : single access read

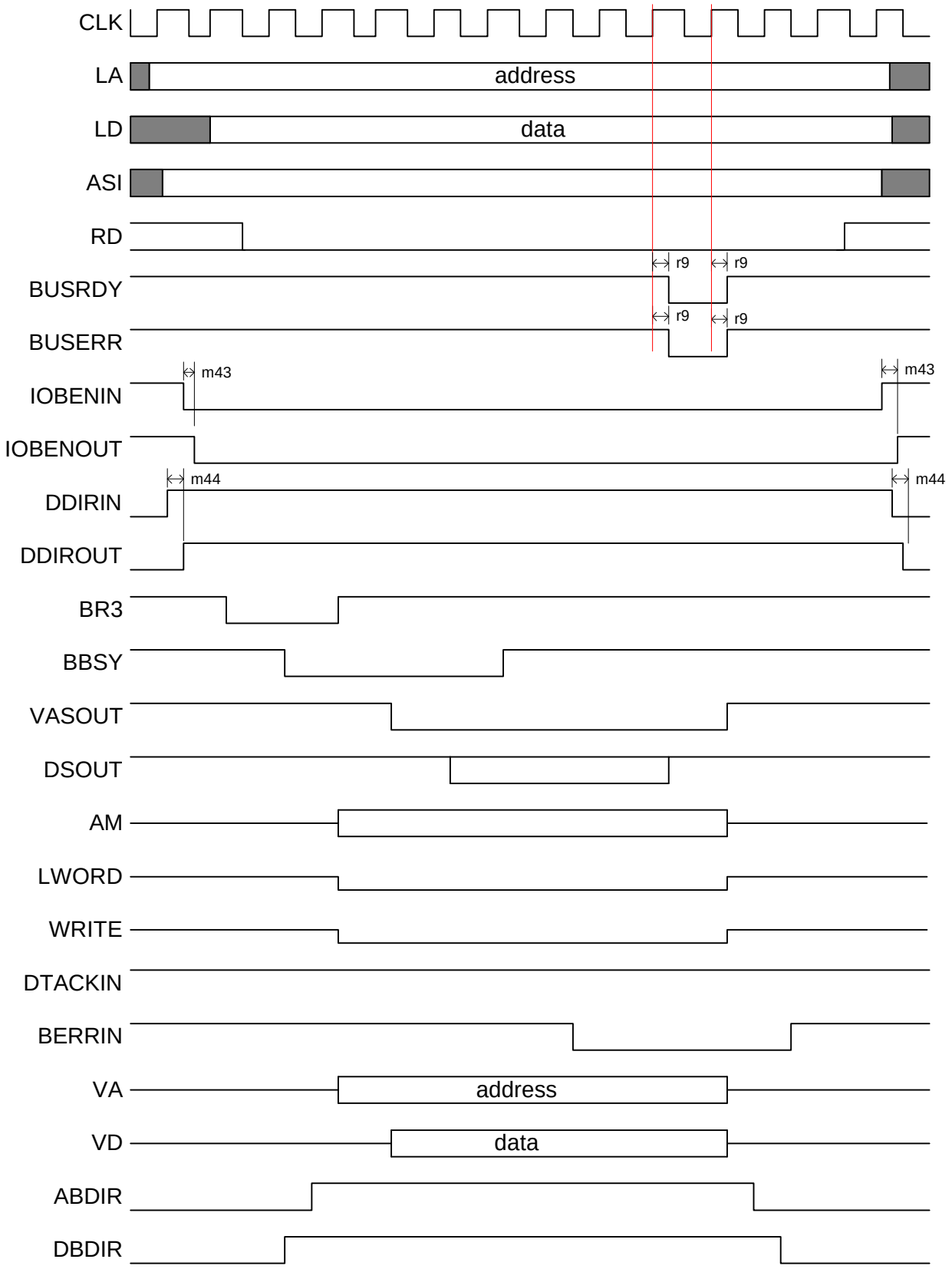


Figure 2.5-5 : EVI Master : access ending by a BERR

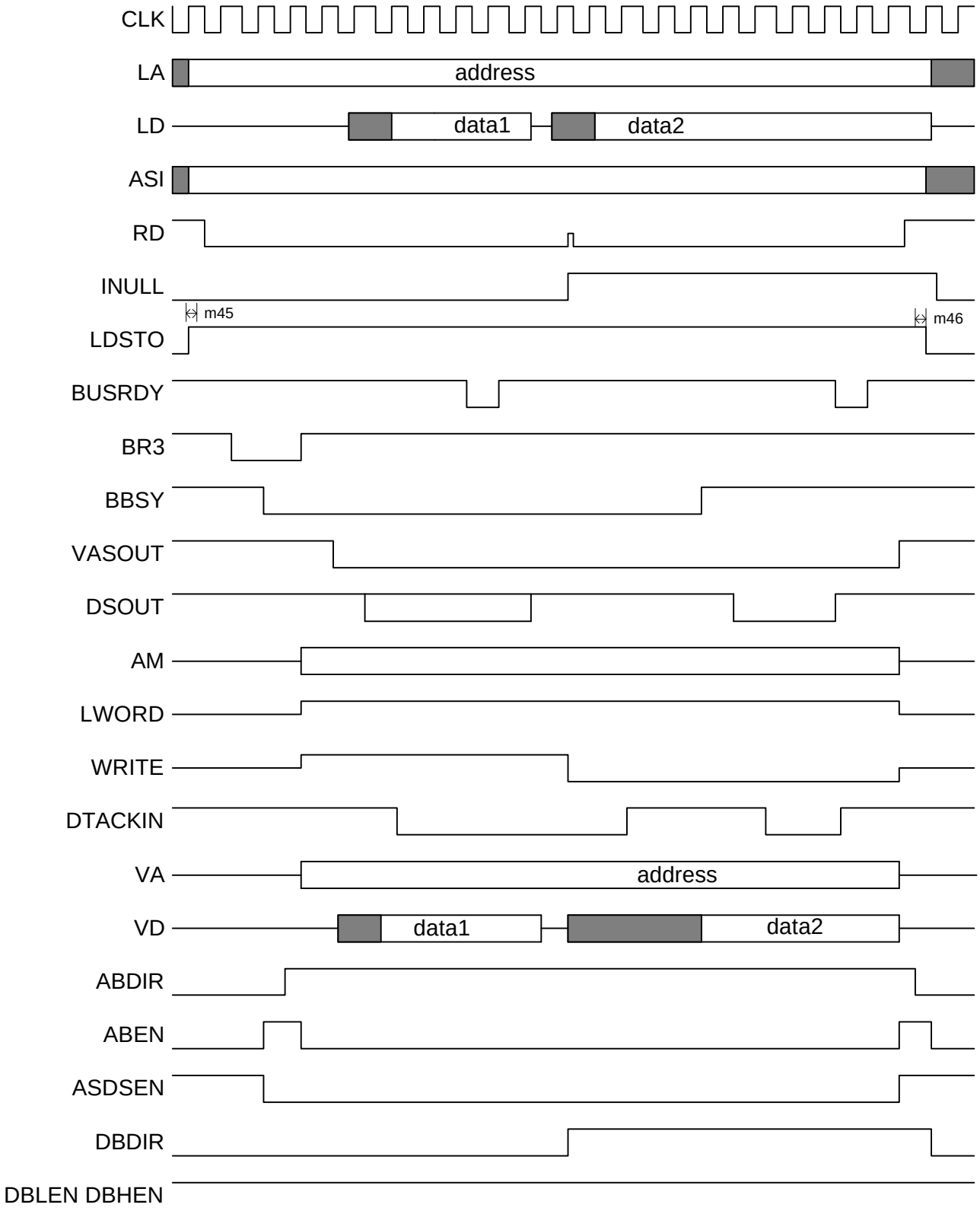


Figure 2.5-6 : EVI master : VME read modify write issued from an ERC load store instruction

for ERC32/3C please refer to Figure 2.5-18

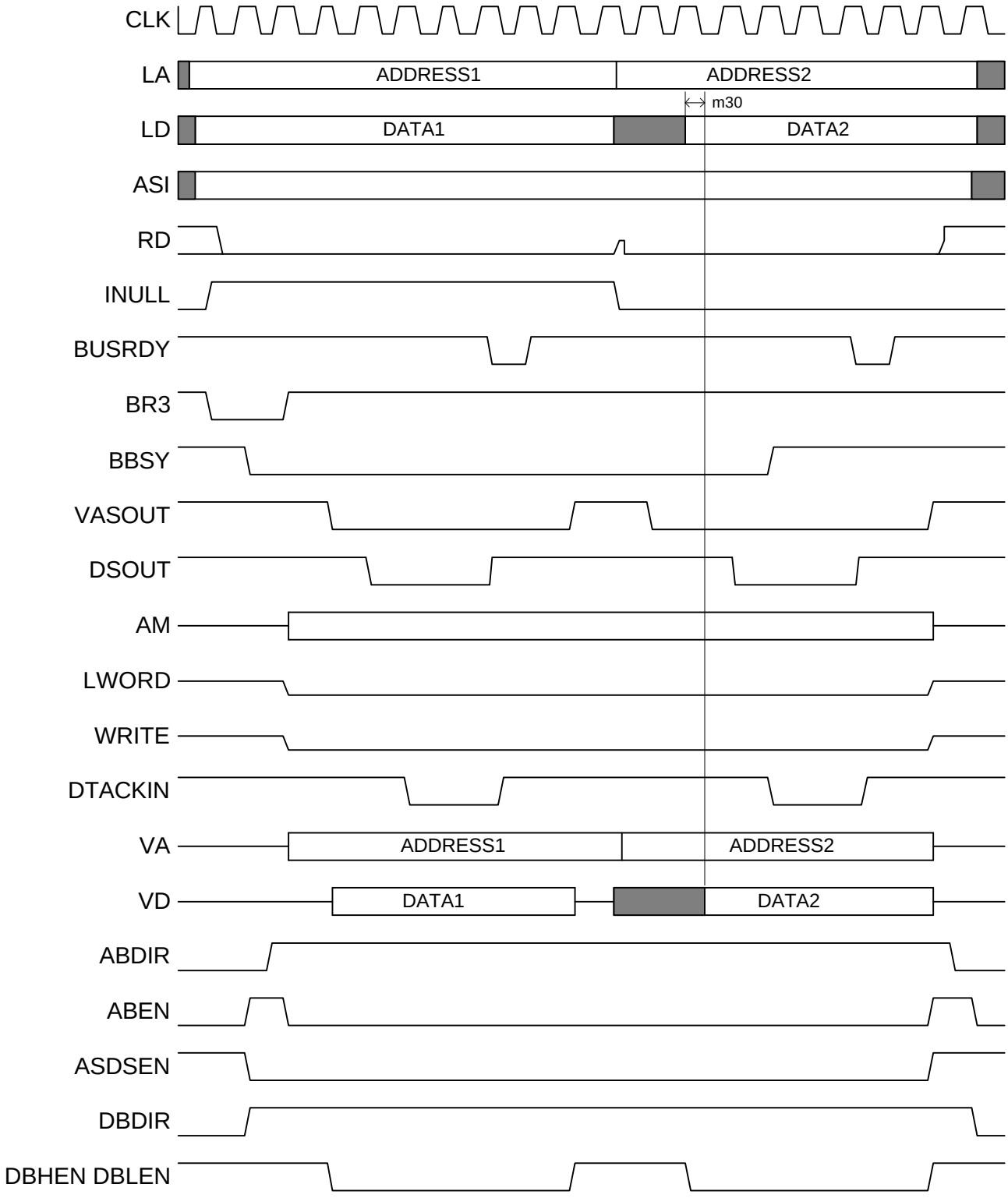


Figure 2.5-7 - EVI Master : double VME write from an ERC32 Store Double instruction

for ERC32/3C please refer to Figure 2.5-19

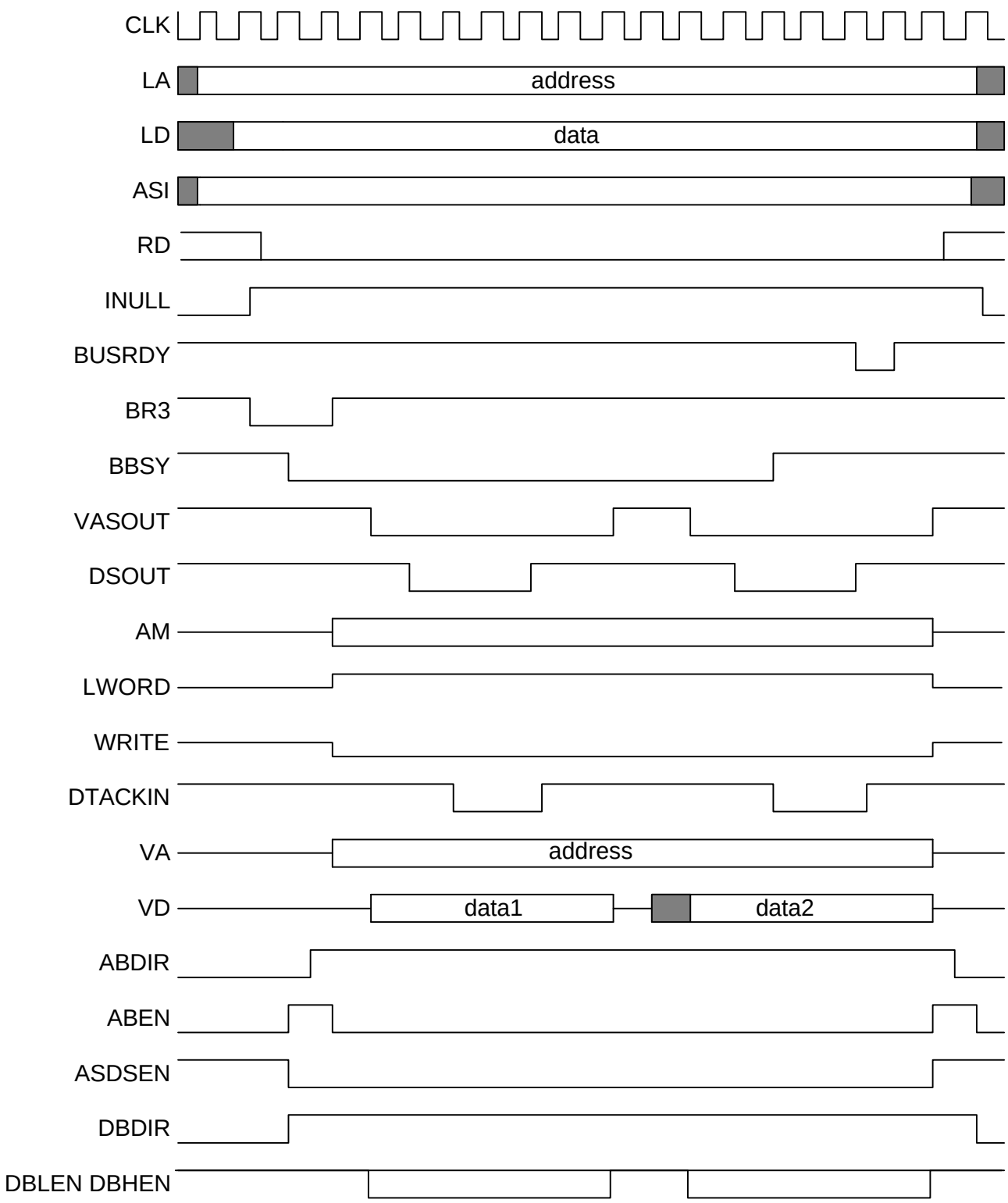


Figure 2.5-8 : EVI master : D16 VME write

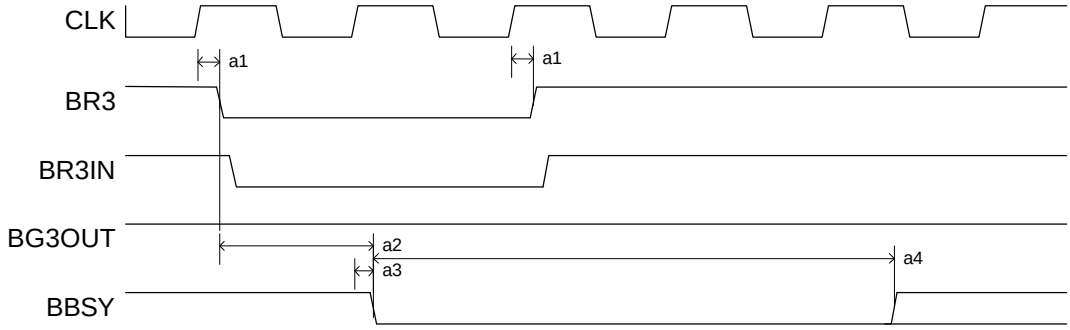


Figure 2.5-9 EVI Bus Arbiter and Bus Requester

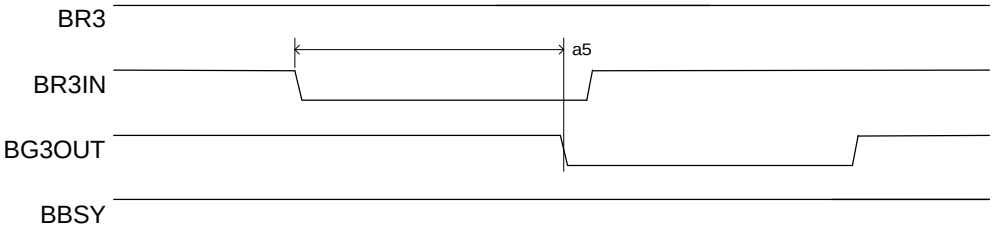


Figure 2.5-10 EVI Bus Arbiter - EVI32 as Arbiter initiating Arbitration daisy chain

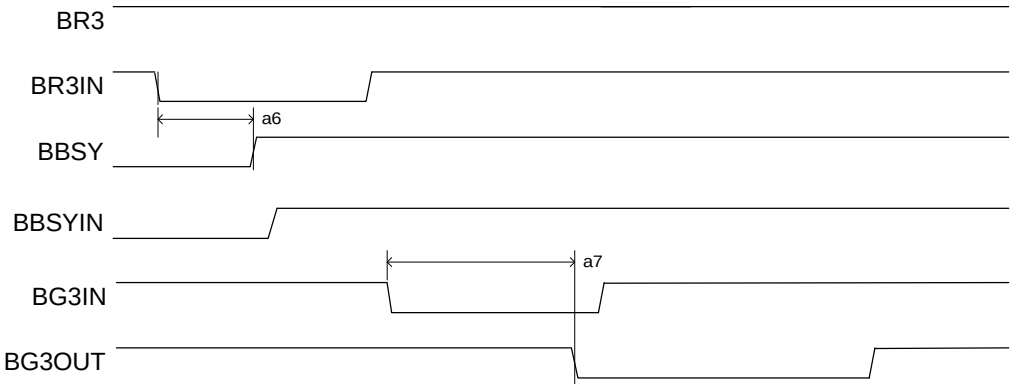


Figure 2.5-11 EVI32 not Arbiter - Daisy chain propagation

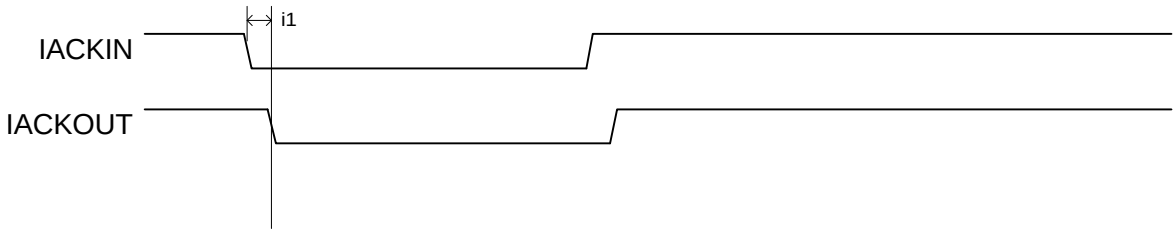


Figure 2.5-12 IACK daisy chain propagation

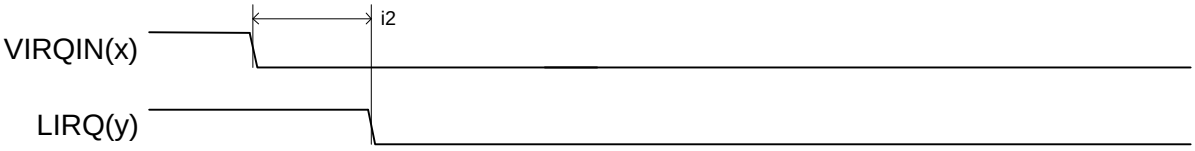


Figure 2.5-13 EVI Interrupt handler : VIRQ to LIRQ

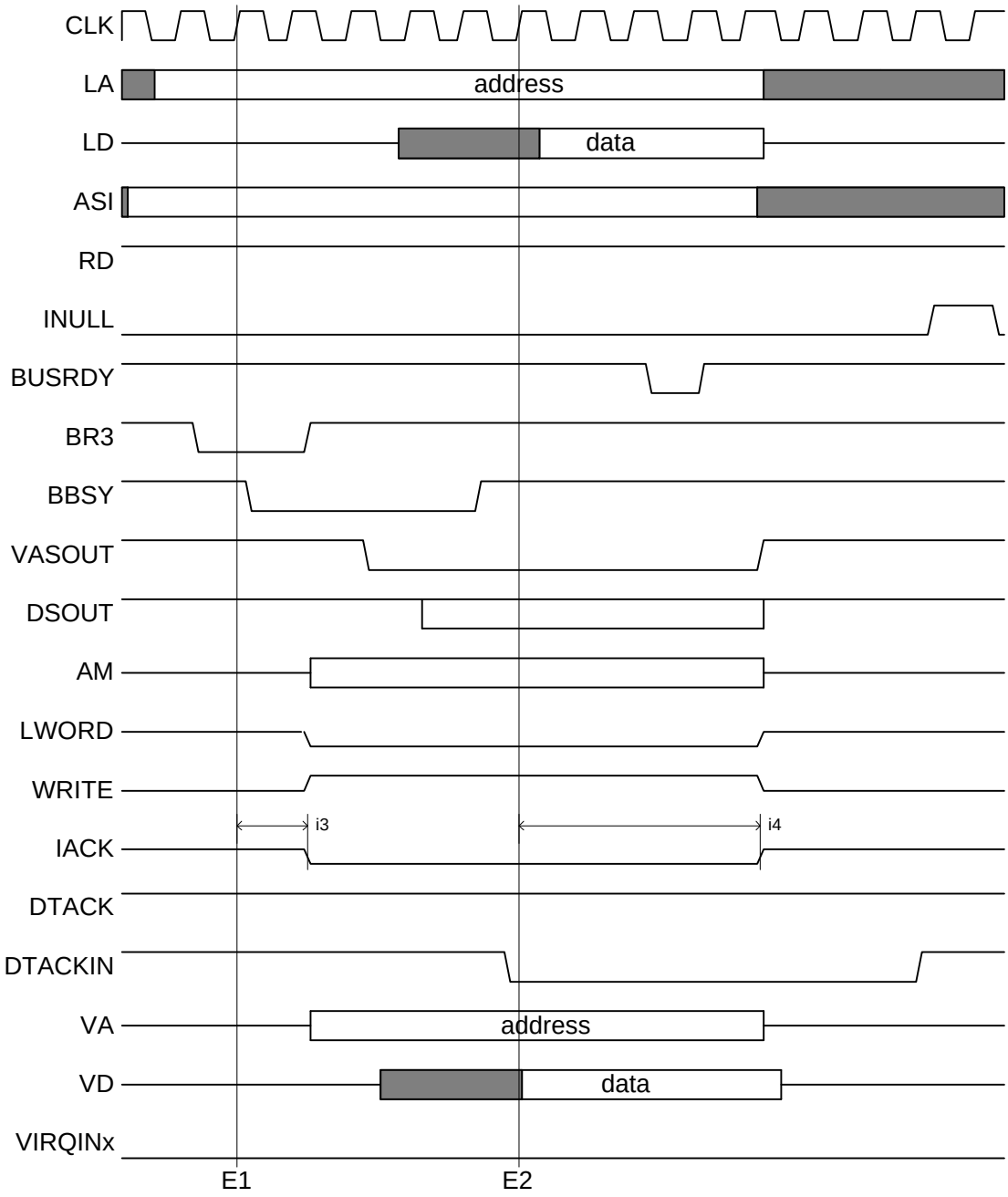


Figure 2.5-14 VME Interrupt Acknowledge cycle

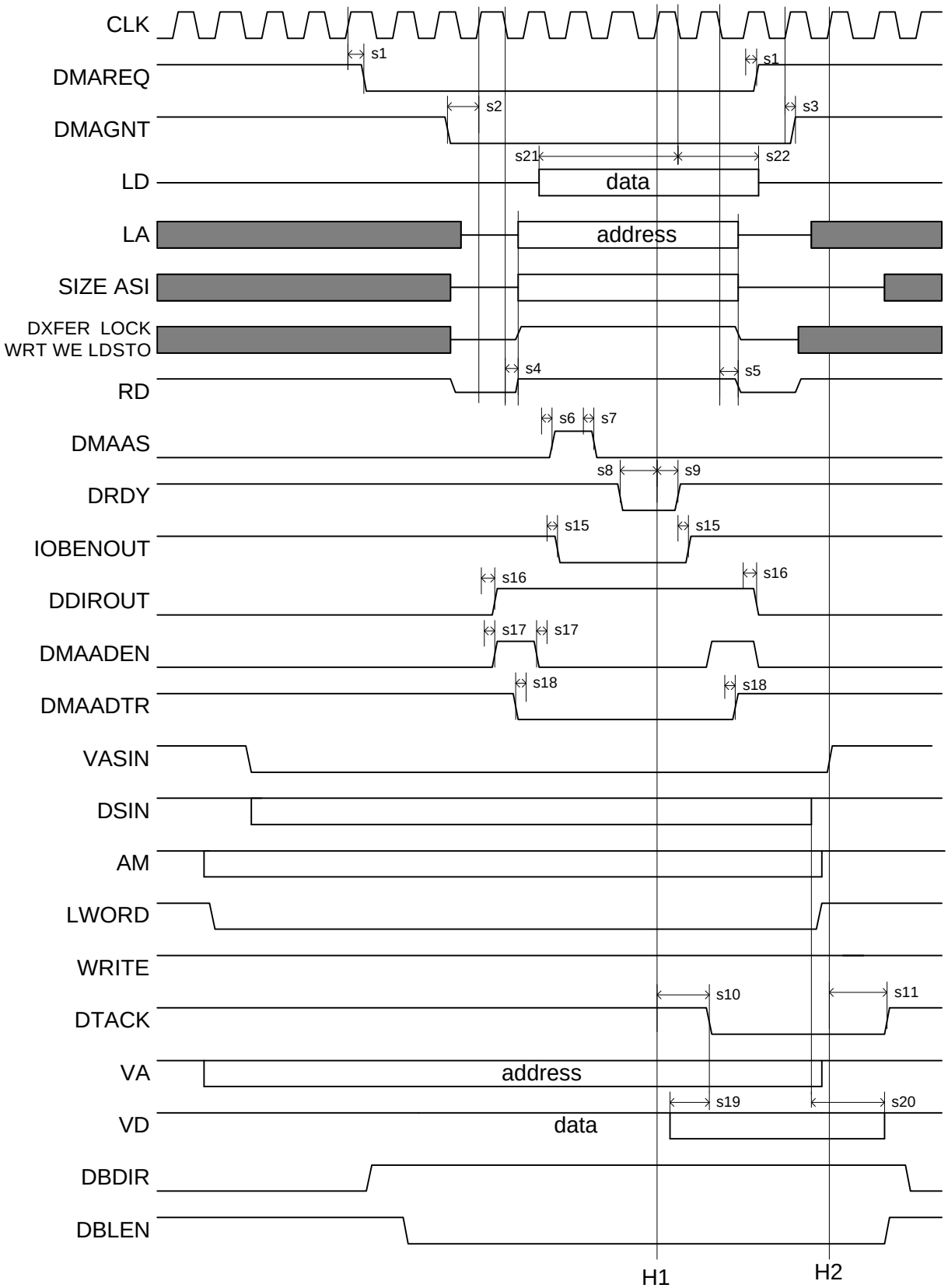


Figure 2.5-15 EVI slave : VME single read access

for ERC32/3C please refer to Figure 2.5-20

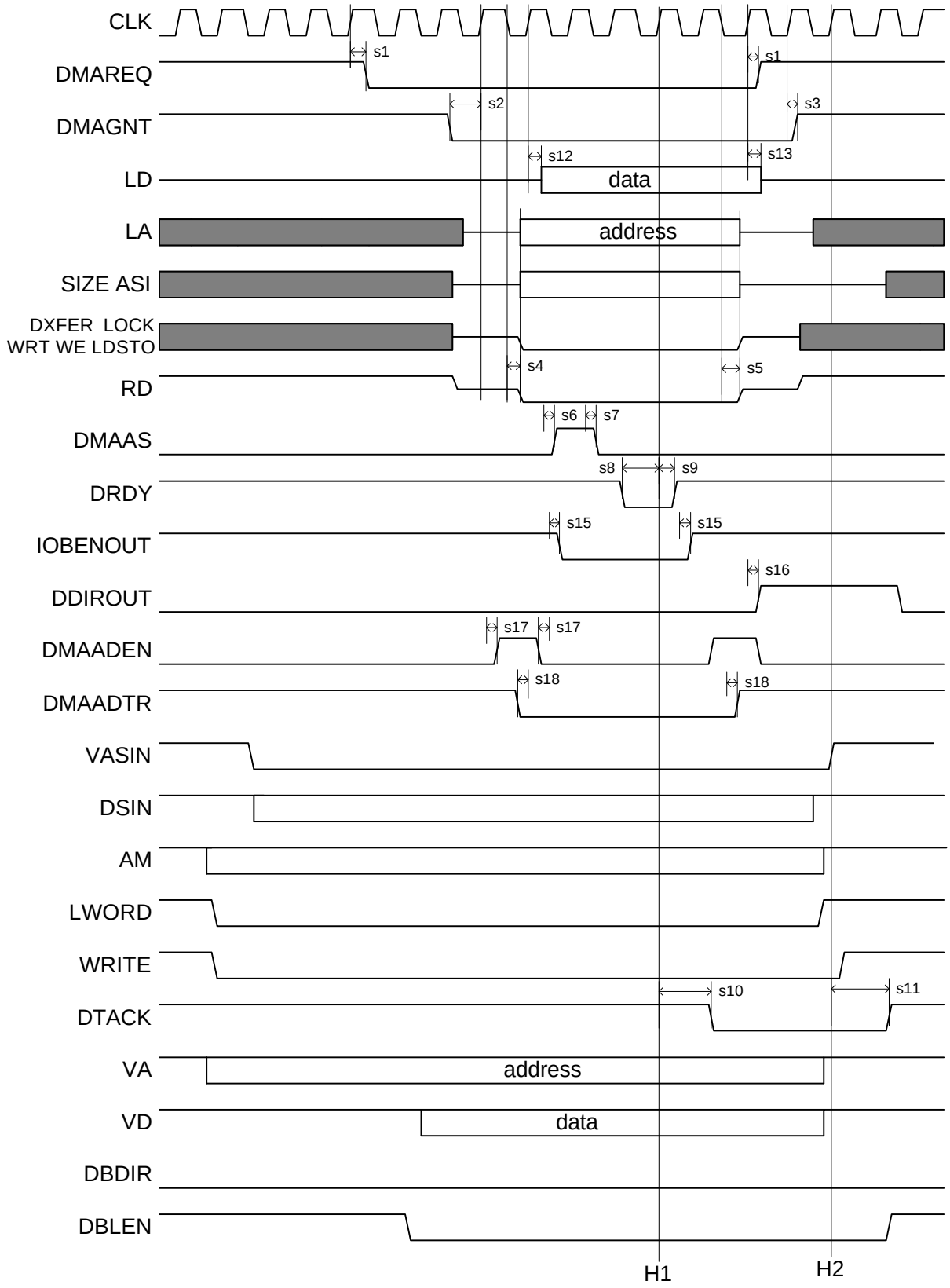


Figure 2.5-16 EVI slave : VME single write access

for ERC32/3C please refer to Figure 2.5-21

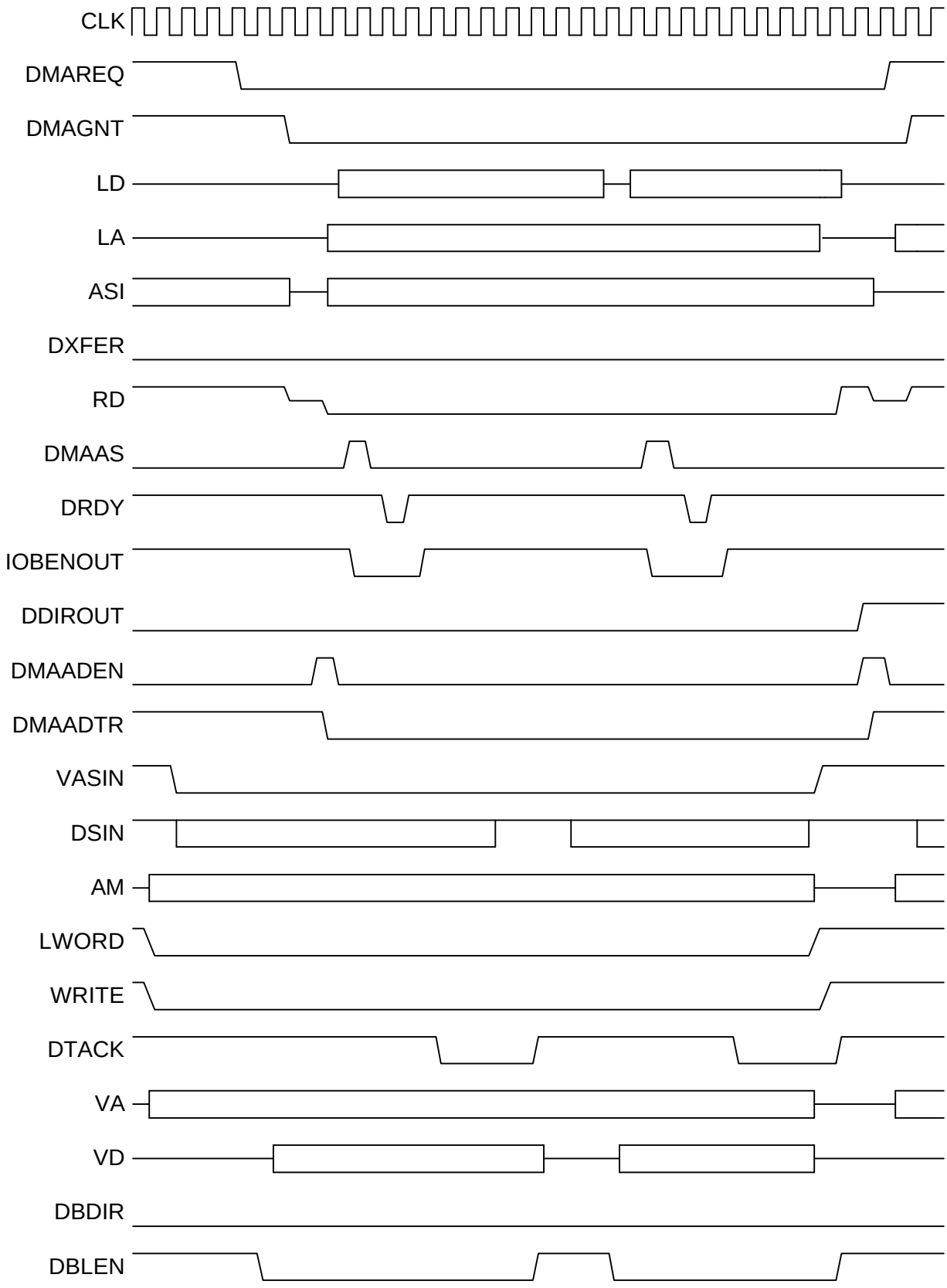


Figure 2.5-17 EVI slave : VME Block transfer write access

2.5.1.6 AC characteristics for the ERC32/3C configuration

The timing and chronograms given in the previous section for ERC32/SC applies for ERC32/3C configuration except when mentioned. In this section the chronograms specific to ERC32/3C are provided.

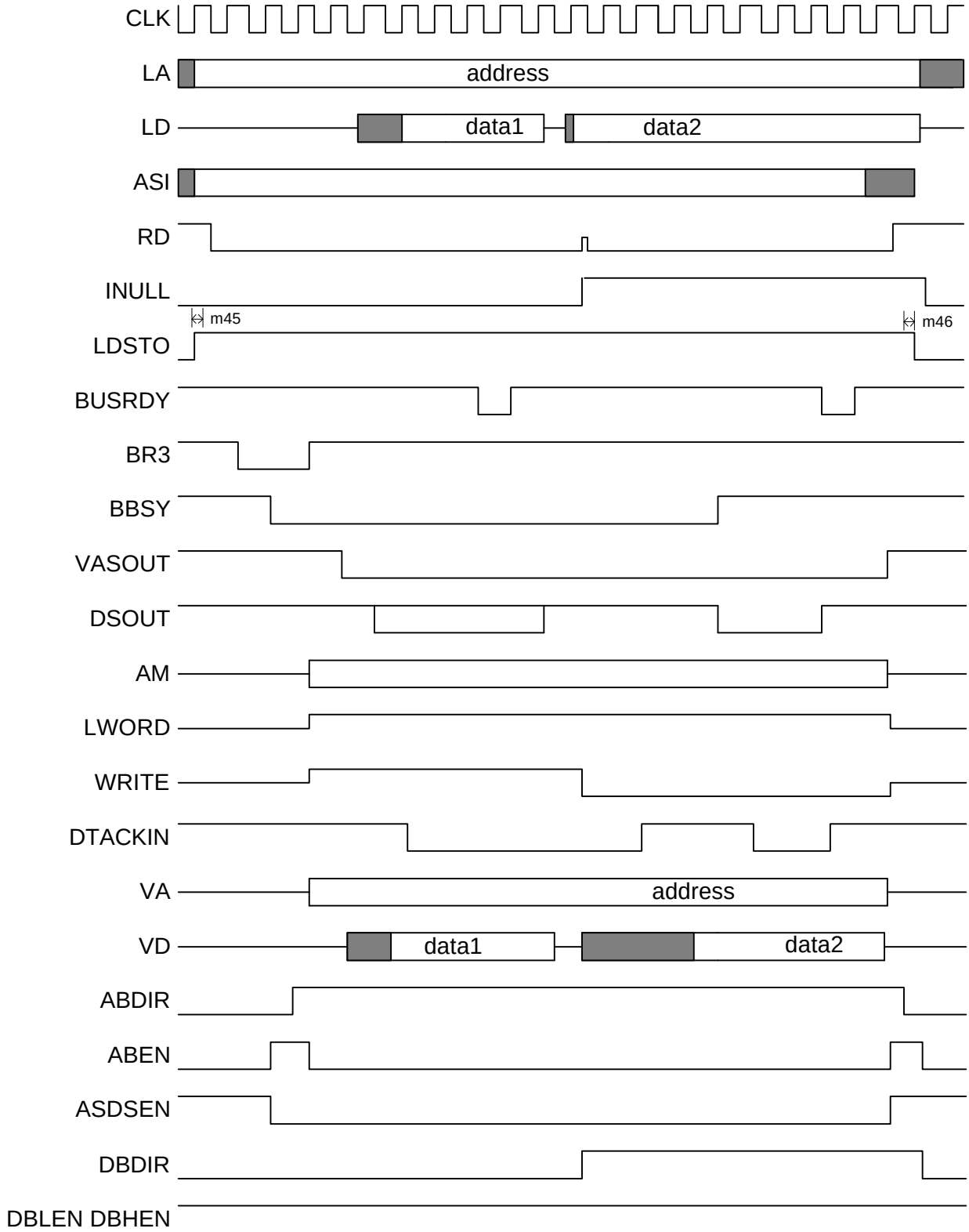


Figure 2.5-18 : ERC32 3C - EVI master : VME read modify write issued from an ERC load store instruction

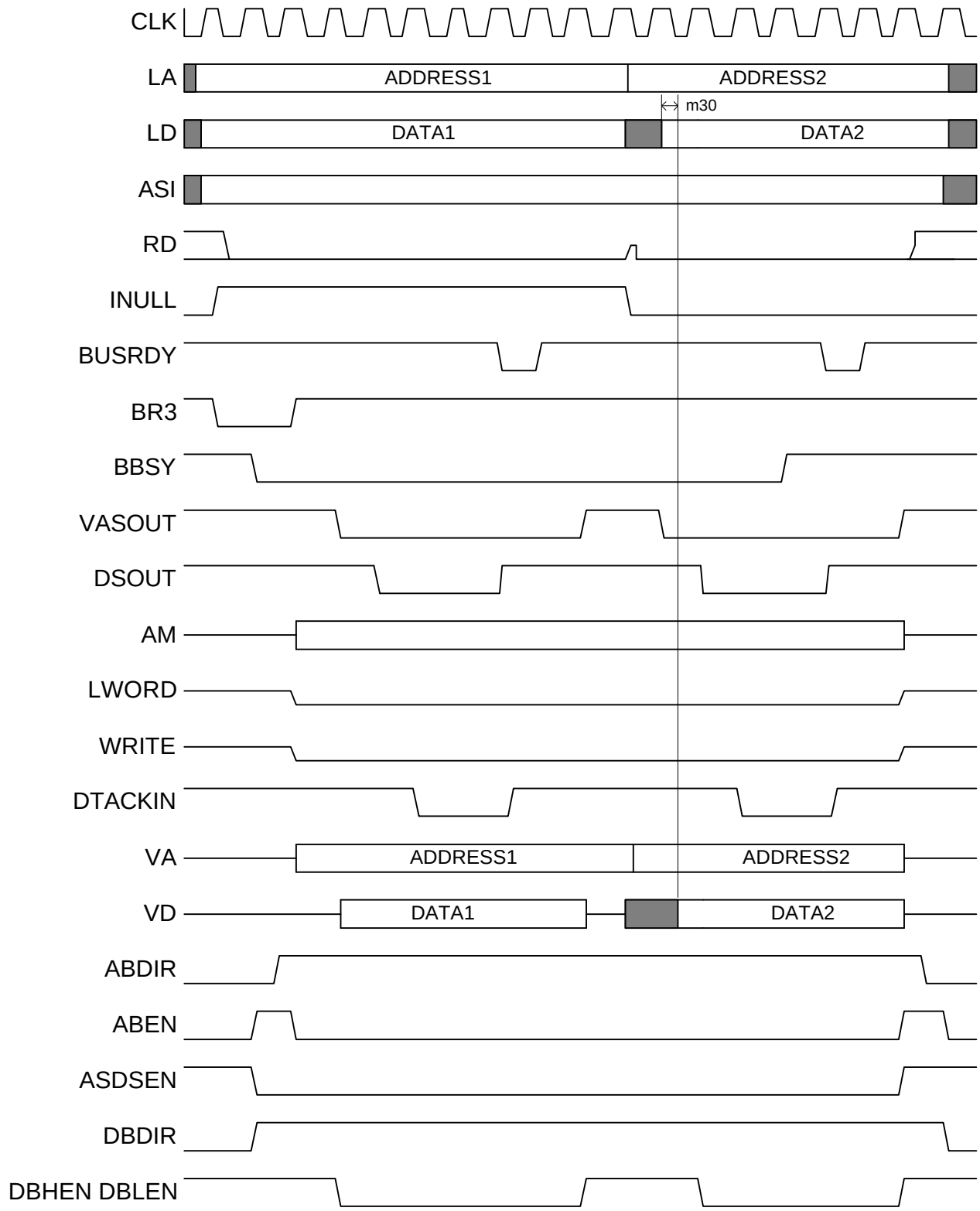


Figure 2.5-19 – ERC32 3C - EVI Master : double VME write from an ERC32 Store Double instruction

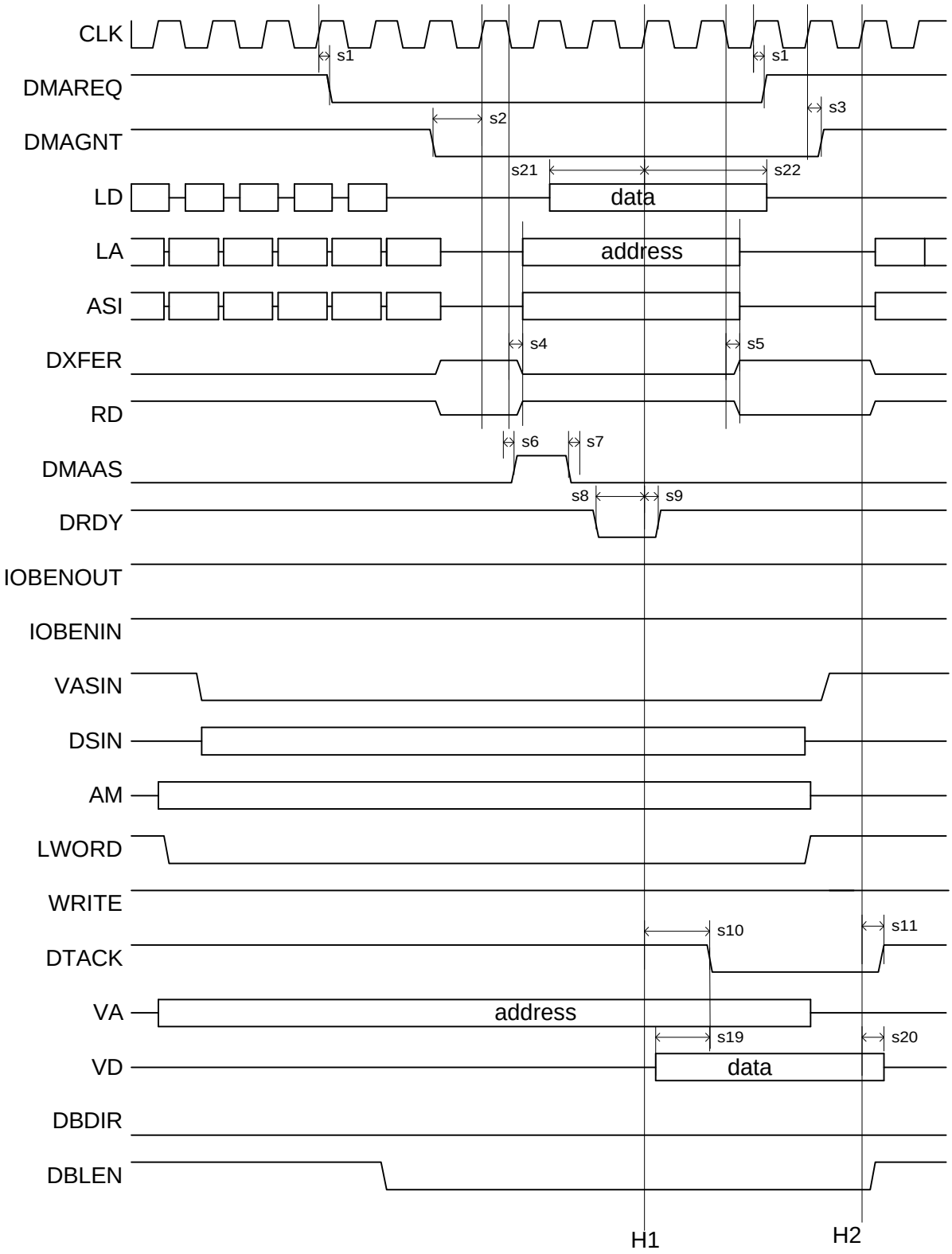


Figure 2.5-20 – ERC32 3 chips - EVI slave : VME single read access

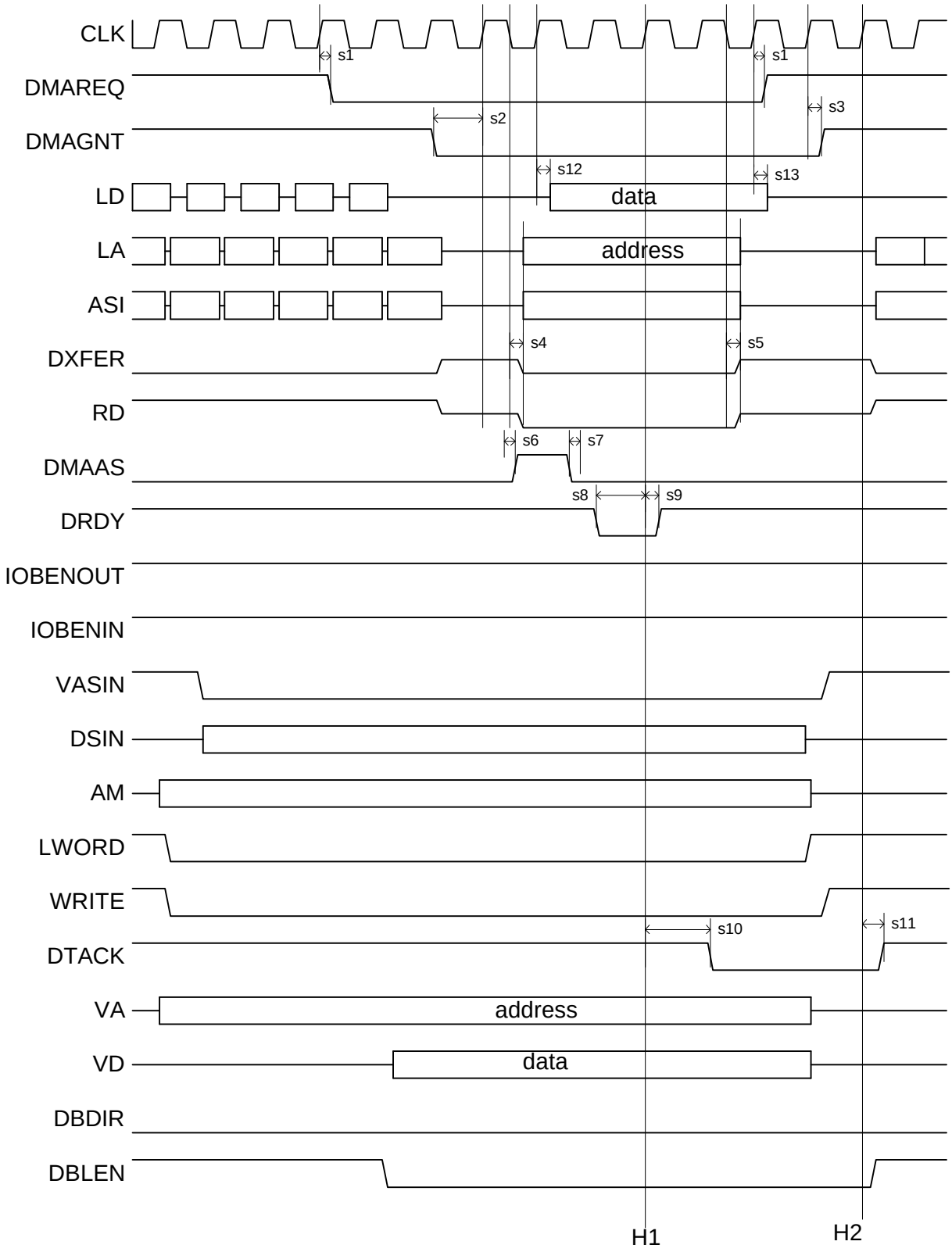


Figure 2.5-21 ERC32 3C - EVI slave : VME single write access

3. FUNCTIONAL DESCRIPTION AND CHARACTERISTICS FOR DSP/DPC INTERFACE

3.1 INTRODUCTION

This section presents the EVI32 interface to DSP and DPC.

3.2 GENERAL DESCRIPTION

The EVI32 device has been initially defined as a 32-bit ERC32 interface to the VME bus (see AD1 and RD1). It has then been adapted to interface a DSP core circuit (MCM DSP or discrete DSP core circuit) to the VME Bus (see AD2 for DSP data sheet, AD3 for DPC specification and AD4 for MCM DSP specification).

The EVI32 device fully adheres to the IEEE 1014-1987 VME bus standard (AD5), and is compatible with the commercial VME bus specification (AD6). EVI32 can act as a system controller and provides both master and slave interfaces.

The DSP version of the EVI32 implements the following functions:

- A32/A24/A16/D32/D16/D8 master interface (A32 and A24 modes have limitations due to the number of bits available on the address port);
- A24/D32/D16/D8 slave interface (A24 mode has limitations due to the number of bits available on the address port);
- Interrupt handler;
- Interrupter;
- Single level arbiter (SGL);
- VME bus timer;
- Optimised D16 interface;
- Four mailboxes for multi-processor communication;
- On-chip error-detection.

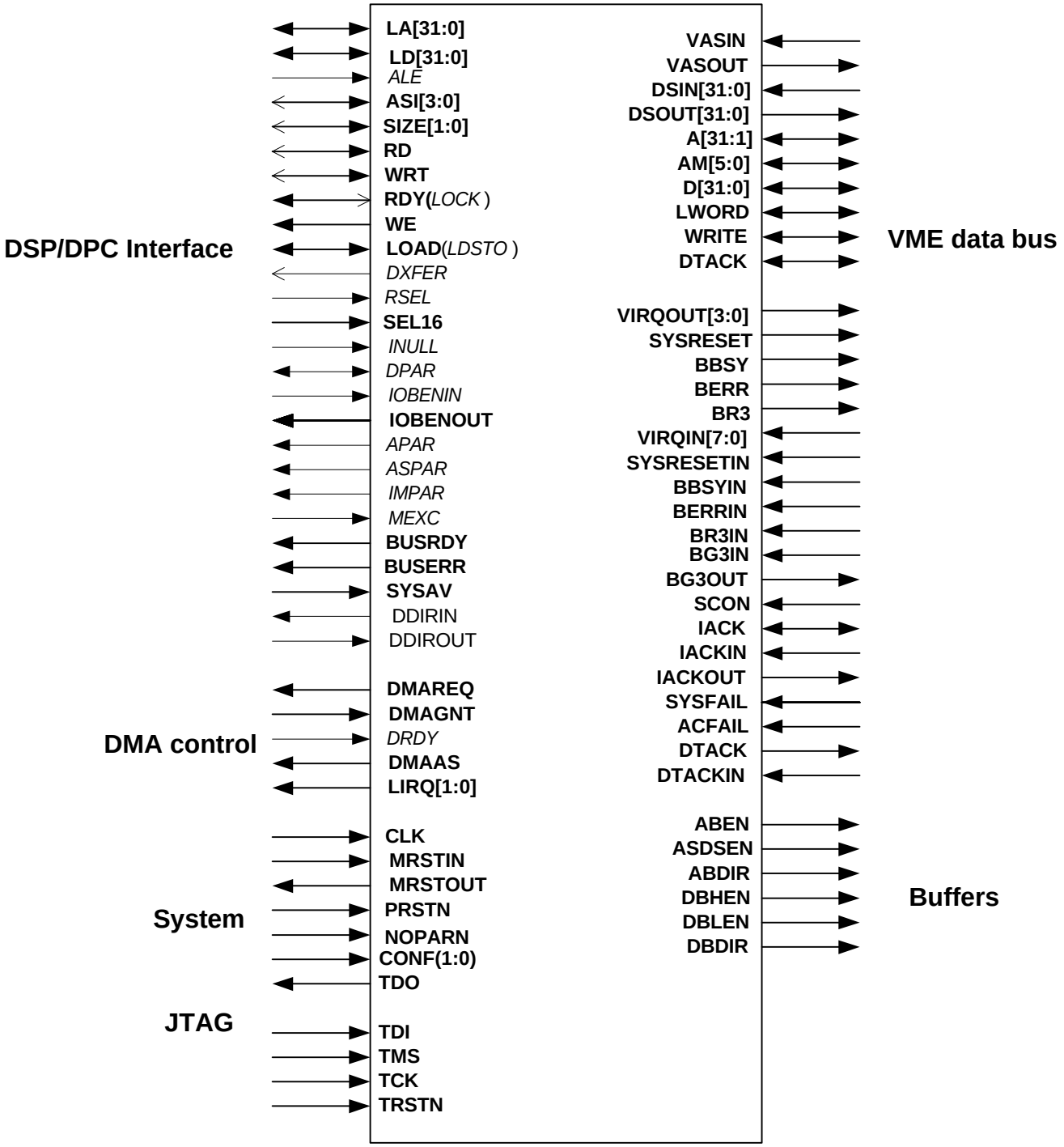


Figure 3-1 : EVI32 pin definition

The pin definition of the DSP version of the EVI32 asic is a subset of the pin definition of the ERC32 version.

The pins that are not used (*MEXC*, for example) are drawn in italic. The input pins that are not used have to be put to inactive level outside the asic. The output pins that are not used shall be not connected.

Some bi-directionnal signals have been changed in mono-directional signals (**ASI** for example). In that case, the right direction has to be selected inside the asic. A second thin arrow has been put on the signal to remember the ERC32 version definition.

Two signals have a new functional definition: **RDY** and **LOAD**. The initial signal name has been put under bracket. **LOAD** is used as a "read" signal during slave read accesses. **RDY** is a second active high "ready" signal used during master accesses (see section 3.3.3).

This new pin definition has been introduced only to clarify the DSP version specification. Then, the user will only see the initial (ERC32 version) pin names and will have to refer to this section to know the unused pins and the signals directions, to section 3.3.1 to know how to connect the EVI32 to a DSP core and to section 3.4 to know each pin definition.

3.2.1 EVI32/DSP interface

During slave accesses, the EVI32 loads and stores datas from/to the DSP program memory by using the DPC resource. It interfaces to the address and data busses of the DSP program interface via external buffers. It may interface directly to the control signals of the DSP program interface.

The DPC user interface is used to access the EVI32 internal registers and the master area. It is mapped in the DSP data interface (see AD3 or AD4). The EVI32 internal registers are mapped in the IO area 1 of the DPC. The VME bus is mapped in the IO areas 2 and 3 of the DPC. Data bus of the user interface is connected to the EVI32 through external buffers. Address bus and Control signals of the user interface may be connected directly to the EVI32.

If EVI32 is connected to a 16 bit VME data bus (D16), 32-bit DSP accesses can be transformed to two 16-bit VME transfers.

3.2.2 VME interface

The EVI32 provides signals for the VME control bus, address bus and data bus. These signals do not have adequate driving strength to drive the VME bus directly and therefore need external buffers. Depending on the width of the address and data busses of the attached VME bus, 6 to 11 external buffers are required.

3.2.3 Master cycles

Master cycles are generated by read and write accesses to I/O areas 2 and 3, mapped in DSP Data space. IO Area 2 is reserved for A32 and A24 VME accesses and IO Area 3 for A16 accesses and Interrupt acknowledges cycles. Two bits of the DSP address bus are used to identify the VME data bus width. During 8- and 16- bit accesses, the EVI32 performs byte swapping to align DSP and VME data.

3.2.4 Slave cycles

During slave accesses, the EVI32 will perform DMA cycles to the DSP program memory. Both 8, 16 and 32 bit accesses can be performed. Block access is allowed for all slave accesses. The internal slave select generator is used to select which VME address the controller will respond to.

3.2.5 Mailboxes

Four mailboxes are provided for inter-processor communication. The mailboxes consist of a 16-bit register mapped in the short VME address space. An interrupt can be generated upon reading or writing the mailbox.

3.2.6 Interrupt handler and interrupter

The interrupt handler can handle any of the seven VME interrupts. A VME interrupt will generate a local DPC interrupt (ExtIT(i)). VME Interrupt acknowledges cycles are performed by DSP by reading the interrupt ID of the interrupting device.

Commanded by the DSP, the interrupter can generate four VME interrupts. The interrupt ID can be individually programmed for all four interrupts.

3.3 FUNCTIONAL DESCRIPTION

3.3.1 (DSP/DPC)/EVI32 schematic

Figure 3-1 and Figure 3-3 show how the EVI32 asic is connected to DSP core respectively in discrete and MCM versions.

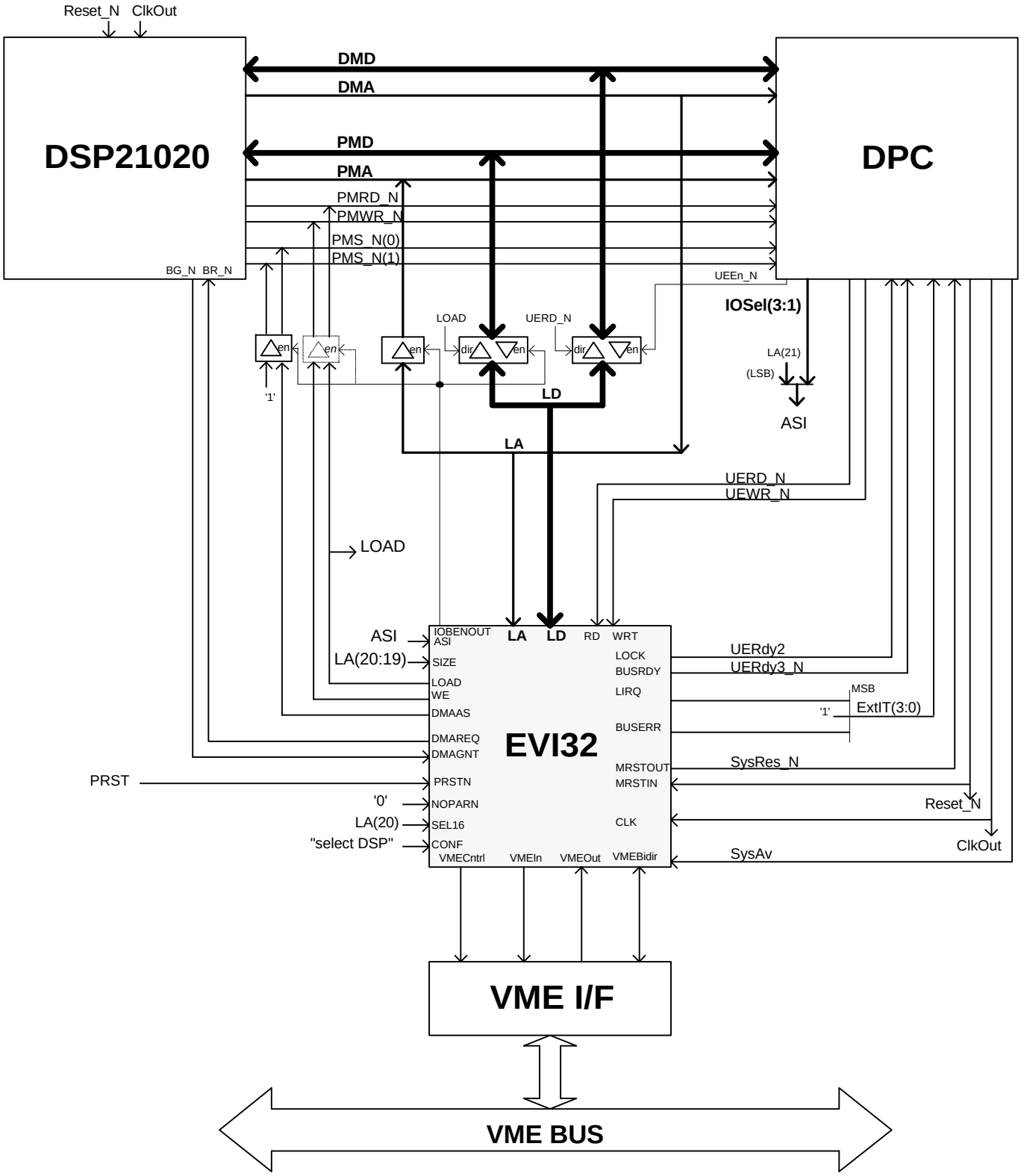


Figure 3-2: EVI32 to discrete DSP core interface

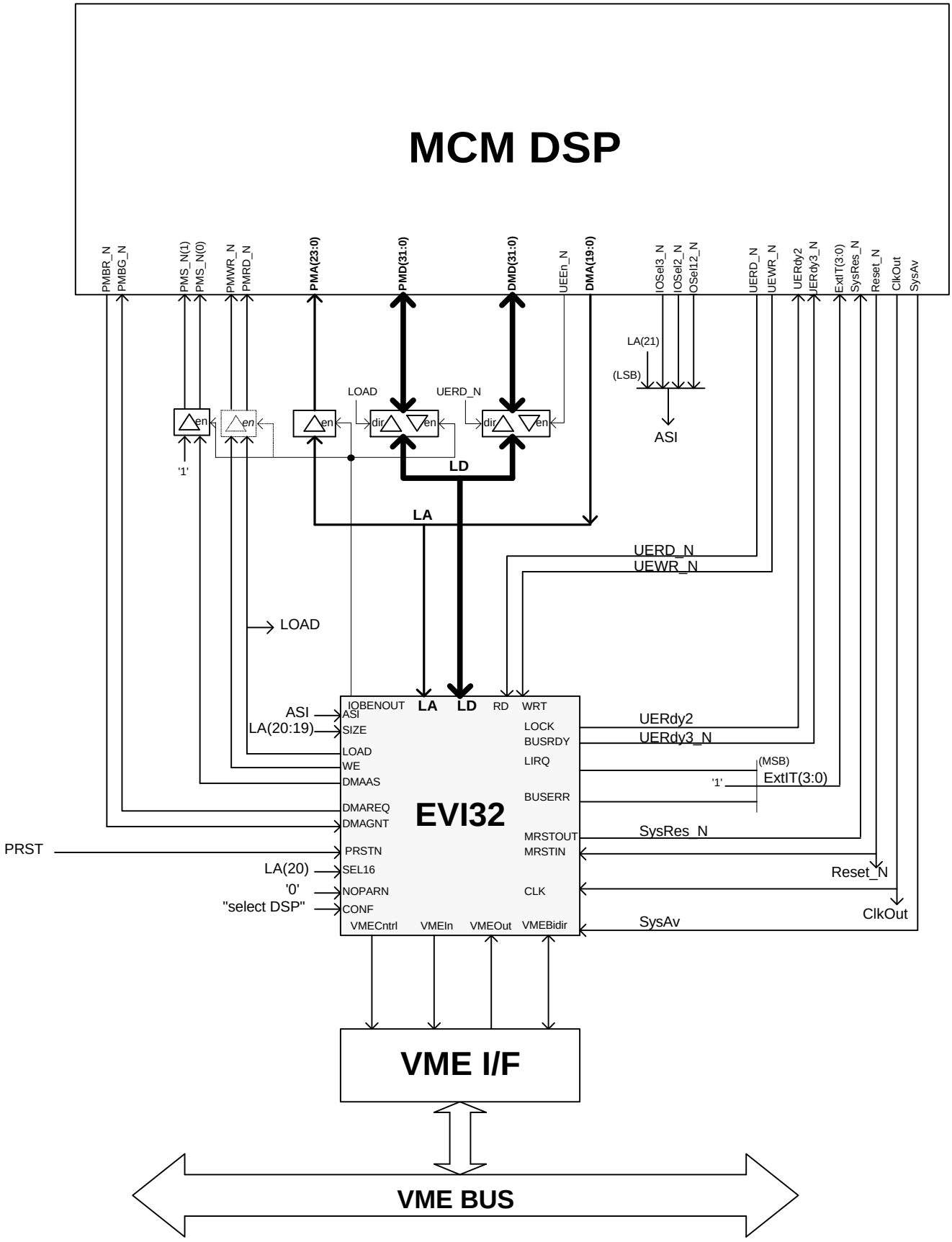


Figure 3-3: EVI32 to MCM DSP interface.

LOAD and WE signals may be connected directly or via external buffers to respectively PMRD_N and PMWR_N signals of the DSP.

IOSel12_N is a subset area of IOSel1_N, decoded by the MCM DSP. IOSel10_N and IOSel11_N, which are part of the same area (IO Area 1), are used inside the MCM for the SMCS function. For correct behavior of this function, IO Area 1 has to be programmed as a 3 Wait States area (see AD4). It is up to the user to program the right number of wait states before accesses, i.e. 3 Wait States for SMCS accesses and 1 Wait State for EVI32 internal registers accesses.

VME I/F contains the same VME Interface than that showed in paragraph 2.7 of the ERC32 version of the EVI32 specification (AD1).

Figure 2.3-3 gives the interconnection of EVI32 to VME bus. An option is given in this figure. According to VME standard the AS*, DS1* and DS0* signals shall be driven by tristate buffers. EVI32 allows the use of open collector buffers as drawn, in order to reduce buffer count. But the correctness of the use of open collector buffers with regards to the VME standard is under the responsibility of the user.

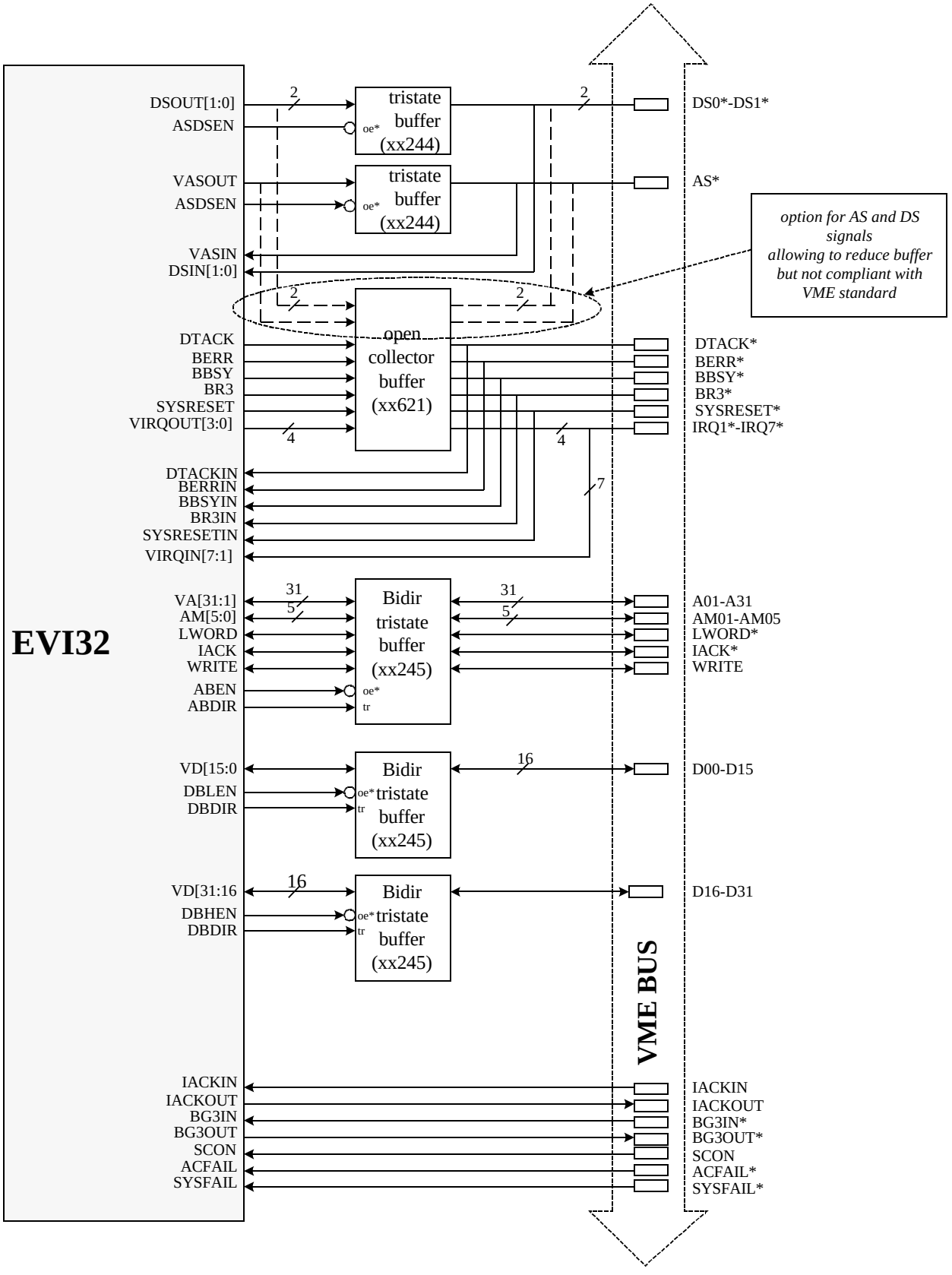


Figure 4 – EVI32 interface to the VME bus

3.3.2 EVI32 registers

3.3.2.1 General

EVI32 provides 14 internal registers to control the operation. The registers are accessed through IO Area 1 by programming one Wait State in the DPC. The registers are read and written with a 32 bits data bus width. An access to an unmapped register is ignored and no error are returned to the processor.

3.3.2.2 Register address map

Table 2-1 shows the EVI32 registers and their corresponding relative address.

Register	Function	Access	Address
MSTREG	Master control register	Read/Write	0x00
SLVREG	Slave control register	Read/Write	0x04
SLAREG	Slave address register	Read/Write	0x08
ICREG	Interrupt configuration register	Read/Write	0x0C
IDREG0	Interrupt identification register	Read/Write	0x10
CMDREG	Interrupt command register	Write only	0x14
ISTREG	Interrupt status register	Read only	0x18
MBCREG	Mailbox control register	Read/Write	0x1C
MB0REG	Mailbox 0 register	Read/Write	0x20
MB1REG	Mailbox 1 register	Read/Write	0x24
MB2REG	Mailbox 2 register	Read/Write	0x28
MB3REG	Mailbox 3 register	Read/Write	0x2C
SSTREG	System status register	Read/Write	0x30
SRREG	System reset register	Read/Write	0x34

Table 3-1 : EVI32 registers

3.3.3 Master interface

3.3.3.1 Operation

A VME cycle is started when an access is performed to the decoded part of the IO Area 2 and IO Area 3 as defined in the master configuration register. IO Area 2 is reserved for A32 and A24 accesses and IO Area 3 for A24 accesses and Interrupt Acknowledges cycles as shown in Table 2-4.

IOSe_N[3:2]	DMA[21]	AM[5:0]	VME Cycle type
“10”	‘0’”	0x0D	extended supervisory data access
“10”	‘1’	0x3D	standard supervisory data access
“01”	‘0’	0x2D	short supervisory data access
“01”	‘1’	0x3F	interrupt acknowledge cycle

Table 3-2 Master ASI versus AM mapping

The master interface supports one, two and four-byte transfers (LSB aligned in the DSP/DPC data bus). This is coded by bits 19 and 20 of the DSP address bus (DMA) as defined in Table 3-3. Whatever the value of these bits is, the DSP sees a byte oriented address space. For double byte accesses, the EVI32 forces the LSB of the incoming DSP address to zero. For quad byte accesses, the EVI32 forces the two LSB of the incoming DSP address to zero. Un-aligned VME master cycles cannot be generated by DSP and are then not supported.

DSP cycle	DMA[20:19]	VME cycle
IO Area read (LSB byte used)	“00”	read byte
IO Area write (LSB byte used)	“00”	write byte
IO Area read (two LSB byte used)	“01”	read double byte
IO Area write (two LSB byte used)	“01”	write double byte
IO Area read (whole data bus used)	“10”	read quad byte
IO Area write (whole data bus used)	“10”	write quad byte
IO Area read (whole data bus used)	“11”	two double byte read
IO Area write (whole data bus used)	“11”	two double byte write

Table 3-4 DSP versus VME cycles

The fields MVA1[7:0], IOS[1:0] and MVA2[7:0] in the master configuration register control define how DSP addresses are mapped on VME addresses (see section 3.3.3.5). The VME bus is mapped on the DSP data memory space between address 0x20800000 and address 0x20BFFFFF in IO Area 2 and between address 0x20C00000 and address 0x20FFFFFF in IO Area 3. The IOS field indicates how much of the DSP address is used for IO Area 2. The VME address is generated from the DSP address and the MVA1 and MVA2 fields. MVA1 field is used only for A32 accesses and contains the 8 MSB bits of the address. MVA2 field is used for A24 and A32 accesses. It contains the potential 16 to 24 bits of the VME address as defined in Table 2-3.

IOS	Used bits in MVA2	Used bytes in I/O area 2
00	7:0	64 K
01	7:1	128 K
10	7:2	256 K
11	7:3	512 K

Table 3-5 Extended general area mapping

If a VME cycle fails due to BUSERR being asserted, the error cause will be indicated in the system status register.

3.3.3.2 Accelerated D16 access

The EVI32 includes accelerated D16 access. This is done by converting quad byte DSP accesses to two double byte VME accesses. This feature is enabled in two ways.If the D16 bit is set in the master configuration register then all 32 bits DSP accesses are converted to D16 VME accesses. If D16 is not set, then the SEL16 input has to be asserted when accelerated D16 access is required. SEL16 has to be connected directly to DMA(19) address signal. The accelerated D16 accesses are not possible for interrupt acknowledge cycles.

3.3.3.3 Block transfer

Not available.

3.3.3.4 DSP bus time-out control

A DSP access to an I/O area will be aborted by the DPC if BUSRDY and RDY have not been generated within 255 clocks after the start of the access. To avoid aborting a VME transaction due to DPC time-out, the master interface includes a time-out counter.

The time-out counter will terminate the DSP VME access by generating BUSERR if:

- Timeout 1 : the VME bus have not been granted to the master interface. Enabling and duration of Timeout 1 is controlled by ET12 and ETD bits of the Master Configuration Register.
- Timeout 2 : he VME bus have been granted but the previous slave did not released the bus. . Enabling and duration of Timeout 2 is controlled by ET12 and ETD bits of the Master Configuration Register.
- Timeout 3 : the addressed slave did not respond within 248 clocks. . Enabling and duration of Timeout 3 is controlled by ET3 and ETD bits of the Master Configuration Register.

If the VME access is aborted due to the last case, the VME BERR signal will also be asserted.

In addition, the EVI32 contains a VME timer that starts when VASIN is activated and that stops counting when VASIN is released. Its duration and enabling is controlled by the VT bit of the Master Configuration Register.

3.3.3.5 Master configuration register

The master configuration register controls the master interface. The register is set to 00000000H during reset.

31	30	29	28 27	26	25	24	23 19	18 11	10	9 8	7 0
ETD	ET3	ET12	VT[1:0]	RR	ME	D16	N/U	MVA1[7:0]	N/U	IOS[1:0]	MVA2[7:0]

ETD : Timeout 1 2 and 3 duration

	Timeout 1	Timeout 2	Timeout 3
ETS = 0	128	160	248
ETS = 1	512	640	992

ET3	: Enable Timeout 3
ET12	: Enable Timeout 1 and Timeout 2
VT	: VME Timer Duration : 00 disabled, 01 : 256 clock cycles, 10 : 512 clock cycles, 11 : 1024 clock cycles
RR	: Release bus on request
ME	: Master interface enable
D16	: Accelerated D16 access enable
BT	: Block transfer enable
AA1	: Alternative AM codes
AA0	: Alternative AM codes
IOS	: I/O area size
MVA	: Most significant part of VME address

Table 3-6 Master configuration register

3.3.4 Slave interface

3.3.4.1 Operation

The slave interface provides access to the DSP program memory from an external VME master. The slave address is programmed in the EVI32 slave configuration register (see section 3.3.4.2.). The following cycle types are supported:

VME cycle
address only (no action)
read single, double & quad byte
read single, double & quad byte block
write single, double & quad byte
write single, double & quad byte block
read-modify-write single, double & quad byte
read & write unaligned

Table 3-7 Supported slave cycles

On single and double byte write accesses, the slave interface will perform a read-modify-write cycle to the DPC since the DMA interface only allows 32-bit accesses.

Slave decoding is done using the slave address (SA) field in the slave address register and the slave size fields (SSZ) in the slave configuration register. During standard address (A24) accesses, SA[6:0] is compared to bit [23:17] of the VME address. If equal, the slave is selected. The size field (SSZ) defines how many of the bits (starting from the left-most bit) shall be compared. In this way, the size of the slave is between 128k and 16M, and mappable anywhere in the VME A24 address space on an aligned block boundary. The most significant part of the local address is generated in a similar fashion and taken from the LMA field in the slave address register. The mapped VME area can thereby be mapped on any block aligned address in the full DSP address space.

Note: it is impossible that a master access selects its own slave area because the master space is located in DSP data memory and the slave space in DSP address memory. Likewise it is impossible that a slave access is done in the master space.

The following VME accesses are supported:

- VME standard supervisory program accesses: AM[5:0] = 0x3E.
- VME standard non-privileged program access: AM[5:0] = 0x3A.
- VME standard supervisory block transfer: AM[5:0] = 0x3F.
- VME standard non-privileged block transfer: AM[5:0] = 0x3B.

If the keep bus bit (KB) in the slave configuration register is set, then the DSP DMA request will be kept during a whole block transfer and during a complete read-modify-write cycle. If KB is not set, the local bus will be released to DSP after each bus access. The KB bit increases the transfer rate but halts the DSP for a longer time.

3.3.4.2 Slave configuration register

The slave configuration register defines the operation of the slave interface. The register is set to 00000000H during reset.

15	14	13	12	11	10	9	8	7	6 4	3 0
KB	SE	PE	NP	SV	BE	N/U	ST	N/U	SSZ[2:0]	N/U

KB : keep bus during block and RMW cycles
SE : slave enable
PE : program accesses enable
NP : non-privileged accesses enable
SV : supervisory accesses enable
BE : block transfer enable
ST : enable standard address decoding
SSZ : decoded slave area size for standard addressing

ESZ	A32 size	see Note 1	SSZ	A24 size	see Note 1
0000	128 k	15	000	128 k	7
0001	256 k	14	001	256 k	6
0010	512 k	13	010	512 k	5
0011	1 M	12	011	1 M	4
0100	2 M	11	100	2 M	3
0101	4 M	10	101	4 M	2
0110	8 M	9	110	8 M	1
0111	16 M	8	111	16 M	0
1000	32 M	7			
1001	64 M	6			
1010	128 M	5			
1011	256 M	4			
1100	512 M	3			
1101	1 G	2			
1110	2 G	1			
1111	4 G	0			

Table 3-8 Slave configuration register

3.3.4.3 Slave address register

The slave address register defines the address selection and generation of the slave interface. The register is set to 00000000H during reset.

29 22	21 15	14 7	6 0
N/U	LMA[6:0]	N/U	SA[6:0]

SA : slave address

LMA : local address (most significant part)

Table 3-9 Slave address register

3.3.5 Mailboxes and system status register

3.3.5.1 General

The four mailboxes provide a mean for inter-processor communication over the VME bus. Each mailbox consist of a 16- bit register mapped into the short VME address space (A16). The mailbox registers can be accessed with A16/D8/D16 transfers. The mailbox configuration register controls the operation of the mailboxes. The mailbox address field (MBA) defines at which address the mailboxes appear in address space, aligned at 256-byte blocks. The SU and NP bits enable supervisor (AM = 0x2D) and non-privileged (AM=0x29) access. Interrupts can optionally be generated to the local processor when the individual mailboxes are read or written. The RI field

enables interrupt generation after the mailbox has been read while the WI field enables interrupt generation after write. Pending mailbox interrupts can be read from the Interrupt status register. A mailbox interrupt is cleared when the local processor reads or writes the corresponding mailbox register.

17	16	15 8	7 4	3 0
NP	SU	MBA[7:0]	WI[3:0]	RI[3:0]

RIn : enable read access interrupt for mailbox n

WIn : enable write access interrupt for mailbox n

MBA : mailbox start address(256-byte block)

SU : enable supervisor access (1M=0x2D)

NP : enable non-privileged access (AM=0x29

A16 address	Register
0000	Mailbox 0
0002	Mailbox 1
0004	Mailbox 2
0006	Mailbox 3
0008	System Status

Table 3-10 Mailbox configuration register

3.3.5.2 VME status register

The VME status register is readable from the VME bus and contains two status bits from the local ERC32 system. It is mapped at address 0x8 (A16/D8/D16) directly after mailbox register 3.

1	0
MR	SA

SA : DSP SYSAV pin

MR : MRSTIN pin

Table 3-11 System Reset register

3.3.6 Interrupt handling

3.3.6.1 Interrupt controller

The EVI32 contains an interrupt controller that generates two local interrupts to the DSP, LIRQ0 and LIRQ1 (individually connected to ExtIT[i]). The two local interrupts are generated by the interrupt controller from 13 internal sources. Table7 shows the interrupt allocation. The two local interrupts are asserted as long as any pending

interrupts are present, the corresponding DPC interrupts should therefore be programmed level-sensitive for correct operation.

Interrupt #	Interrupt source
13	ACFAIL
12	Mailbox 3
11	Mailbox 2
10	VME interrupt 7
9	VME interrupt 6
8	VME interrupt 5
7	VME interrupt 4
6	SYSFAIL
5	Mailbox 1
4	Mailbox 0
3	VME interrupt 3
2	VME interrupt 2
1	VME interrupt 1

Table 3-12 Interrupt numbering

The interrupt level for each interrupt is programmed in the interrupt configuration register.

25 13	12 0
IL[13:1]	IE[13:1]

IEn : interrupt enable for interrupt n (0=disabled, 1= enabled)

ILn : interrupt level for interrupt n (0=level 0: LIRQ0 driven, 1= level 1; LIRQ1 driven)

Table 3-13 Interrupt configuration register

The status of pending interrupts can be read from the interrupt status register.

24 21	20 17	16 13	12 0
PGI[3:0]	MI1[3:0]	MI0[3:0]	PI[13:1]

PIn : pending interrupt n

MI0 : highest priority pending interrupt in level 0

MI1 : highest priority pending interrupt in level 1

PGIn : pending generated VME interrupt n

Table 3-14 Interrupt status register

3.3.6.2 VME interrupt handler

The VME interrupt handler can handle all seven VME interrupts. The handling of a VME interrupt is enabled by enabling the corresponding bit in the interrupt configuration register. When an interrupt is detected, the corresponding interrupt pending bit is set in the interrupt status register and a local interrupt is generated to the DSP. To acknowledge the VME interrupt, an interrupt acknowledge cycle needs to be performed to read the interrupter's STATUS/ID. This is done by doing a read cycle with DMA[21] equal to '1' to an arbitrary location in IO area 3. The read value contains the STATUS/ID of the interrupter that generated the interrupt. During the interrupt acknowledge cycle, address bits 4 - 2 of the local address bus are used to generate bits 3 - 1 of the VME address bus and are used to identify which interrupt is being acknowledged. The following sequence shows how a VME interrupt is handled:

- A VME interrupt is generated by asserting VIRQOUT.
- A local DSP interrupt is generated by asserting LIRQ.
- DSP takes an interrupt trap, disabling further interrupts (at this level).
- The DSP interrupt routine reads the EVI32 status register to identify the pending interrupt.
- The DSP interrupt routine generates a VME interrupt acknowledge cycle by reading the right address. At this point, any VME ROAK interrupts will de-assert VIRQOUT.
- The DSP interrupt routine will read the interrupting device's register. At this point, any RORA interrupts will de-assert VIRQOUT.

It should be noted that for RORA interrupts, the interrupt service routine must allow at least 2 ms between the last step above and re-enabling of the corresponding EVI32 interrupt (VME specification rule 4.8).

A D08 interrupt acknowledge cycle must be performed with the least significant bit (A0) of the DSP address equal to one, since D08 interrupters respond only to DS(0).

If the VME acknowledge cycle is terminated with a bus error (BERR asserted), then the DSP load cycle will be terminated with BUSERR (connected to ExtIT[i]) asserted.

3.3.6.3 VME interrupter

The interrupter is capable of generating four VME interrupts. Interrupts are generated by writing to the Interrupt command register. Monitoring of generated interrupts is done through the interrupt status register. The VME STATUS/ID for each of the generated interrupts is programmed in the Interrupt identification register and is 7 bits long for VME interrupts 2 - 7, and 8 bits for VME interrupt 1. The VME interrupt number of a generated interrupt is defined by the interrupt select (IS) bits in the interrupt identification register. Pending generated interrupts (not yet acknowledged) can be cleared by writing to the interrupt command register. When a generated interrupt is acknowledged through a VME interrupt acknowledge cycle, the interrupter responds with the STATUS/ID, clears the pending bit and releases the interrupt line. This corresponds to a VME ROAK interrupter.

The interrupter will only respond to an interrupt acknowledge cycle when a generated interrupt is pending for that interrupt. The interrupter will respond to D8/D16/D32 acknowledge cycles, but only provide the least significant 7/8 bits. The remaining data bits will be high, as specified in the VME specification (AD4).

3.3.6.4 Interrupter identification register

The interrupt identification register contains the STATUS/ ID value for each generated interrupt. The register is set to 00000000H during reset.

31	30 24	23	22 16	15	14 8	7 0
IS3	ID3[6:0]	IS2	ID2[6:0]	IS1	ID1[6:0]	ID0[7:0]

ID0[6:0] : STATUS/ID code for generated interrupt 0 (VME irq# 1)

ID1[6:0] : STATUS/ID code for generated interrupt 1 (VME irq# 2/3)

ID2[6:0] : STATUS/ID code for generated interrupt 2 (VME irq# 4/5)

ID3[6:0] : STATUS/ID code for generated interrupt 3 (VME irq# 6/7)

ISn : Isn = 0 generates even VME interrupt, else odd

Table 3-15 Interrupt identification register

3.3.6.5 Interrupt command register

The interrupt generate register is a write-only register used to generate and clear interrupts.

9	8	7 4	3 0
CS	CA	CI[3:0]	GI[3:0]

GIn : generate interrupt Idn

CIn : clear pending generated interrupt IDn

CA : clear ACFAIL interrupt

CS : clear SYSFAIL interrupt

Table 3-16 Interrupt command register

3.3.7 System status register

The system status register indicates the bus error cause and the status of some VME signals. A write to this register will only affect the RBE, SBE and MBE fields.

16 15	14	13 11	10	9	8	7	6 0
RBE	SBE	MBE[2:0]	SC	0	AC	SF	VIRQ[7:1]

VIRQn : complemented value of VME IRQn signal

AC : complemented value of ACFAIl signal

SF : complemented value of SYSFAIL signal

SC : value of SCON signal

MBE : bus error related to master access (ERC32 or VME)

SBE : bus error caused by slave : VME access to own slave area

RBE : bus error caused by register access

MBE[2:0]	Master Bus error cause
000	No error
001	VME bus grant not received (time-out 1)
010	Unused
011	Master/slave access conflict (try again)
100	Unused
101	VME access terminated with BUSERR
110	Unused
111	Unused
RBE[1:0]	Register Bus error cause
00	No error
01	Wrong write in register (size error)
10	Access to non-existing EVI32 register
11	Both previous error cases

Table 3-17 EVI32 status register

3.3.8 VME system controller functions

The arbiter, bus timer and IACK daisy-chain driver are only enabled if EVI32 acts as a system controller (when the SCON input is asserted).

3.3.8.1 Arbiter

The arbiter is a single level (SGL) arbiter as defined in the VME specification. To improve latency, bus parking can be enabled by setting the RR bit in the master configuration register, which will keep BBSY asserted between consecutive accesses until there is a bus request from another master.

3.3.8.2 Bus timer

A VME bus timer is provided in the EVI32. It consists of an 8-bit counter clocked by the system clock. The timer is reset and started when VASIN is asserted, indicating a bus access. If DTACK is not asserted before the counter reaches 248, BERR is asserted, indicating a bus error. During block transfers, the counter is reset after each DTACK.

3.3.8.3 IACK daisy-chain driver

The IACK daisy-chain driver generates a falling edge on the IACKOUT output when any interrupt handler on the VME bus acknowledges an interrupt.

3.3.9 Reset operation

3.3.9.1 General

EVI32 has three reset inputs; power-on reset (PRST), MEC reset (MRSTIN) and VME reset (SYSRESETIN). Two reset outputs are provided, one for the DPC (MRSTOUT) and one for the VME bus (SYSRESET).

EVI32 is internally reset when any of the following conditions are true:

- the MRSTIN input is asserted and the MRSTOUT output is not asserted;
- the PRST input is asserted;
- the SYSRESETIN input is asserted while the SR bit in the system reset register has the value zero (see section 2.3.9.2);
- the ER bit in the system reset register is set to the value 1 (in this case, neither SYSRESET nor MRTSOUT is asserted). This can for example be used after a hardware error has been detected, or similar.

During the internal EVI32 reset, all registers are cleared to their default zero values and all outputs (except the MRSTOUT output) are placed in their inactive state.

The MRSTOUT output is asserted on any of the following conditions:

- the PRST input is asserted;
- the SYSRESETIN input is asserted while the SR bit in the system reset register has the value 0 (see section 2.3.9.2).

The VME SYSRESET output is asserted on any of the following conditions:

- the PRST input is asserted;
- SR bit in the system reset register is set to the value 1 while the SCON input is being asserted;

If the VME SYSRESET is generated by setting the SR bit in the system reset register the minimum assertion time of 200ms for the SYSRESET signal (as per AD4) must be controlled via software.

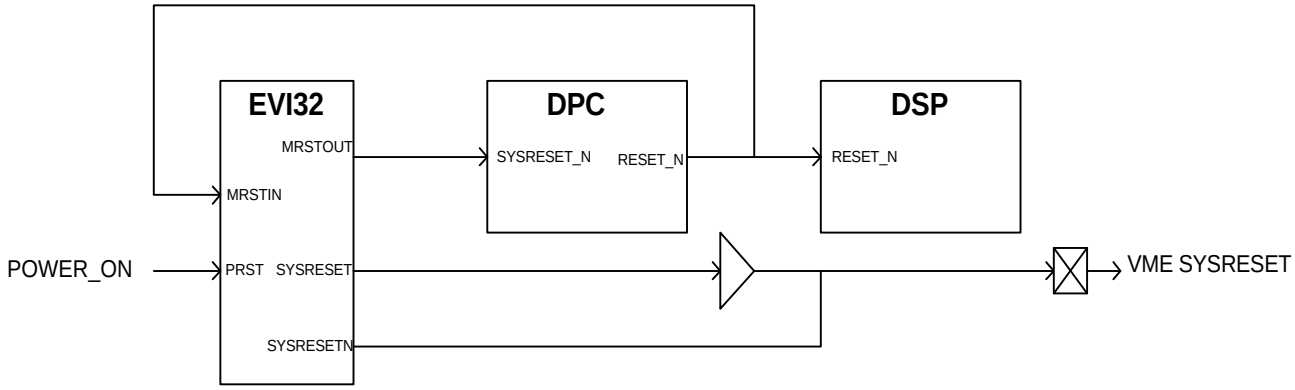


Figure 3-5: Reset management

3.3.9.2 System reset register

The system reset register is used to either generate VME SYSRESET or to reset EVI32. The PO bit can be written with any value, but will only be reset when PRST is asserted.

2	1	0
PO	ER	SR

SR : generate VME SYSRESET (see section 2.3.9.1)

ER : reset EVI32 (see section 2.3.9.1)

PO : cleared on power-on-reset

Table 3-18 VME status register

3.3.9.3 Register reset values

All EVI32 registers are cleared to `all zeros' during reset.

3.3.10 Error detection

The EVI32 uses SEU hardened D flip-flop internally. Thus no parity protection is provided on internal registers, and no hardware error signal is output.

EVI32 does not generate or check parity for DPC/DSP.

3.4 EVI32 SIGNAL DESCRIPTION

3.4.1 EVI32 signal summary

Table 2-19, Table 2-20, Table 2-21 and Table 2-22. provide the signal summary of EVI32.

Name	Type	Function	Active polarity
LA[31:0]	Bidir	Address bus (un-latched)	High
DMAAS	Tristate output	DMA address strobe	High
LD[31:0]	Bidir	Data bus	High
DPAR	*Bidir*	*Not used. Forced as an input*	*High*
ALE	*Input*	*Not used*	*Low*
ASI[3:0]	Bidir	Access type selection. Forced as an input.	Low
SIZE[1:0]	Bidir	Size of the access. Forced as an input.	High
RD	Bidir	Read strobe for master accesses. Forced as an input	Low
WRT	Bidir	Write strobe for master accesses. Forced as an input	Low
LOCK (RDY)	Output	Active high ready for master accesses. Forced as an output	High
WE	Output	Write strobe for slave accesses. High Z level otherwise.	Low
LOAD(LDSTO)	Tristate output	Read strobe for slave accesses. High Z level otherwise	Low
DXFER	*Tristate output*	*Not used*	*High*
DMAREQ	Output	DMA bus request	Low
DMAGNT	Input	DMA bus grant	Low
DRDY	*Input*	*Not used*	*Low*
MEXC	*Input*	*Not used*	*Low*
BUSRDY	Output	Active low ready for master accesses	Low
BUSERR	Output	Bus error	Low
IRQ[1:0]	Output	Local interrupt	Low
RSEL	*Input*	*Not used*	*Low*
IOBENIN	*Input*	*Not used*	*Low*
DDIRIN	*Input*	*Not used*	*Low*
DDIROUT	*Output*	*Not Used*	

Table 3-19 DSP/DPC interface

Name	Type	Function	Active polarity
CLK	Input	DPC CLKOUT	High
PRSTN	Input	Power-on reset	Low
MRSTIN	Input	Reset input (connect to DPC RESET)	Low
MRSTOUT	Output	Reset output (connect to DPC SYSRESET)	Low
ASPAR	Tristate output	*Not used*	*High*
APAR	Tristate output	*Not used*	*High*
IMPAR	Tristate output	*Not used*	*High*
NOPARN	Input	Disable parity generation. Must be forced to low state	Low
SYSAV	Input	System available	High
SEL16	Input	Enable accelerated 16 bit access	High
INULL	*Input*	*Not used*	*High*

Table 3-20 DSP/DPC interface (con't)

Name	Type	Function	Active polarity
VASIN	Input	Address stable	Low
VASOUT	Output	Address stable	Low
DSIN[1:0]	Input	Data strobes	Low
DSOUT[1:0]	Output	Data strobes	Low
ACFAIL	Input	Power failure	Low
SYSFAIL	Input	System failure	Low
SYSRESET	Output	System reset	Low
SYSRESETIN	Input	System reset	Low
BBSY	Output	Bus busy	Low
BBSYIN	Input	Bus busy	Low
BERR	Output	Bus error	Low
BERRIN	Input	Bus error	Low
DTACK	Output	Data acknowledge	Low
DTACKIN	Input	Data acknowledge	Low
VIRQIN[7:1]	Input	Interrupts	Low
VIRQOUT[3:0]	Output	Interrupts	Low
A[31:1]	Bidir	Address bus	High
D[31:0]	Bidir	Data bus	High
AM[5:0]	Bidir	Address modifier	High
IACK	Bidir	Interrupt acknowledge	Low
LWORD	Bidir	Long word	Low
WRITE	Bidir	Write strobe	Low
BG3IN	Input	Bus grant in	Low
IACKIN	Input	Interrupt ack in	Low
BG3OUT	Output	Bus grant out	Low
IACKOUT	Output	Interrupt ack out	Low
BR3	Output	Bus request	Low
BR3IN	Input	Bus request	Low
SCON	Input	System controller	Low

Table 3-21 VME interface

Name	Type	Function	Active polarity
ABEN	Output	VME address buffer enable	Low
ABDIR	Output	VME address buffer direction	Low
DBLEN	Output	VME data buffer enable (low 16 bits)	Low
DBHEN	Output	VME data buffer enable (high 16 bits)	Low
DBDIR	Output	VME data buffer direction	Low

Table 3-22:Buffer control

Name	Function		
VCC[10:0]	Power input		
GND[15:0]	Ground		

Table 3-23: Power pins

3.4.2 EVI32 detailed signal description

3.4.2.1 Clock , reset and configuration signals

SYSCLK (input) – System Clock

This pin shall be connected to CLKOUT of the DPC. It is the master clock of the EVI32.

CONF[1:0] (input) – Configuration of EVI32

CONF pins are used to program EVI32 for ERCSC, ERC 3 chips, DSP/DPC configuration. CONF shall be set to "01" to configure EVI32 in ERC SC mode (CONF(1) is set to 0 and CONF(0) is set to 1). Other values are used to configure EVI32 either for DSP/DPC or ERC32 3C or in test mode. A wrong configuration may damage the chip.

PRSTN (input) – Power-on reset

Reset input activated at power up.

MRSTIN (input) – Reset input

This pin shall be connected to the DPC RESET signal.

MRSTOUT (output) – Reset output

This pin shall be connected to the DPC SYSRESET signal.

NOPARN – Parity disabled

This pin must be forced to ‘0’ because the parity generation and check is not used.

SEL16 – Enable accelerated 16 bit access (input)

This configuration pin enables accelerated 16 bit accesses on the VME bus. This pin has to be connected to DSP DMA(19) signal.

SCON – System Controller Enable (input)

This configuration pin configures the EVI32 in System Controller for the VME bus.

SYSAV - System Availability (input)

This pin shall be connected to the SYSAV signal of the DPC. This signal is asserted as soon as the system is available.

3.4.2.2 DSP/DPC interface

LA[31:0] - Address Bus (bi-directional)

These pins shall be connected to the address bus of the DSP through external buffers (connection to DMA for master accesses and to PMA for slave accesses). The address bus is generated by the DSP in normal mode. In DMA mode this bus must be driven by the EVI32.

ASI[3:0] - Address Space Identifier (bi-directional)

IOSel_N(0) is connected to ASI(0), IOSel_N(1) to ASI(1) and IOSel_N(2) to ASI(2). DSP DMA(21) is connected to ASI(3).

SIZE[1:0] - Bus Transaction Size (bi-directional)

These pins indicates the size of the transfer during Master accesses. They have to be connected to DPC DMA[20:19].

DL[31:0] - Data Bus (bi-directional)

These pins shall be connected to the data busses of the DSP core through external buffers (connection to DMRMD bus for master accesses and to PMD bus for slave accesses). These pins form a 32-bit bi-directional data bus that serves as the interface between the DSP core and the EVI32. It is driven by the EVI32 only during read of its internal registers and when making read accesses on the VME bus. In case of Direct Memory Access, it is driven or read by EVI32.

APAR - Address Bus Parity (tristate output)

Not Used.

ASPAR - ASI and SIZE Parity (tristate output)

Not Used.

IMPAR – Control Signal Parity (tristate output)

Not Used.

DPAR - Data Bus Parity (bi-directional)

Not Used.

RD – Master Read Access (bi-directional)

This pin shall be connected to the UERD_N signal of the DPC for master read accesses.

ALEN - Address Latch Enable (input)

Not Used.

RSELN – Register Select (input)

Not Used.

IOBENIN - IO Buffer Enable (input)

Not Used.

IOBENOUT - IO Buffer Enable (output)

Not Used.

BUSRDYN - Bus Ready (output)

This pin shall be connected to the UERDY3_N signal of the DPC. BUSRDYN is generated by the EVI32 at the end of a master access.

BUSERRN - Bus Error (output)

This pin shall be connected to an IT signal (ExtIT(i)_N or IRQj_N) of the DSP core. BUSERRN is generated together with BUSRDYN by the EVI32 if an error is detected during a master access.

LOCK (RDY) –Bus Ready (bi-directional)

This pin shall be connected to the UERDY2 signal of the DPC. BUSRDYN is generated by the EVI32 at the end of a master access.

WRT – Master Write Access (bi-directional)

This pin shall be connected to the UEWR_N signal of the DPC for master write accesses

IRQ[1:0] – Local Interrupt Request(output)

This pin shall be connected to an IT signal (ExtIT(i)_N or IRQj_N) of the DSP core. These 2 signals are two local interrupts to the DSP.

The following signals of the DSP/DPC interface of the EVI32 are only used when DMA mode is activated.

DMAAS - DMA Address Strobe (tristate output)

This pin shall be connected to the PMSi_N signal of the DSP through an external buffer. During DMA transfers (when the EVI32 is bus master) this output is used to inform the DPC that the address from the DMA is valid and that the access cycle shall start. DMAAS can be asserted multiple times during DMA grant.

DMAREQN - DMA Request (output)

This pin shall be connected to the Bus Request signal of the DSP core. DMAREQN is to be issued by the EVI32 when requesting the access to the processor bus as a master.

DMAGNTN - DMA Grant (input)

This pin shall be connected to the Bus Grant signal of the DSP core. DMAGNT* is generated by the DSP as a response to a DMAREQN.

DDIRIN - IO Buffer Direction In (input)

Unused

DDIROUT - IO Buffer Direction Out (output)

Unused

DRDYN - Data Ready during DMA access (input)

Not Used.

INULL - Integer Unit Nullify Cycle (input)

Not Used.

DXFER - Data Transfer (tristate output)

Not Used.

LOAD(LDSTO) – Slave Read Access (tristate output)

This pin shall be connected to the PMRD_N signal of the DSP directly or through external buffer. This signal is used during slave read accesses.

WEN – Slave Write Access (tristate output)

This pin shall be connected to the PMWR_N signal of the DSP directly or through external buffer. This signal is used during slave write accesses.

3.4.2.3 VME signal interface

Please refer to section 2.4.2.3 for VME signal description

3.5 CHARACTERISTICS

3.5.1 Electrical interfaces

3.5.1.1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Vdd	Supply voltage	-0.5	6	V
Vi	Input voltage	-0.5	Vdd + 0.5V	V
Ts	Storage temperature	-65	150	°C
Tj	Maximum junction temperature		165	°C
Rqjc	Thermal resistance		10	°C/W

3.5.1.2 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Supply voltage	4.5	5.0	5.5	V
To	Operating temperature	-55	25	125	°C
Vi	Input Voltage	0	Vdd	Vdd	V
Vo	Output Voltage	0	Vdd	Vdd	V

3.5.1.3 DC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Vil	Input low voltage			0.8	V
Vih	Input high voltage		2.2		V
Vol	Output voltage low level	Vdd = Min Iol = 3 mA		0.4	V
Voh	Output voltage high level	Vdd = Min Ioh = -3 mA	2.4		V
Ioz	Output leakage current	Vdd = Max 0 ≤ Vout ≤ Vdd	-5	5	uA
Iiz	Input leakage current	Vdd = Max 0 ≤ Vin ≤ Vdd	-5	5	uA
Isc	output short circuit current (one output at a time during 1s max)	Vdd = Max Vout = 0v		48	mA
Iccop1	Dynamic Supply current for array	Vdd = Max f = 25MHz		50	mA
Iccop0	Dynamic Supply current for buffers	Vdd = Max f = 25MHz		60	mA
Iccsb1	Static power consumption for array	Vdd = Max		35	uA
Iccsb0	Static power consumption for buffers	Vdd = Max		25	uA

3.5.1.4 Capacitance ratings

Parameters	Description	Max (pF)
Cin	Input capacitance	5
Cout	Output capacitance	7
Cio	Input/output bus capacitance	10

3.5.1.5 AC characteristics

The following markers are used in the chronograms to reference timing values :

- Master configuration :
  - E1 : rising edge of CLK that precede BBSY falling edge
  - E2 : rising edge of CLK for which DTACKIN has been sampled low for the first time

- Slave configuration :
  - H1 : falling edge of CLK used by ERC to generate DRDY
  - H2 : rising edge of CLK for which DS* has been sampled high at the end of the access

ref	parameter	symbol	min	max
c1	CLK period	T	66,66 ns	
f	CLK frequency	F = 1/T		15 MHz

ref	I/F	pin	dir	type	ref edge	min	max
EVI REGISTER INTERFACE							
r1	DSP	LA	in	setup time	CLK+	11,5	
r2	DSP	LA	in	hold time	CLK+	0	
r3	DSP	LD	in	setup time	CLK+	3,1	
r4	DSP	LD	in	hold time	CLK+	0	
r5	DSP	RD WRT	in	setup time	CLK+	8,8	
r6	DSP	RD WRT	in	hold time	CLK+	0	
r7	DSP	ASI(1)	in	setup time	CLK+	10,5	
r8	DSP	ASI(1)	in	hold time	CLK+	0	
r9	DSP	BUSDRY	out	output delay	CLK+		24,5
r10	DSP	RSEL to LD invalid	out	output delay	RSEL -	0	
r11	DSP	RSEL to LD valid	out	output delay	RSEL +		24
r12	DSP	LD	out	hold time	CLK+		0
r13	DSP	RSEL to LD Hi-Z	out	output delay	RSEL +		24
r14	DSP	VIRQOUT	out	output delay	CLK+		21,3
EVI VME MASTER INTERFACE - SINGLE WRITE							
m1	DSP	LA	in	setup time	CLK+	11,5	
m2	DSP	LA	in	hold time	CLK+	0	
m3	DSP	LD	in	setup time	CLK+	3,1	
m4	DSP	LD	in	hold time	CLK+	0	
m5	DSP	ASI	in	setup time	CLK+	11	
m6	DSP	ASI	in	hold time	CLK+	0	
m7	DSP	RD	in	setup time	CLK+	8,8	
m8	DSP	RD	in	hold time	CLK+	0	
m9	DSP	WRT	in	setup time	CLK+	8,4	
m10	DSP	WRT	in	hold time	CLK+	0	
m14	DSP	E1 to VASOUT	out	output delay	E1 CLK+	2T	2T + 21,4
m15	DSP	E2 to VASOUT	out	output delay	E2 CLK+	3T	3T + 21,4
m16	DSP	E1 to DSOUT	out	output delay	E1 CLK+	3T	3T + 21,0
m17	DSP	E2 to DSOUT	out	output delay	E2 CLK+	1T	1T + 21,0
m18	DSP	E1 to AM	out	output delay	E1 CLK+	1T	1T + 25,8
m19	DSP	E2 to AM	out	output delay	E2 CLK+	3T	3T + 25,8
m20	DSP	E1 to LWORD	out	output delay	E1 CLK+	1T	1T + 25,1
m21	DSP	E2 to LWORD	out	output delay	E2 CLK+	3T	3T + 25,1
m22	DSP	E1 to WRITE	out	output delay	E1 CLK+	1T	1T + 25,1
m23	DSP	E2 to WRITE	out	output delay	E2 CLK+	3T	3T + 25,1
m26	DSP	E1 to VA	out	output delay	E1 CLK+	1T	1T + 27,8
m27	DSP	E2 to VA	out	output delay	E2 CLK+	3T	3T + 27,8
m28	DSP	E1 to VD	out	output delay	E1 CLK+	2T	2T + 22,0
m29	DSP	E2 to VD	out	output delay	E2 CLK+	3T	3T + 22,0
m30	DSP	ABDIR	out	output delay	CLK-		16
m32	DSP	ABEN	out	output delay	CLK+		23,9
m34	DSP	ASDSEN	out	output delay	CLK+		18,2
m36	DSP	DBDIR	out	output delay	CLK+		16,3
m38	DSP	DBHEN DBLEN	out	output delay	CLK+		17,9

ref	I/F	pin	dir	type	ref edge	min	max
EVI VME MASTER INTERFACE - SINGLE READ							
m40	DSP	LD	out	Hi-Z to Invalid	CLK+	0	
m41	DSP	LD	out	Valid to Hi-Z	CLK+		22
m42	DSP	VD to LD Valid	out	output delay	VD		20,9
EVI ARBITRATION							
a1	VME	BR3	out	output delay	CLK+		22,1
a2	VME	BR3(L) to BBSY(L)	out	output delay	BR3		1T + 3,0
a3	VME	BBSY	out	output delay	CLK+		21,4
a4	VME	BBSY(L) to BBSY(H)	out	duration	BBSY	4T	
a5	VME	BR3IN(L) to BG3OUT(L)	out	output delay	BR3IN		1T + 21,2
a6	VME	BR3IN(L) to BBSY(H)	out	output delay	BR3IN	1T + 0,0	
a7	VME	BG3IN(L) to BG3OUT(L)	out	output delay	BG3IN		2T + 21,2
EVI INTERRUPT MANAGEMENT							
i1	VME	IACKIN(L) to IACKOUT(L)	out	output delay	IACKIN		16,6
i2	VME	VRIQINx(L) to LIRQy(L)	out	output delay	VIRQIN		1T + 30,3
i3	VME	F1 to IACK(L)	out	output delay	E1 CLK+		1T + 25,7
i4	VME	F2 to IACK Hi-Z	out	output delay	E2 CLK+		4T + 25,7
EVI SLAVE INTERFACE							
s1	DSP	DMAREQ	out	output delay	CLK+		22,5
s2	DSP	DMAGNT	in	setup time	CLK+	6,7	
s3	DSP	DMAGNT	in	hold time	CLK+	0	
s4	DSP	LA LDSTO WE Hi-Z to Active	out	output delay	CLK-	0	
s5	DSP	LA LDSTO WE Active to Hi-Z	out	output delay	CLK-		27,9
s6	DSP	DMAAS low to high	out	output delay	CLK+		18,4
s7	DSP	DMAAS high to low	out	output delay	CLK+		18,4
s8	DSP	LDSTO WE	out	output delay	CLK+		23
s10	DSP	DTACK(L)	out	output delay	CLK+		21,5
s11	DSP	DTACK(H)	out	output delay	CLK+		21,5
s12	DSP	LD Hi-Z to Active	out	output delay	CLK+	0	
s13	DSP	LD Active to Hi-Z	out	output delay	CLK+		26,6
s19	VME	VD	out	setup time	DTACK-	1,5T + 0,8	
s20	VME	VD	out	hold time	DS+	1T + 17,2	
s21	DSP	LD	in	setup time	CLK-	4,8	
s22	DSP	LD	in	hold time	CLK-	0	

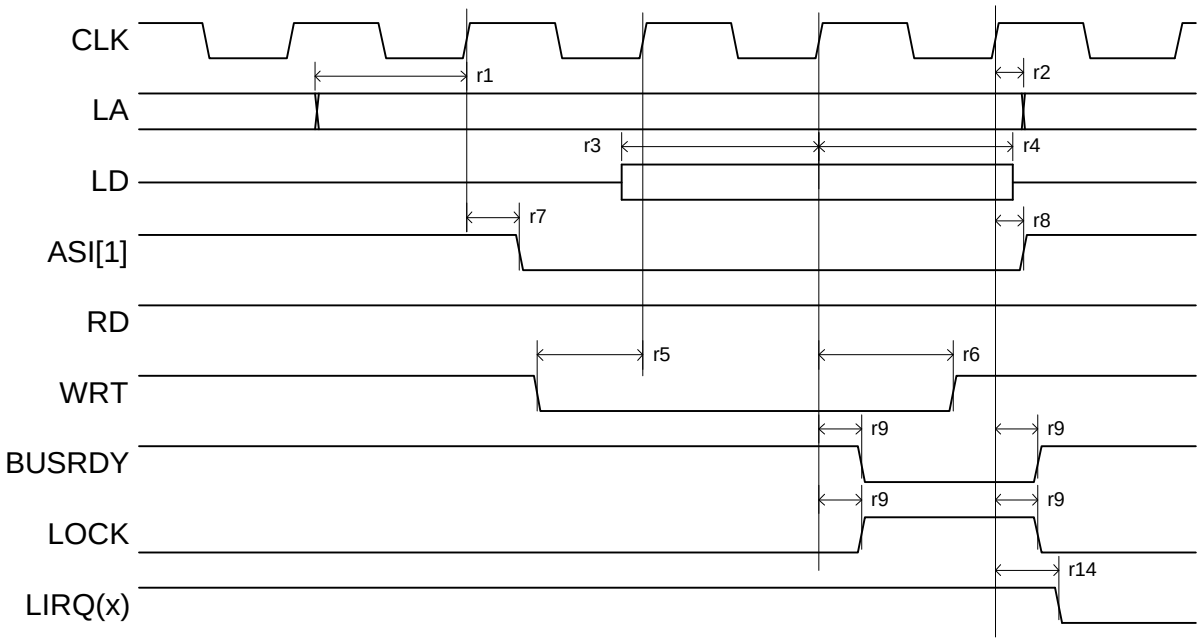


Figure 3.5-1 EVI Register write

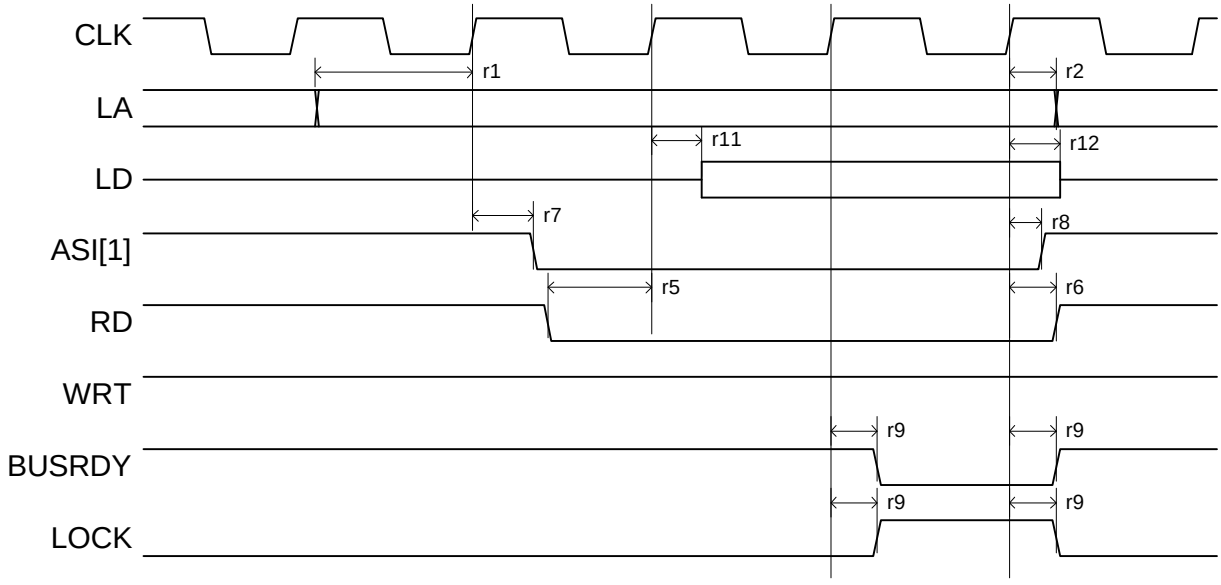


Figure 3.5-2 EVI Register read

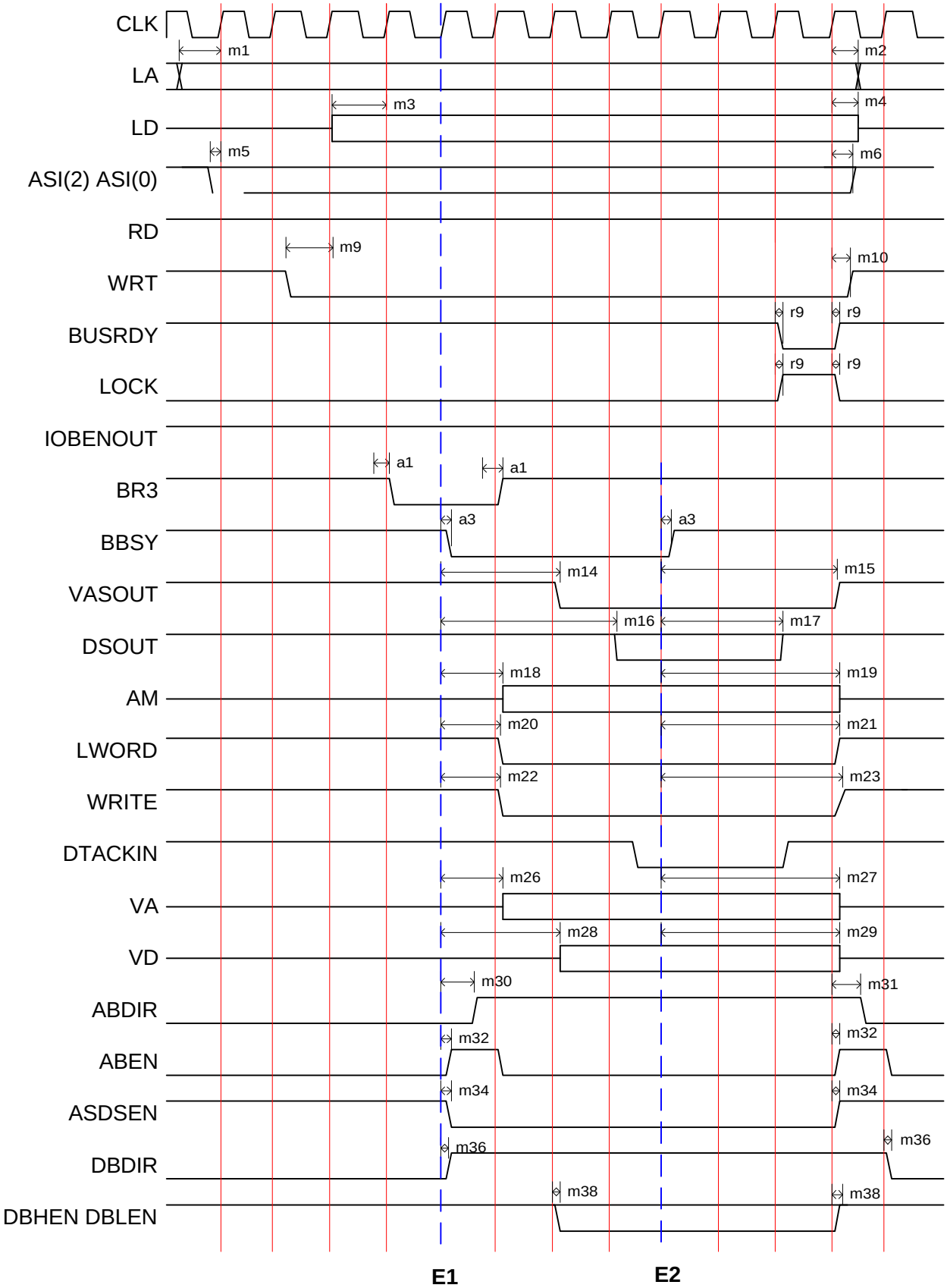


Figure 3.5-3 EVI Master : single access write

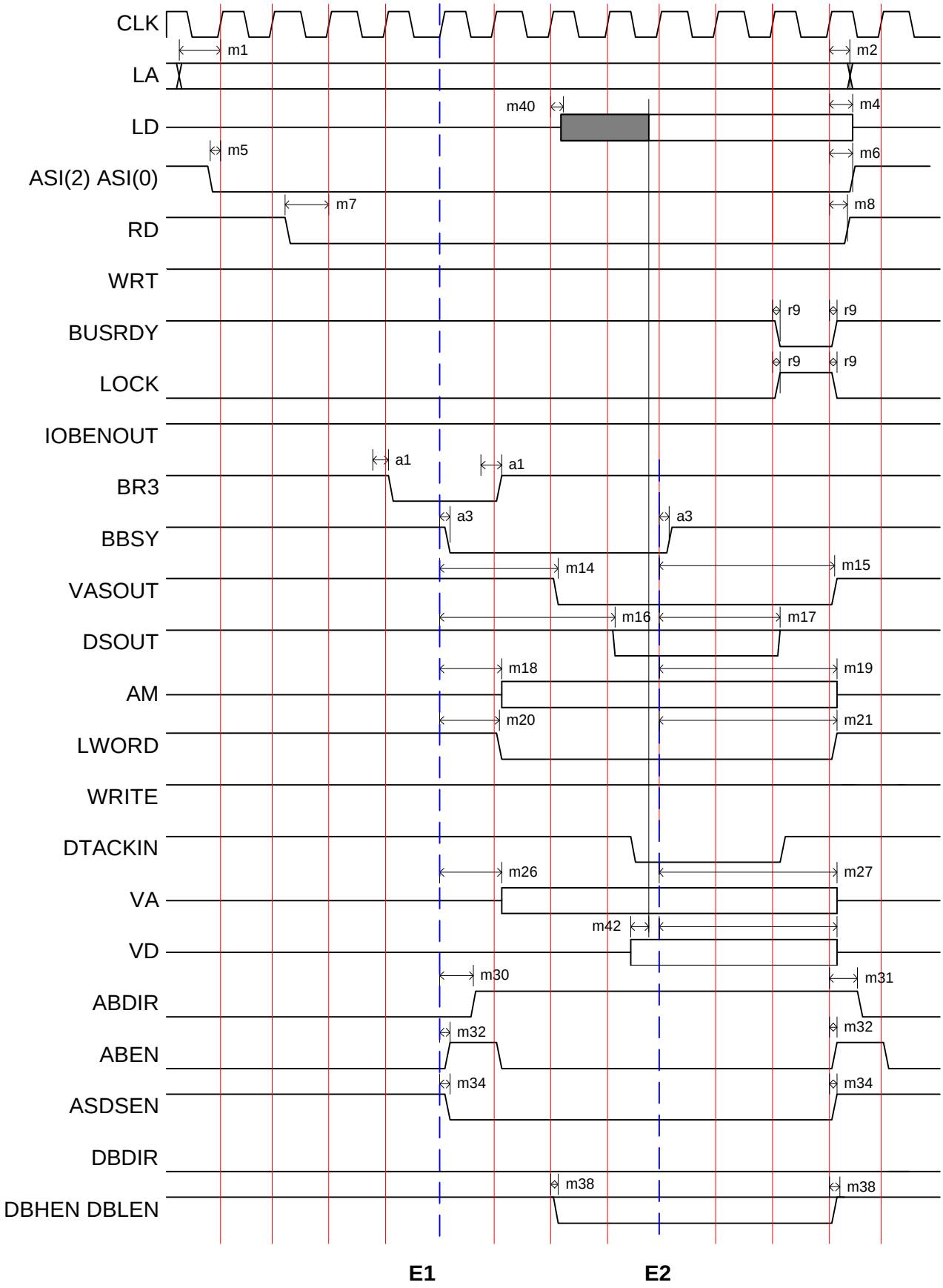


Figure 3.5-4 EVI Master : single access read

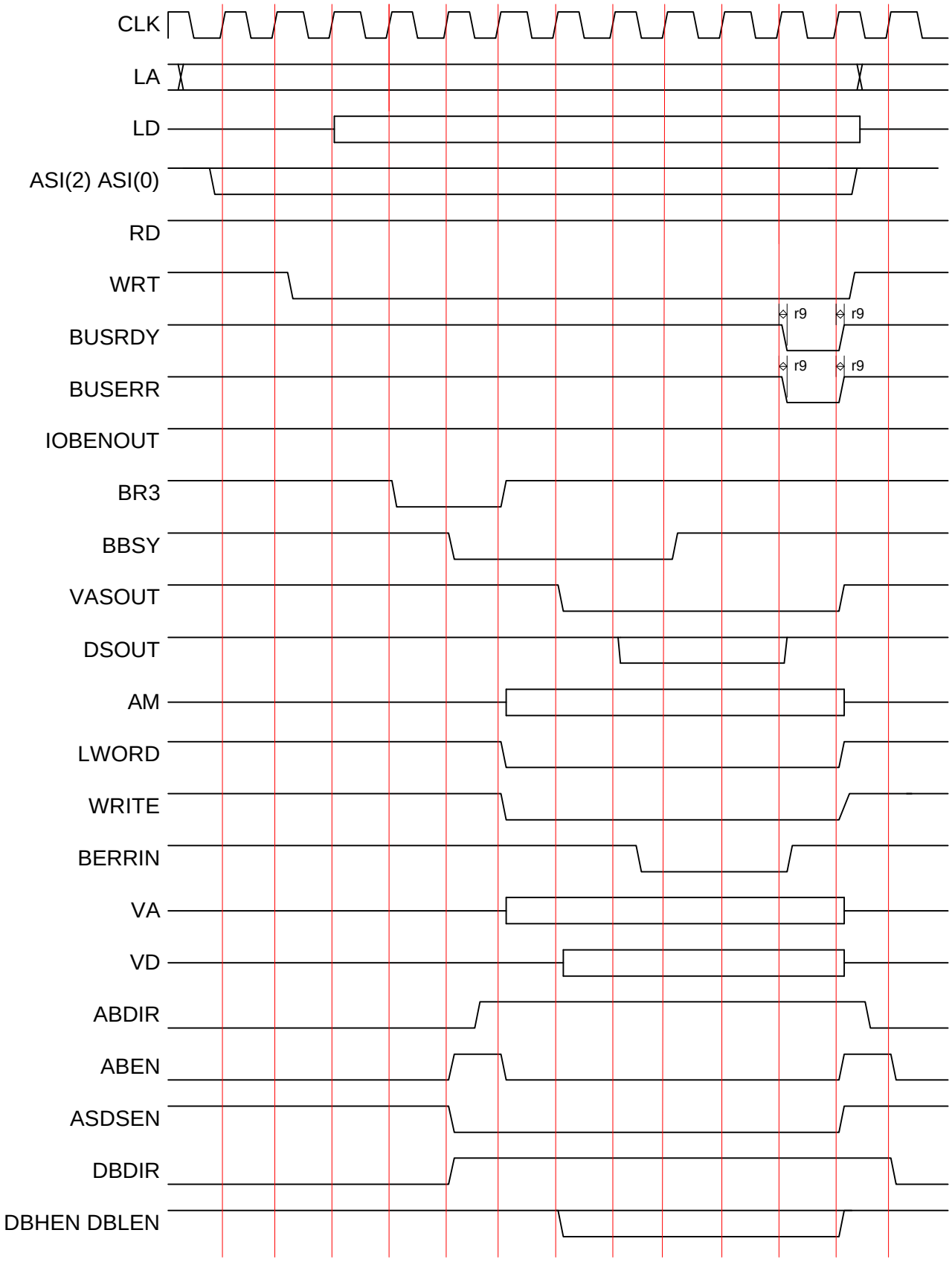


Figure 3.5-5 : EVI Master : access ending by a BERR

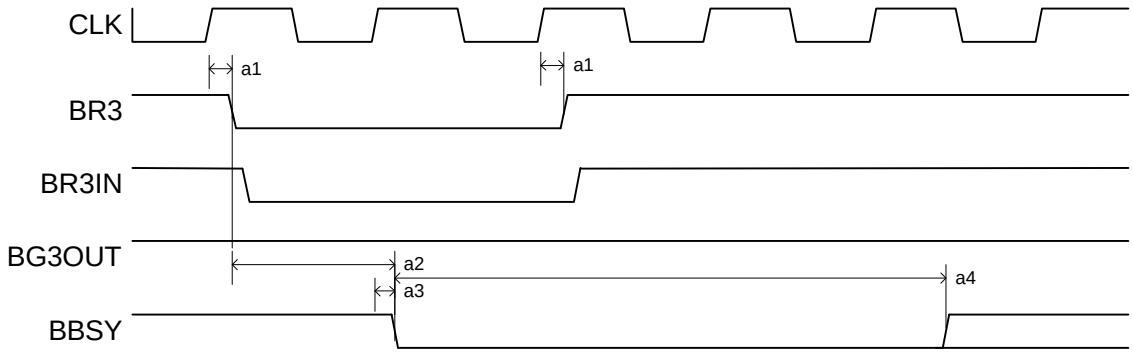


Figure 3.5-6 EVI Bus Arbiter and Bus Requester

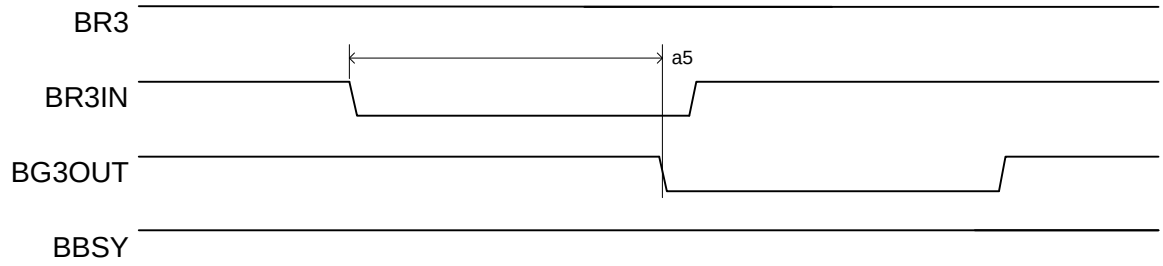


Figure 3.5-7 EVI Bus Arbiter - EVI32 as Arbiter initiating Arbitration daisy chain

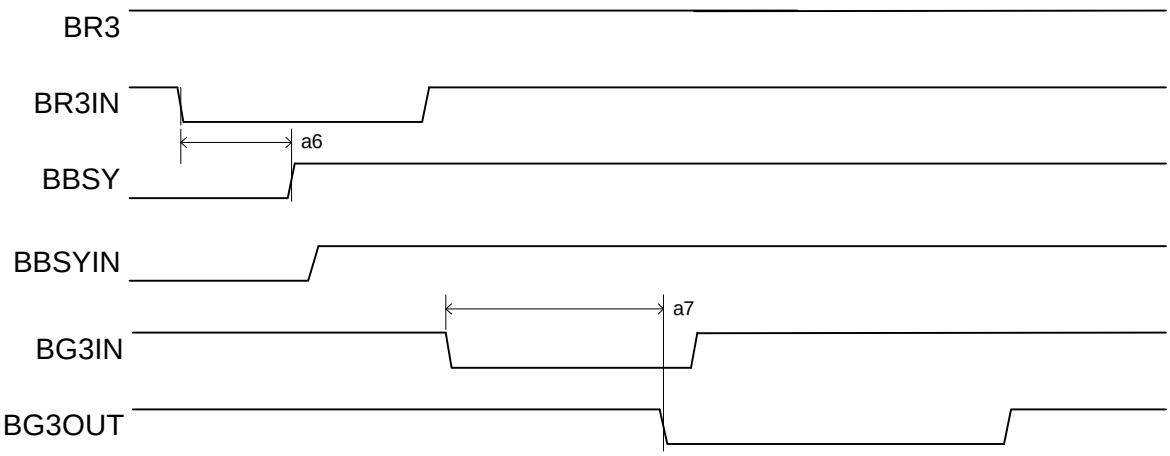


Figure 3.5-8 EVI32 not Arbiter - Daisy chain propagation

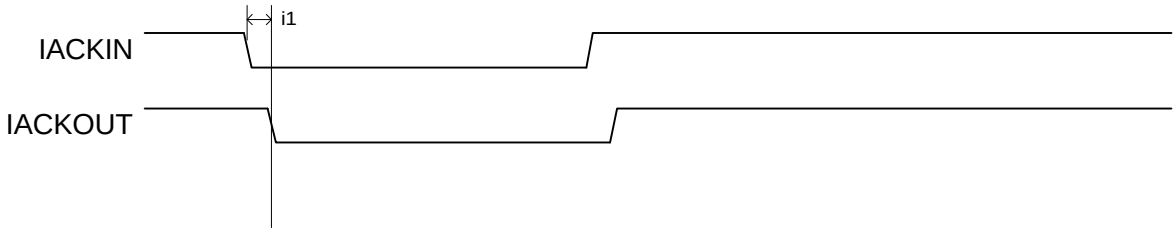


Figure 3.5-9 IACK daisy chain propagation

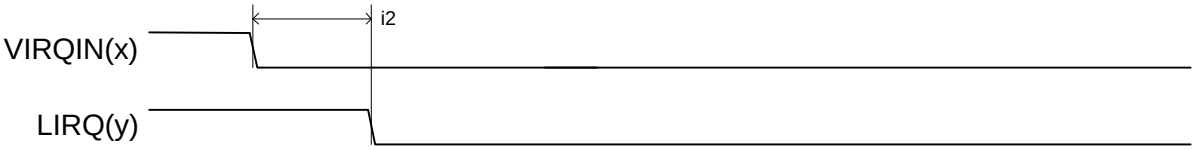


Figure 3.5-10 EVI Interrupt handler : VIRQ to LIRQ

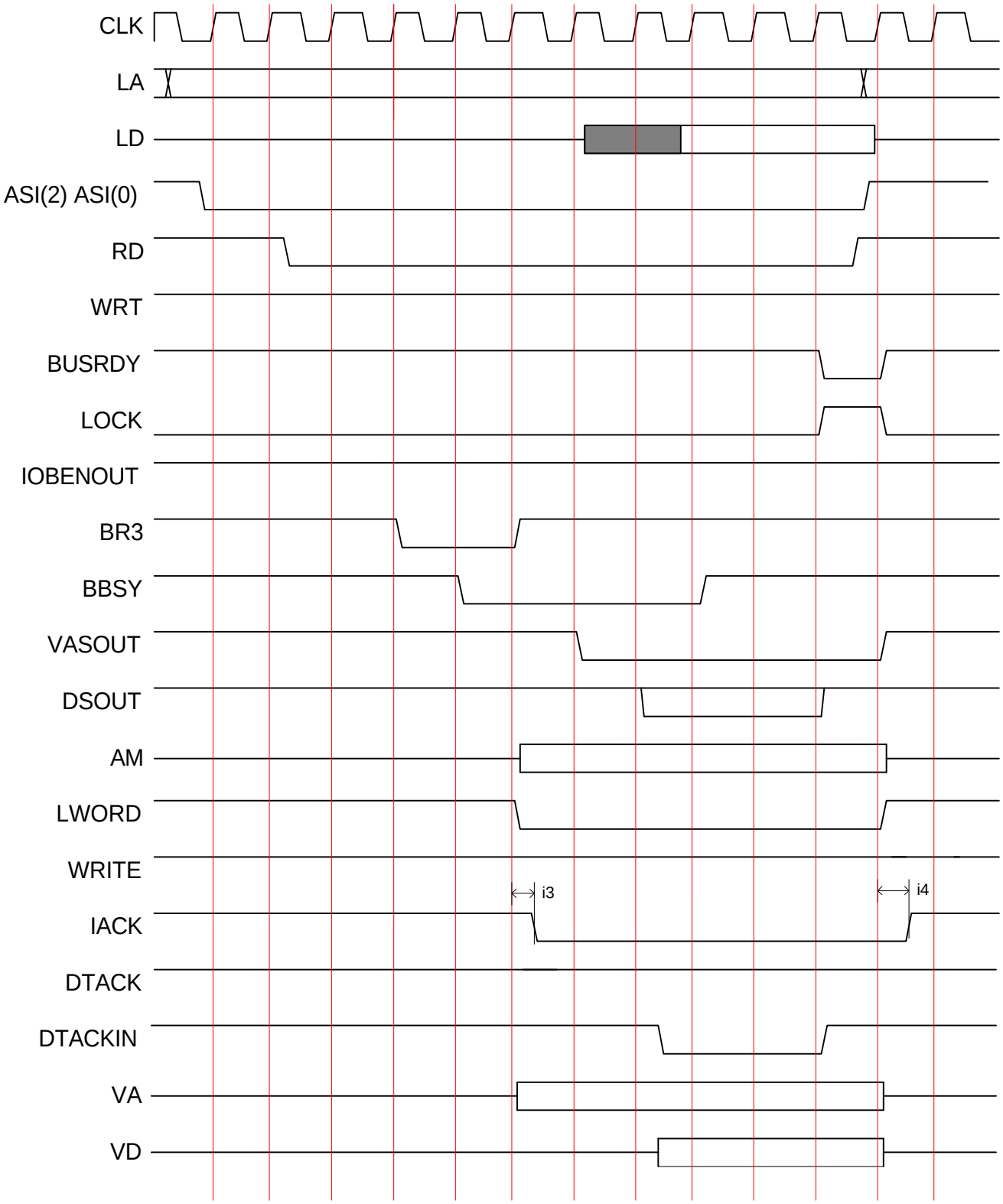


Figure 3.5-11 EVI interrupt acknowledge cycle

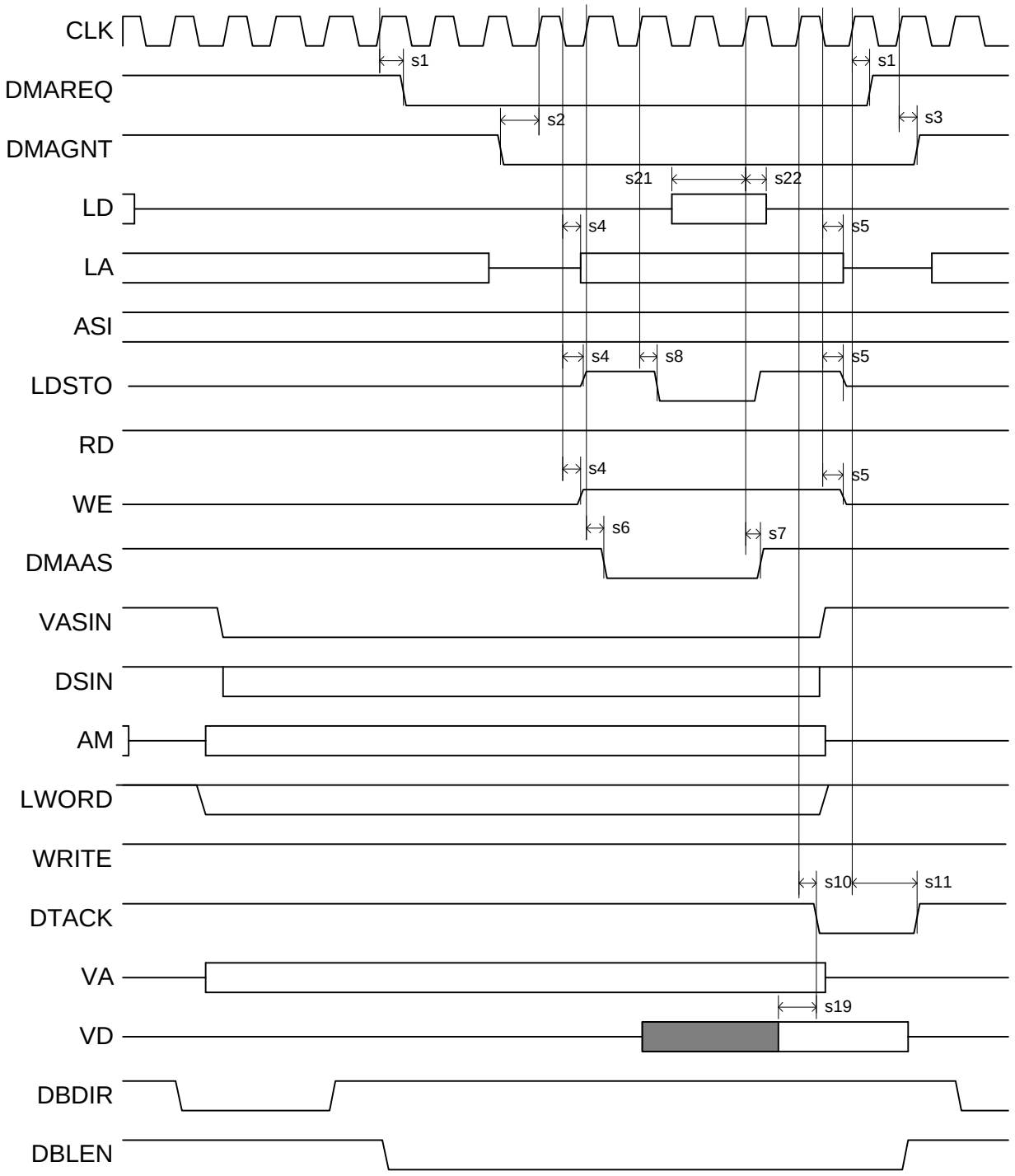


Figure 3.5-12 EVI slave : VME single read access

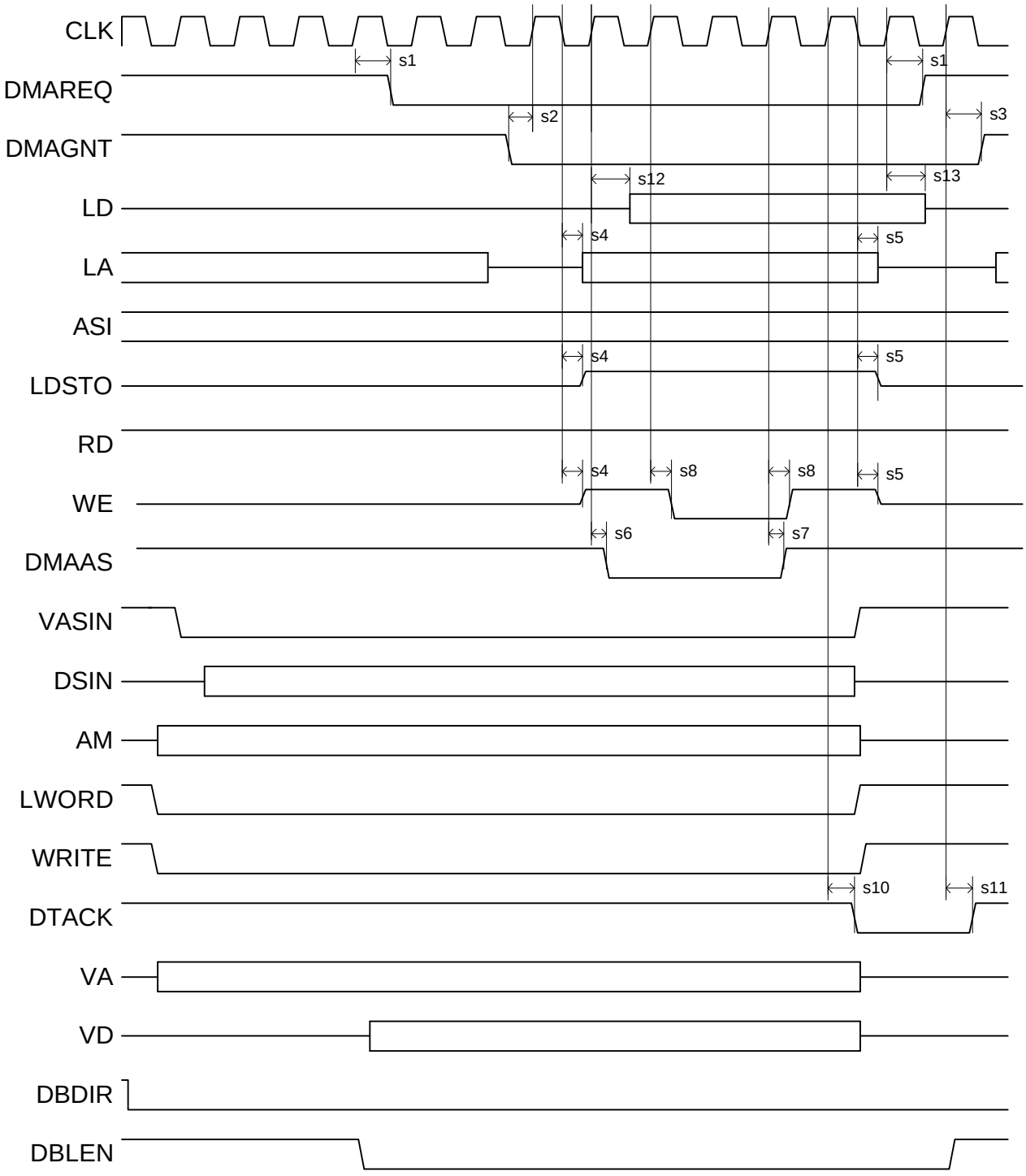


Figure 3.5-13 EVI slave : VME single write access

4. MECHANICAL INTERFACES

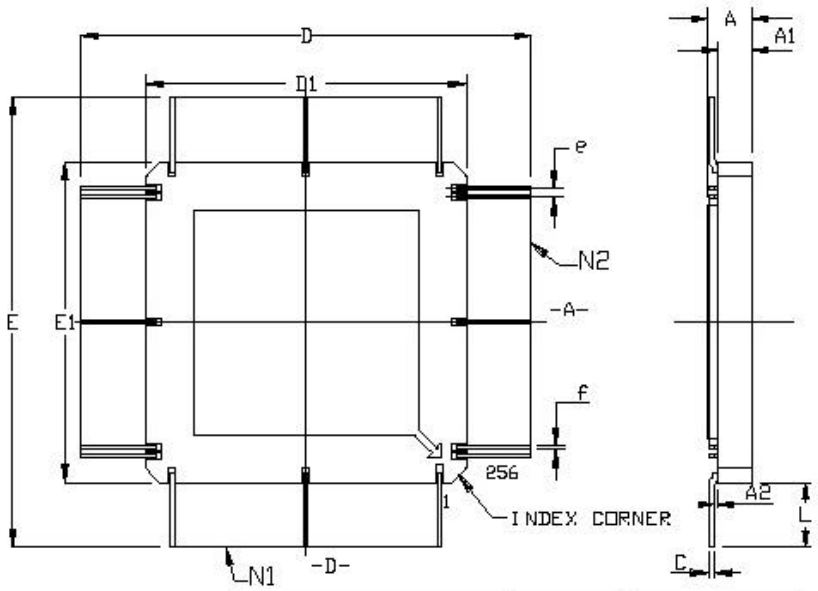
4.1 PACKAGING

The EVI32 is procured in a 256 pin ceramic package. The description of this package is provided hereafter.

TEMIC Semiconductors

Mechanical Data

256 LEAD MQFP_F



	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

PACKAGE CODE : U06N U16N U29N U36N U54N U66N U67N U69N
INTERNAL CODE : KZ
MHS S.A.
REV : H DATE : 15-06-99

4.2 PIN ASSIGNMENT

Signal	Buffer	Pin	Type	Signal	Buffer	Pin	Type
BVSS1	BVSSBENQ	1	VSB	VA[6]	BIOT3UP	129	I/O
LD[0]	BIOT3UP	2	I/O	VA[5]	BIOT3UP	130	I/O
LD[1]	BIOT3UP	3	I/O	VA[4]	BIOT3UP	131	I/O
LD[2]	BIOT3UP	4	I/O	VA[3]	BIOT3UP	132	I/O
LD[3]	BIOT3UP	5	I/O	VA[2]	BIOT3UP	133	I/O
LD[4]	BIOT3UP	6	I/O	VA[1]	BIOT3UP	134	I/O
LD[5]	BIOT3UP	7	I/O	BVCC6	BVCCBSNQ	135	VDB
LD[6]	BIOT3UP	8	I/O	BVSS9	BVSSBENQ	136	VSB
LD[7]	BIOT3UP	9	I/O	BBSYIN	BINTTL	137	I
BVCC1	BVCCBP	10	VDB	BG3IN	BINTTL	138	I
LD[8]	BIOT3UP	11	I/O	BR3IN	BINTTL	139	I
LD[9]	BIOT3UP	12	I/O	DTACKIN	BINTTL	140	I
LD[10]	BIOT3UP	13	I/O	BERRIN	BINTTL	141	I
LD[11]	BIOT3UP	14	I/O	DSIN[0]	BINTTL	142	I
LD[12]	BIOT3UP	15	I/O	DSIN[1]	BINTTL	143	I
LD[13]	BIOT3UP	16	I/O	IACKIN	BINTTL	144	I
LD[14]	BIOT3UP	17	I/O	VIRQIN[7]	BINTTL	145	I
LD[15]	BIOT3UP	18	I/O	VIRQIN[6]	BINTTL	146	I
BVSS2	BVSSBP	19	VSB	VIRQIN[5]	BINTTL	147	I
LD[16]	BIOT3UP	20	I/O	VIRQIN[4]	BINTTL	148	I
LD[17]	BIOT3UP	21	I/O	VIRQIN[3]	BINTTL	149	I
LD[18]	BIOT3UP	22	I/O	VIRQIN[2]	BINTTL	150	I
LD[19]	BIOT3UP	23	I/O	VIRQIN[1]	BINTTL	151	I
LD[20]	BIOT3UP	24	I/O	VASIN	BINTTL	152	I
LD[21]	BIOT3UP	25	I/O	ACFAIL	BINTTL	153	I
LD[22]	BIOT3UP	26	I/O	SCON	BINTTL	154	I
LD[23]	BIOT3UP	27	I/O	SYSFAIL	BINTTL	155	I
BVCC2	BVCCBP	28	VDB	SYSRESETIN	BINTTL	156	I
LD[24]	BIOT3UP	29	I/O	BVCC7	BVCCBSNQ	157	VDB
LD[25]	BIOT3UP	30	I/O	VCCA2	BVCCA	158	VDA
LD[26]	BIOT3UP	31	I/O	VSSA2	BVSSA	159	VSA
LD[27]	BIOT3UP	32	I/O	BVSS10	BVSSBENQ	160	VSB
LD[28]	BIOT3UP	33	I/O	ABEN	BOUT6	161	O
LD[29]	BIOT3UP	34	I/O	ABDIR	BOUT6	162	O
LD[30]	BIOT3UP	35	I/O	ASDSEN	BOUT6	163	O
LD[31]	BIOT3UP	36	I/O	DBHEN	BOUT6	164	O

Signal	Buffer	Pin	Type	Signal	Buffer	Pin	Type
LD[32]	B3STA6	37	O/Z	BERR	BOUT3	165	O
BVSS3	BVSSBSNQ	38	VSB	VIRQOUT[0]	BOUT3	166	O
BVSS4	BVSSBENQ	39	VSB	VIRQOUT[1]	BOUT3	167	O
CLK	BINTTL	40	I	VIRQOUT[2]	BOUT3	168	O
CONF[1]	BINTTL	41	I	VIRQOUT[3]	BOUT3	169	O
CONF[0]	BINTTL	42	I	BVCC8	BVCCBP	170	VDB
TRSTN	BINTUP	43	I	DTACK	BOUT3	171	O
TCK	BINTTL	44	I	IACKOUT	BOUT3	172	O
TMS	BINTUP	45	I	IACK	BIOT3UP	173	I/O
TDI	BINTUP	46	I	SYSRESET	BOUT3	174	O
ALE	BINTTL	47	I	VA[24]	BIOT3UP	175	I/O
INULL	BINTTL	48	I	VA[25]	BIOT3UP	176	I/O
IOBENIN	BINTTL	49	I	VA[26]	BIOT3UP	177	I/O
MRSTIN	BINTUP	50	I	VA[27]	BIOT3UP	178	I/O
NOPARN	BINTTL	51	I	BVSS11	BVSSBP	179	VSB
PRSTN	BINTUP	52	I	VA[28]	BIOT3UP	180	I/O
RSEL	BINTTL	53	I	VA[29]	BIOT3UP	181	I/O
SEL16	BINTTL	54	I	VA[30]	BIOT3UP	182	I/O
WRT	BINTTL	55	I	VA[31]	BIOT3UP	183	I/O
DMAGNT	BINTTL	56	I	VD[16]	BIOT3UP	184	I/O
DRDY	BINTTL	57	I	VD[17]	BIOT3UP	185	I/O
MEXC	BINTTL	58	I	VD[18]	BIOT3UP	186	I/O
DDIRIN	BINTTL	59	I	VD[19]	BIOT3UP	187	I/O
BVCC3	BVCCBP	60	VDB	VD[20]	BIOT3UP	188	I/O
DDIROUT	BOUT6	61	O	VD[21]	BIOT3UP	189	I/O
RD	BIOT3UP	62	I/O	BVCC9	BVCCBP	190	VDB
SIZE[0]	BIOT3UP	63	I/O	VD[22]	BIOT3UP	191	I/O
SIZE[1]	BIOT3UP	64	I/O	VD[23]	BIOT3UP	192	I/O
LDSTO	BIOT3UP	65	I/O	VD[24]	BIOT3UP	193	I/O
LOCK	B3STA3	66	O/Z	VD[25]	BIOT3UP	194	I/O
ASI[0]	BIOT3UP	67	I/O	VD[26]	BIOT3UP	195	I/O
ASI[1]	BIOT3UP	68	I/O	VD[27]	BIOT3UP	196	I/O
ASI[2]	BIOT3UP	69	I/O	VD[28]	BIOT3UP	197	I/O
ASI[3]	BIOT3UP	70	I/O	VD[29]	BIOT3UP	198	I/O
TDO	B3STA3	71	O/Z	VD[30]	BIOT3UP	199	I/O
BVSS5	BVSSBSNQ	72	VSB	VD[31]	BIOT3UP	200	I/O
VCCA1	BVCCA	73	VDA	BVSS12	BVSSBSNQ	201	VSB
VSSA1	BVSSA	74	VSA	BVSS13	BVSSBENQ	202	VSB
BVSS6	BVSSBENQ	75	VSB	DMAREQ	BOUT3	203	O

Signal	Buffer	Pin	Type	Signal	Buffer	Pin	Type
VD[0]	BIOT3UP	76	I/O	DMAAS	BOUT6	204	O
VD[1]	BIOT3UP	77	I/O	WE	B3STA3	205	O/Z
VD[2]	BIOT3UP	78	I/O	SYSAV	BIOT3UP	206	I/O
VD[3]	BIOT3UP	79	I/O	DXFER	B3STA3	207	O/Z
VD[4]	BIOT3UP	80	I/O	IOBENOUT	BOUT6	208	O
VD[5]	BIOT3UP	81	I/O	BUSERR	BOUT3	209	O
VD[6]	BIOT3UP	82	I/O	BUSRDY	BOUT3	210	O
VD[7]	BIOT3UP	83	I/O	LIRQ[0]	BOUT3	211	O
VD[8]	BIOT3UP	84	I/O	LIRQ[1]	BOUT3	212	O
VD[9]	BIOT3UP	85	I/O	MRSTOUT	BOUT3	213	O
VD[10]	BIOT3UP	86	I/O	APAR	B3STA6	214	O/Z
BVCC4	BVCCBP	87	VDB	ASPAR	B3STA6	215	O/Z
VD[11]	BIOT3UP	88	I/O	IMPAR	B3STA6	216	O/Z
VD[12]	BIOT3UP	89	I/O	DMAADEN	BOUT6	217	O
VD[13]	BIOT3UP	90	I/O	DMAADTR	BOUT6	218	O
VD[14]	BIOT3UP	91	I/O	BVCC10	BVCCBSNQ	219	VDB
VD[15]	BIOT3UP	92	I/O	BVSS14	BVSSBENQ	220	VSB
AM[0]	BIOT3UP	93	I/O	LA[0]	BIOT3UP	221	I/O
AM[1]	BIOT3UP	94	I/O	LA[1]	BIOT3UP	222	I/O
AM[2]	BIOT3UP	95	I/O	LA[2]	BIOT3UP	223	I/O
AM[3]	BIOT3UP	96	I/O	LA[3]	BIOT3UP	224	I/O
AM[4]	BIOT3UP	97	I/O	LA[4]	BIOT3UP	225	I/O
AM[5]	BIOT3UP	98	I/O	LA[5]	BIOT3UP	226	I/O
BVSS7	BVSSBP	99	VSB	LA[6]	BIOT3UP	227	I/O
DBLEN	BOUT6	100	O	LA[7]	BIOT3UP	228	I/O
DBDIR	BOUT6	101	O	BVCC11	BVCCBP	229	VDB
BBSY	BOUT3	102	O	LA[8]	BIOT3UP	230	I/O
BR3	BOUT3	103	O	LA[9]	BIOT3UP	231	I/O
BG3OUT	BOUT3	104	O	LA[10]	BIOT3UP	232	I/O
DSOUT[0]	BOUT3	105	O	LA[11]	BIOT3UP	233	I/O
DSOUT[1]	BOUT3	106	O	LA[12]	BIOT3UP	234	I/O
VASOUT	BOUT3	107	O	LA[13]	BIOT3UP	235	I/O
WRITE	BIOT3UP	108	I/O	LA[14]	BIOT3UP	236	I/O
LWORD	BIOT3UP	109	I/O	LA[15]	BIOT3UP	237	I/O
VA[23]	BIOT3UP	110	I/O	BVSS15	BVSSBP	238	VSB
BVCC5	BVCCBP	111	VDB	LA[16]	BIOT3UP	239	I/O
VA[22]	BIOT3UP	112	I/O	LA[17]	BIOT3UP	240	I/O

Signal	Buffer	Pin	Type	Signal	Buffer	Pin	Type
VA[21]	BIOT3UP	113	I/O	LA[18]	BIOT3UP	241	I/O
VA[20]	BIOT3UP	114	I/O	LA[19]	BIOT3UP	242	I/O
VA[19]	BIOT3UP	115	I/O	LA[20]	BIOT3UP	243	I/O
VA[18]	BIOT3UP	116	I/O	LA[21]	BIOT3UP	244	I/O
VA[17]	BIOT3UP	117	I/O	LA[22]	BIOT3UP	245	I/O
VA[16]	BIOT3UP	118	I/O	LA[23]	BIOT3UP	246	I/O
VA[15]	BIOT3UP	119	I/O	BVCC12	BVCCBP	247	VDB
VA[14]	BIOT3UP	120	I/O	LA[24]	BIOT3UP	248	I/O
VA[13]	BIOT3UP	121	I/O	LA[25]	BIOT3UP	249	I/O
VA[12]	BIOT3UP	122	I/O	LA[26]	BIOT3UP	250	I/O
BVSS8	BVSSBP	123	VSB	LA[27]	BIOT3UP	251	I/O
VA[11]	BIOT3UP	124	I/O	LA[28]	BIOT3UP	252	I/O
VA[10]	BIOT3UP	125	I/O	LA[29]	BIOT3UP	253	I/O
VA[9]	BIOT3UP	126	I/O	LA[30]	BIOT3UP	254	I/O
VA[8]	BIOT3UP	127	I/O	LA[31]	BIOT3UP	255	I/O
VA[7]	BIOT3UP	128	I/O	BVSS16	BVSSBSNQ	256	VSB

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4.3 RELIABILITY

- The EVI32 failure rate at 50°C shall be lower than tbd fit

4.4 RADIATIONS

The EVI32 device withstands as a minimum 50 kRad of total dose radiation, has a low sensitivity to single event upsets, and is immune to heavy ion and proton induced latch-up.