INTRODUCTION

For people familiar with old ECSS-Q-ST-60-02C

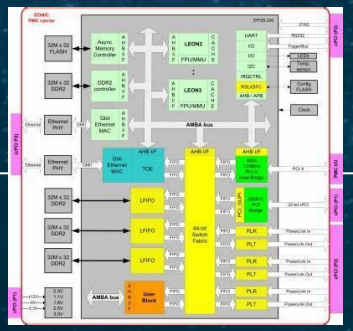
ECSS standards
ASIC, FPGA and IP Core

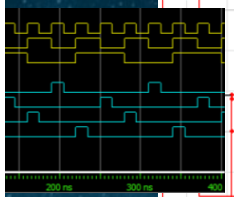
engineering

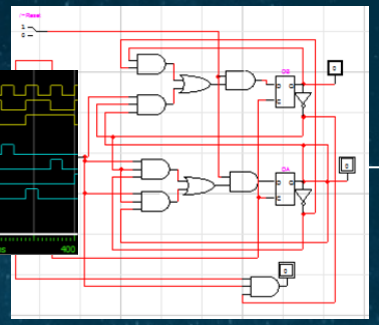
ECSS-E-ST-20-40C

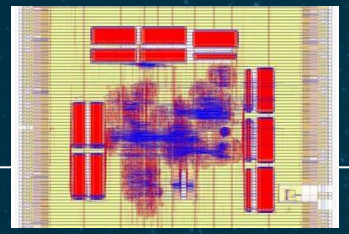
product assurance

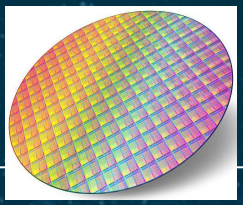
ECSS-Q-ST-60-03C

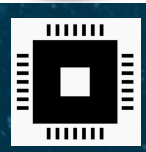


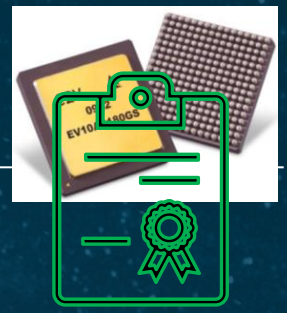












Agustín Fernández León (TEC-E)
Isabelle Conway (TEC-QQS)

Open info + Q&A session - 23/01/2024

Contents

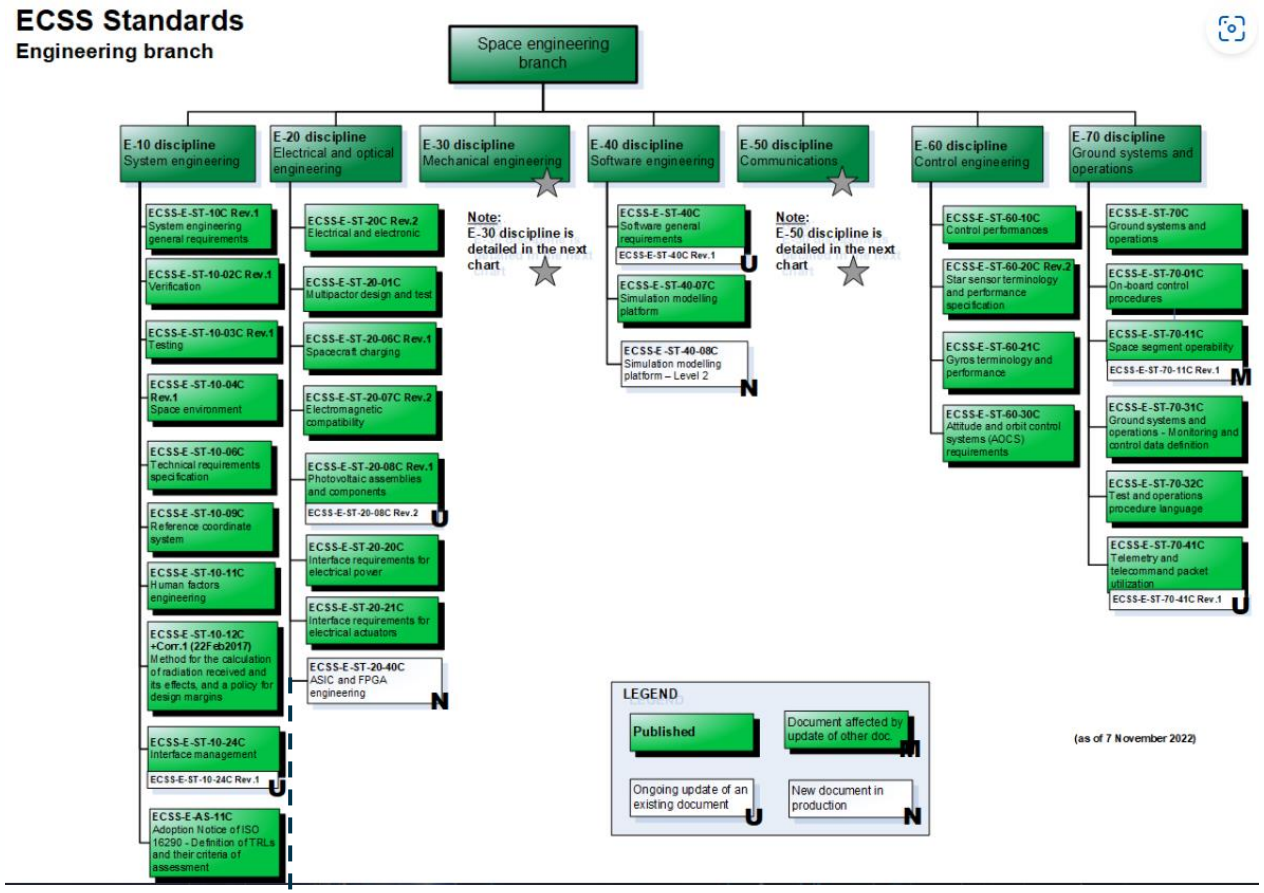
1. Brief history of ASIC/FPGA ECSS standards and handbook
2. Structure (main chapters, annexes) of new standards
3. Highlights of ASIC/FPGA/IP Core **Product Assurance** standard (ECSS-Q-ST-60-03)

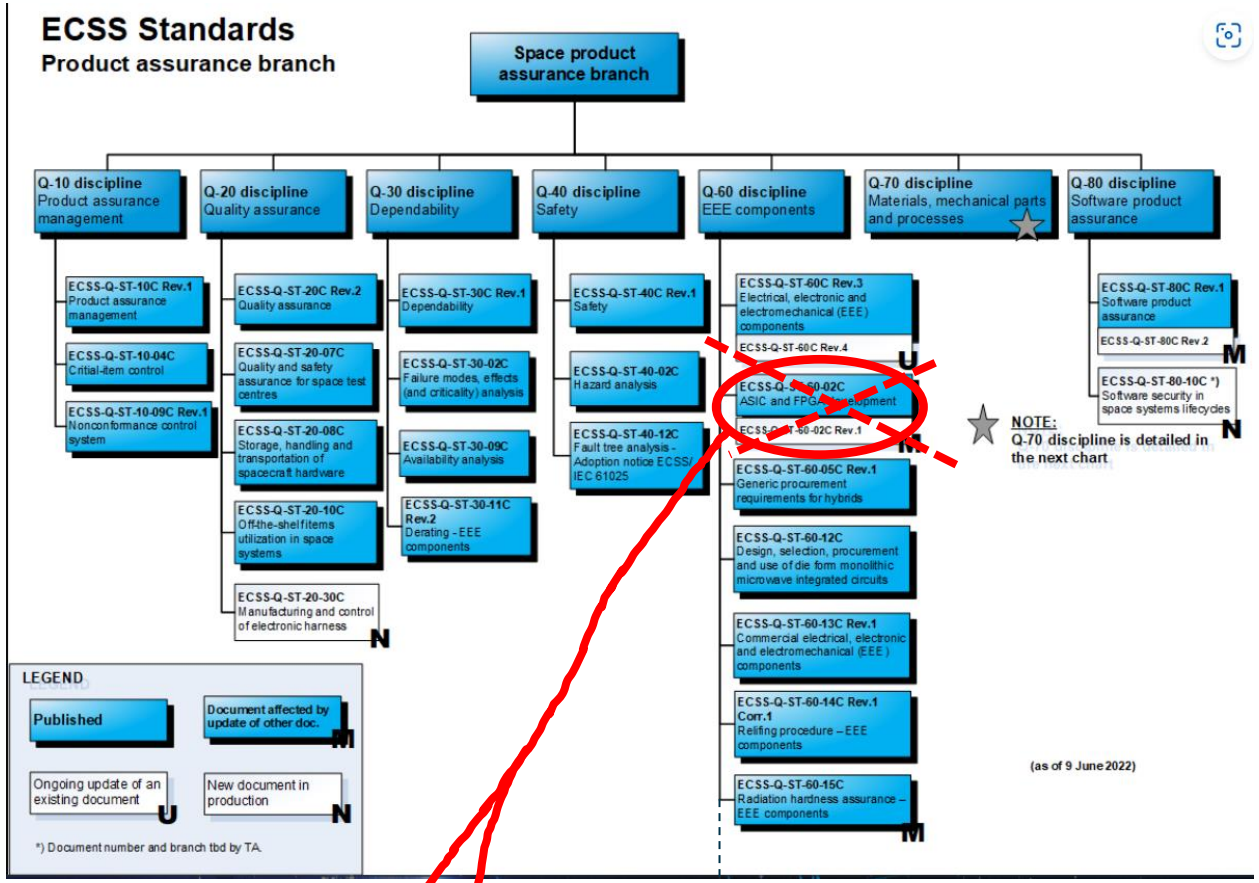
Focus on ASIC/FPGA/IP Core **Engineering** standard (ECSS-E-ST-20-40C)

6. Terms, definitions, conventions
7. Main content improvements wrt old standard engineering requirements (ECSS-Q-ST-60-02 chapter 5)
8. General requirements (tailoring, development flow, phase reviews, VCD)
9. Walk through development flow, phase by phase

10. Equipment/Systems vs DEVICEs development life cycles: milestones alignment in time and terminology
11. Where to find these standards and complementary information
12. Applying these standards and challenges
13. More information and questions

Old ECSS Q-60-02 (2008) standard is superseded by two: E-20-40 and Q-60-03 (11 Oct 2023)





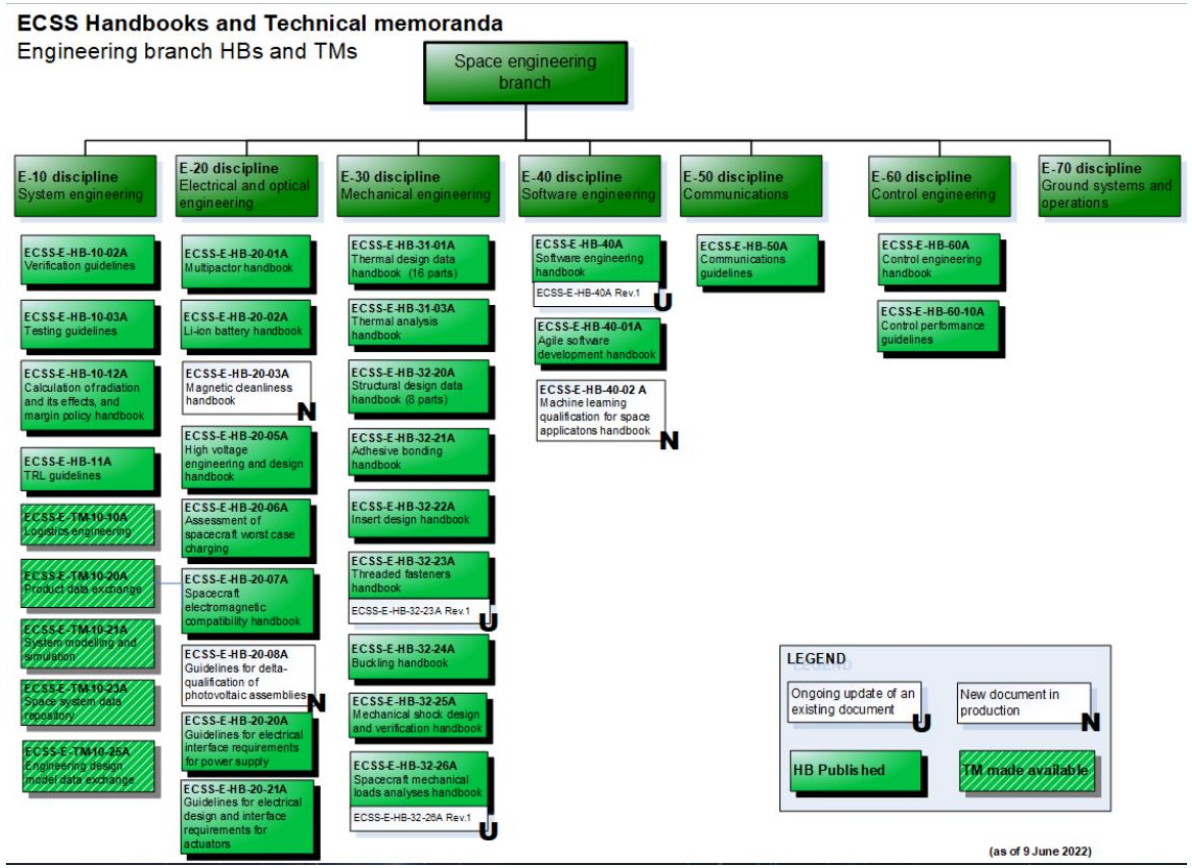
ECSS-E-ST-20-40C

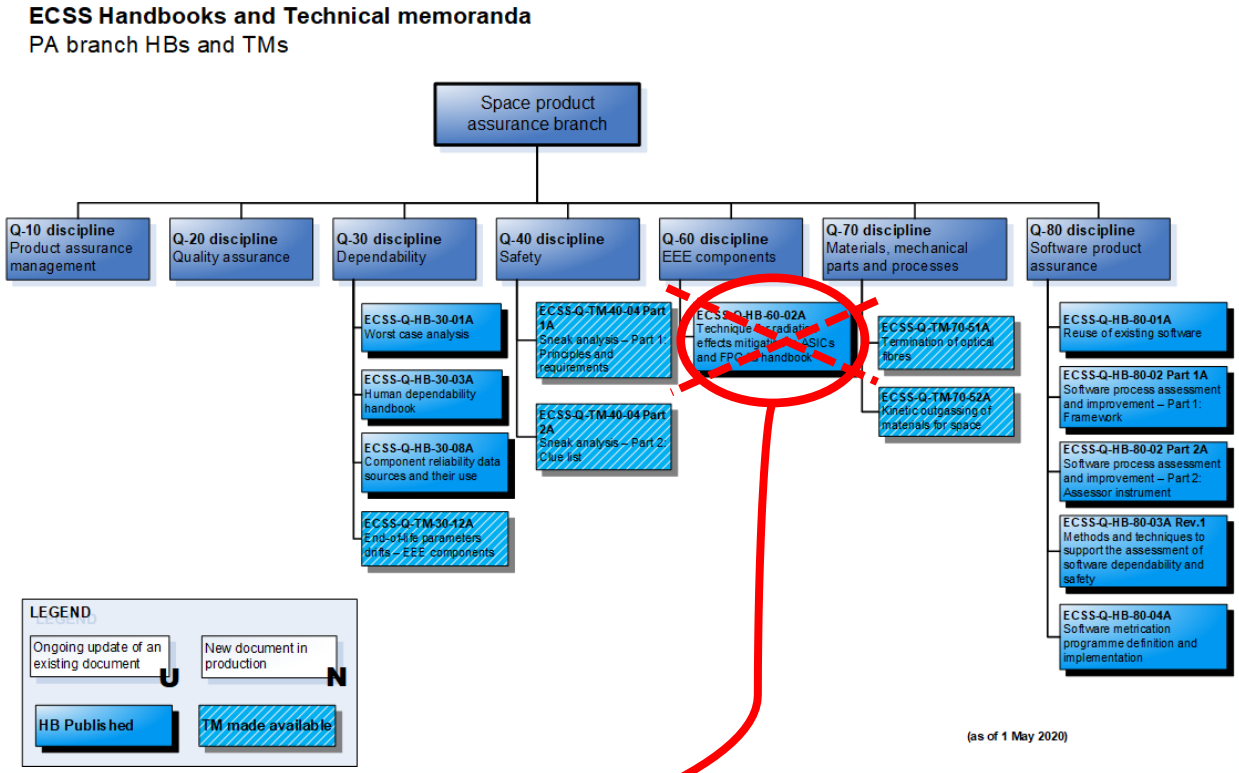
"ASIC, FPGA and IP Core engineering"
(Oct 2023)

ECSS-Q-ST-60-03C

"ASIC, FPGA and IP Core product assurance"
(Oct 2023)

ECSS HB on rad effects mitigation techniques for ASICs and FPGAs moves to E branch with slightly new name – contents are the same!





ECSS-**E**-HB-20-40A

"Engineering Techniques for radiation effects mitigation in ASICs and FPGAs" (Sept 2016)

ECSS standards for ASIC, FPGA and IP Core development - what for?

- **ECSS-E-ST-20-40C** - ASIC, FPGA and IP Core Engineering – 11th October 2023
- **ECSS-Q-ST-60-03C** – ASIC, FPGA and IP Core Product Assurance – 11th October 2023

Scope: successful development of **digital, analogue and mixed analogue-digital** signal custom designed integrated circuits, **ASICs, FPGAs** and **IP Cores** (= DEVICEs). Also applicable to non-monolithic microelectronics systems made of more than one die interconnected and packaged into a **System-in-Package** DEVICE. For SiP the standard applies to (a) the development of each individual monolithic die, and to (b) the integration onto a multi-die single DEVICE considering those dice as IP Cores.

Not in the scope: **selection, control, procurement or usage of DEVICEs** for space projects nor **DEVICE *ESCC qualification* requirements**. Those requirements are covered by ECSS-Q-ST-60C EEE components standard and the *ESCC generic specification No. 9000* respectively. Nevertheless, this standard contemplates the possibility for the DEVICE to undergo *ESCC qualification* after the DEVICE customer acceptance as an "ECSS qualified" DEVICE, and thus a DEVICE *ESCC Detail Specification* and DEVICE Radiation Test Plan and Report are **optional** expected outputs.

DEVICE "ECSS qualification" status: assessed based on the requirements from both ECSS-E-ST-20-40 and ECSS-Q-ST-60-03. DEVICE is qualified and accepted according to ECSS standards, when all DEVICE development reviews defined in ECSS-E-ST-20-40 are declared successful by the customer's engineering and PA responsible persons and project management who monitored the DEVICE development.

2 new stds have replaced old Q-ST-60-02C

ECSS

E

Q

ESCC

E-20 Electrical and electronic

Q-60 EEE Components

Q-ST-60-02C ASIC & FPGA Development

Ch. 5 Engineering

Ch. 4 & 6 program management & QA

E-ST-20-40 ASIC, FPGA and IP Core Eng.

Q-ST-60-03 ASIC, FPGA and IP Core PA

Generic Spec No. 9000

IC: Monolithic Microcircuits +

E-HB-20-40C Engineering Mitigation Techniques for ASIC & FPGA

Q-HB-60-02C Mitigation Techniques for ASIC & FPGA

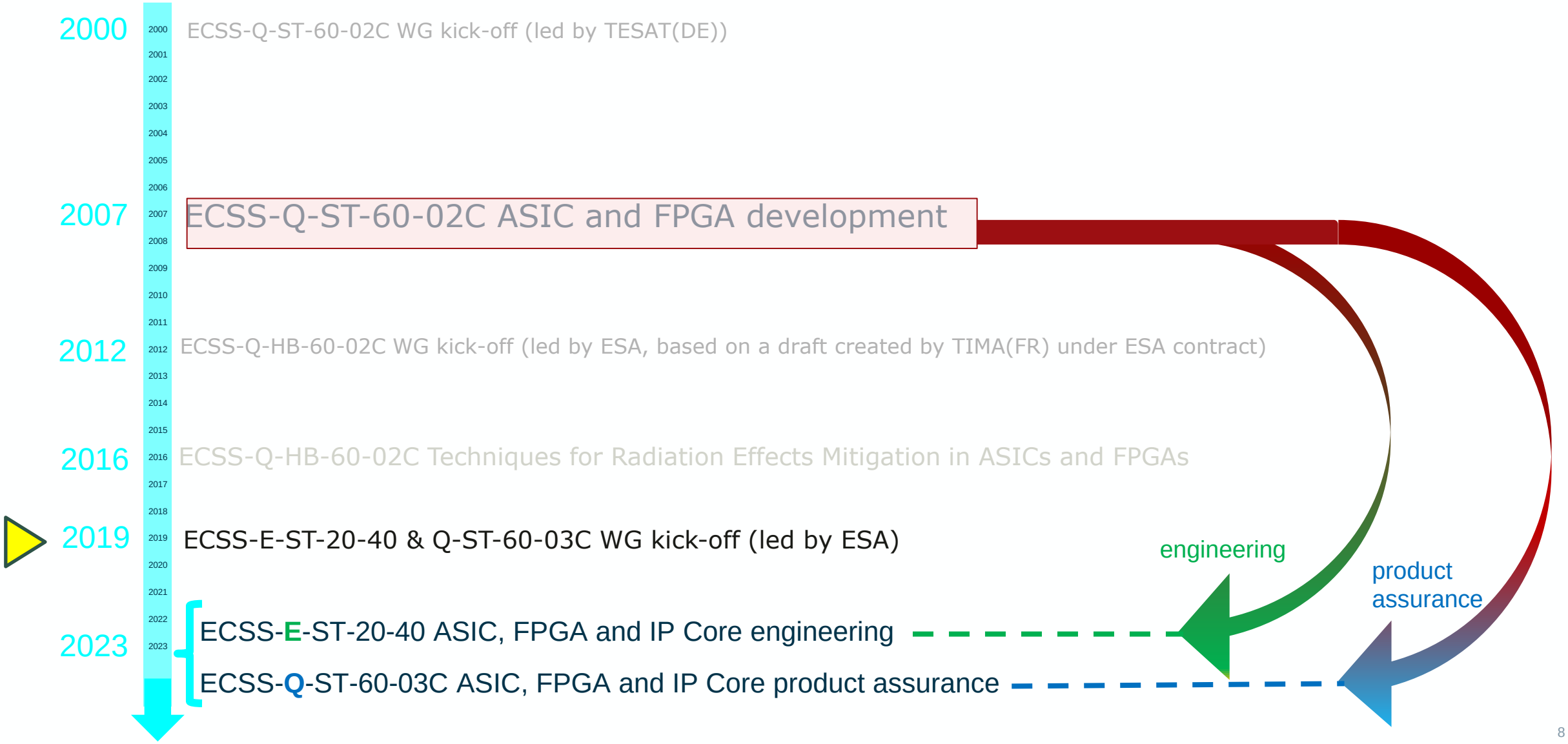
ECSS standards for ASIC, FPGA and IP Core development – history behind

- **ECSS-E-ST-20-40C** - ASIC, FPGA and IP Core Engineering – 11th October 2023
- **ECSS-Q-ST-60-03C** – ASIC, FPGA and IP Core Product Assurance – 11th October 2023

These 2 new ECSSes are the result of the **collaborative efforts of ASIC, FPGA and IP Cores (= "DEVICE") engineering experts and product assurance experts** (gathered in a common ECSS WG created in 2019)

- ECSS WG convenor and book captain for ECSS-E-ST-20-40 (Agustin Fernandez Leon – TEC-E)
- book captain for ECSS-Q-ST-60-03 (Isabelle Conway – TEC-QQS)

Timeline: ECSS ST and HB for ASIC and FPGA



Timeline: NEW ECSS Stds for ASIC, FPGA and IP Core

Aug 2017 - preliminary list of **28** change requests proposed by ESA Microelectronics Section

Apr 2018 - **42** change requests proposed by **11** ASIC/FPGA experts from European companies and institutes (including TAS, ADS, RUAG, Arquimea, Cobham Gaisler, TESAT, IMEC, CNES) at a dedicated meeting at ESTEC

Oct 2019 - New ECSS-E-ST-20-40 & Q-60-03C WG kick-off : **10** members, **37** experts (TAS, ADS, OHB, GMV, TESAT, Cobham Gaisler, BSC, Ariane, RAL, CNES, DLR and ESA)

After 2 years and 10 months, a world pandemic and >55 meetings…

Aug 2022 - ECSS-E-ST-20-40 & Q-ST-60-03C in Public Review between Aug 23rd -> Jan 2023

Oct 2023 - 11th Oct 2023: publication of new standards after WG processed **318** requests for changes

- ECSS-**E**-ST-20-40 ASIC, FPGA and IP Core engineering
- ECSS-**Q**-ST-60-03C Rev.1 ASIC, FPGA and IP Core product assurance

The “old” ECSS-Q-ST-60-02C had Engineering and PA requirements

Table of contents

85% !!

The “old” ECSS-Q-ST-60-02C had Engineering and PA requirements

Table of contents of Chapter 5

…

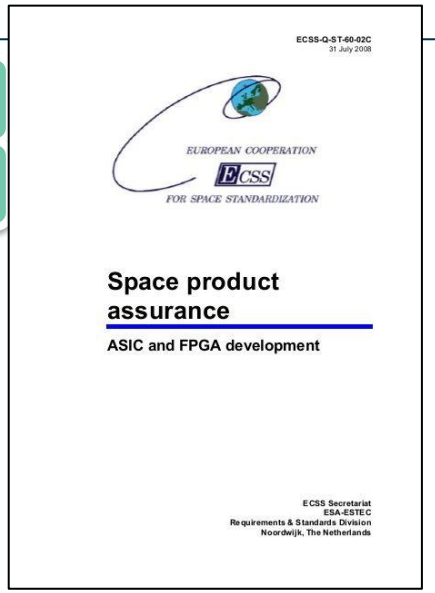
…

85% !!

The “old” ECSS-Q-ST-60-02C had Engineering and PA

15% is product / quality assurance , dependability

- But with many simple references to other Q-branch stds – New Q-60-03 has expanded such requirements for clarity and coherence with Q-branch ECSSes



new standards : first chapters

ECSS-E-ST-20-40C (2023)

Change log
Introduction
1 Scope
2 Normative references
3 Terms, definitions and abbreviated terms
- 3.1 Terms from other standards
- 3.2 Terms specific to the present standard
- 3.3 Abbreviated terms
- 3.4 Conventions
  - 3.4.1 Names of DEVICE development phases and reviews
  - 3.4.2 Companies involved in the DEVICE development
  - 3.4.3 Types of DEVICEs and requirements tailoring tag notation
- 3.5 Nomenclature

4 Principles
- 4.1 DEVICE development
- 4.2 Verification methods

ECSS-Q-ST-60-03C (2023)

Change log
1 Scope
2 Normative references
3 Terms, definitions and abbreviated terms
- 3.1 Terms from other standards
- 3.2 Terms specific to the present standard
- 3.3 Abbreviated terms
- 3.4 Conventions
  - 3.4.1 Names of DEVICE development phases and reviews
- 3.5 Nomenclature

4 ASIC, FPGA and IP Core product assurance principles
- 4.1 Overview
- 4.2 Organization of this Standard
- 4.3 Tailoring

These chapters DO NOT contain requirements

new standards separate Engineering and PA requirements

ECSS-E-ST-20-40C (2023)

5 DEVICE engineering
- 5.1 General requirements
- 5.2 DEVICE Definition Phase
- 5.3 DEVICE Architecture Definition Phase
- 5.4 DEVICE Design and Verification Phase
- 5.5 DEVICE Detailed Design Phase
- 5.6 DEVICE Layout Phase
- 5.7 DEVICE Implementation Phase
- 5.8 DEVICE Validation, Qualification and Acceptance Phase

6 Pre-tailoring according to DEVICE criticality and type

+ 12 Annexes (9 DRDs)

ECSS-Q-ST-60-03C (2023)

5 Product Assurance programme implementation
- 5.1 Organization and responsibility
- 5.2 DEVICE product assurance programme management
- 5.3 Risk management and critical item control
- 5.4 Supplier selection and control
- 5.5 Tools and supporting environment

6 DEVICE Process Assurance
- 6.1 DEVICE development lifecycle
- 6.2 Requirements applicable to all DEVICE engineering processes/phases
- 6.3 Requirements applicable to individual DEVICE engineering processes and activities
- 6.4 Process Assessment and improvement

7 DEVICE product quality assurance
- 7.1 Product quality objectives and metrication
- 7.2 IP Core or DEVICES intended for Reuse

8 DEVICE Configuration Management
- 8.1 DEVICE Configuration Management planning and control
- 8.2 Configuration Management implementation
- 8.3 Configuration Control

9 Tailoring by DEVICE criticality

+ 5 Annexes (3 DRDs)

Engineering and Product Assurance separation similar to
"ECSS-E-ST-40 SW engineering" and "ECSS-Q-ST-80 SW PA", compliant to ECSS-Q-ST-10/20/30 Product assurance

E-ST-20-40 Annexes (when "normative", they contain requirements too!)

Annex A (normative) DEVICE **Requirements Specification** (DRS) - DRD

Annex B (normative) DEVICE **Development Plan** (DDP) - DRD

Annex C (normative) DEVICE **Verification Plan** (DVeP) - DRD

Annex D (normative) DEVICE **Validation Plan** (DVaP) - DRD

Annex E (normative) DEVICE **Support and Maintenance Plan** (DSMP) - DRD

Annex F (normative) **Feasibility and Risk Assessment Report** (FRAR) - DRD

Annex G (normative) **Architecture Definition Report** (ADR) - DRD

Annex H (normative) DEVICE **Data Sheet** (DDS) - DRD

Annex I (normative) **Experience Summary Report** (ESR) - DRD

These normative Anexes DO contain (most of the) requirements!

And more…

Annex J (informative) **Generic Development Flow Variations**

Annex K (informative) DEVICE **Development Expected Outputs**

Annex L (informative) **Equivalence of phase and milestone terminology of ECSS-M-ST-10 and ECSS-E-ST-20-40**

Q-60-03C Annexes (if “normative” they contain requirements too!)

Annex A (normative) **Product Assurance Plan (DPAP)** - DRD

Annex B (normative) **Product Assurance Report (DPAR)** - DRD

Annex C (normative) **DEVICE Reuse File (DRF) – DRD**

Annex D (informative) **DEVICE Development Expected Outputs**

Annex E (informative) **Traceability from ECSS-Q-ST-60-03C to ECSS-Q-ST-60-02C**

These normative Annexes DO contain requirements but none of them are pre-tailored

These DRDs specify the scope and content of documents to be delivered as part of requirements in the ECSS body

EIDP (End Item Data-Package)	ECSS-Q-ST-20 Annex B
CMP (Configuration Management Plan)	ECSS-M-ST-40 Annex A
CIDL (Configuration Item Data List)	ECSS-M-ST-40 Annex C
ABCL (As-Built Configuration List)	ECSS-M-ST-40 Annex D
SCF (SW Configuration File)	ECSS-M-ST-40 Annex E

New standards: improving the FORMAT

- **higher clarity**, simplicity
- **better and new definitions** of terms used in the context of this standard. Some definitions eliminated (not used)
- consistent **terminology** , also wrt the new Software ECSS-E-ST-40 / Q-ST-80 stds, and clarifying terminology differences between M/Q/Product Assurance stds and terminology choices in E-ST-20-40/ECSS-Q-ST-60-03
- More examples and clarifications provided through many more “**NOTES**”
- Minimize dispersion of requirements between main chapters and normative annexes (DRD = Document Requirements Definition)
- Minimize redundancies (particularly inside each std, E and Q, but also between them).
- Separation of **engineering** (now in E-ST-20-40C) versus **product assurance** requirements (now in Q-ST-60-03C)

New standards: improving the FORMAT

E-ST-20-40:

- The main chapter structure of old ECSS-Q-ST-60-02C chapter 5 was maintained.
- Most requirements (directly linked to main key documents like Specs, Plans and Reports) are found in the DRD annexes, but there are in main chapters. This is why the main chapters are now much shorter!
- The pre-tailoring table in chapter 6 lists ALL requirements (both from DRDs and from main chapters).

Q-ST-60-03C:

- Chapter structure based on Q-ST-80 (co-engineering with E-ST-40) to ensure co-engineering with ECSS-E-ST-20-40, and with additional chapter for "Configuration Management"

NOTE: Q-ST-60-03C includes Annex E with one table that provides traceability from requirements in new Q-ST-60-03C (2023) to "old" Q-ST-60-02C (2008). A same table listing all "expected outputs" from both stds is included in both stds.

New standards: improving the CONTENT

E-ST-20-40:

- All chapters and requirements of old ECSS-Q-ST-60-02C chapter 5 taken as starting point, reviewed item by item, improving many requirements, adding many new ones, eliminating the ones superseded by new ones,
- having as reference a global “generic development flow” that admits variations, different types and criticalities of DEVICES
- all requests for changes gathered from industry and ESA experts implemented.

Q-ST-60-03C:

- All PA requirements from ECSS-Q-ST-60-02 were moved to Q-ST-60-03 (section 4, 6, and all clauses referring to ECSS-Q-ST-10/20/30). All Configuration Management requirements from ECSS-Q-ST-60-02 were also moved. A splinter sub-WG created to draft it.

NOTE: There are some content overlaps between the E-ST-20-40 and Q-ST-60-03C stds, as sometimes the borderline is blurry… similar things are being requested with different names, as Q-ST-60-03C strictly adheres to other Q and M standards and their terminology while E-ST-20-40 uses widely accepted DEVICE engineers’ terminology – thereby Annex L in E-ST-20-40 to help understand some terminology equivalences

ECSS-Q-ST-60-03C : some content highlights

- **What <u>has not</u> changed (since old ECSS-Q-ST-60-02C) in ECSS-Q-ST-60-03C**
  - ECSS-Q-ST-60-03C fully respects ECSS-Q-ST-60-02C compliance to **ECSS-Q-ST-10** (Product Assurance Management), **ECSS-Q-ST-20** (Quality Assurance), **ECSS-Q-ST-30** (Dependability), **ECSS-M-ST-10** (Project Planning and Implementation) and **ECSS-M-ST-40** (Configuration and Information Management)
  - ECSS Q-ST-60-03 has explicitly adapted all above ECSS requirements to ECSS-E-ST-20-40 workflow phases and reviews

NOTE: training for existing ECSSes (as listed on this slide and the following one) is organised by the ECSS Secretariat. Information can be found on the ECSS Website.

ECSS-Q-ST-60-03C : some content highlights

- **NEW requirements (wrt old ECSS-Q-ST-60-02C)** in ECSS-Q-ST-60-03C cover:
  - Tailoring by criticality (in line with ECSS-Q-ST-30/40), i.e. in line with severity of the consequence of DEVICE failure
  - Alignment to phases and reviews defined in ECCS-E-ST-20-40
  - Alignment to verification and validation activities defined in ECSS-E-ST-20-40
  - Security Assurance
  - Reuse: engineering, verification, legal (licence, IPR) requirements
  - Definition of deactivated and unreachable DEVICE functions
  - Definition of Metrication programme requirements
  - IVV – Independent Verification Validation by Third Party (for criticality A DEVICES)
  - ECSS qualification status assessment and maintenance, in line with ECSS-M-ST-10 and ECSS-Q-ST-20
  - Processes assessment and improvement
  - Risk Management (in line with ECSS-M-ST-80)
  - Safety (in line with ECSS-Q-ST-40)
  - Non Conformance Control System (in line with ECSS-Q-ST-10-09)

FOCUS of the presentation from now on

The DEVICE Engineering standard

ECSS-**E**-ST-**20-40C**

Major differences between ECSS-E-ST-20-40C and Q-ST-60-02C engineering chapter 5 – (1/2)

1. **New term definitions**: “software”, “building block”, “DEVICE”, “DEVICE database”, “DEVICE model”, “FPGA Programming Tests”, “processing unit”, “Production or Manufacturing Tests”, “synthesis tool”, “system requirements”, “validation”, “verification”, “verification methods”…**34 terms** (old one: 23) and others improved (e.g. “IP Cores”) or eliminated (were not used)
2. Many **NOTES** added with more **examples and clarifications**
3. **Most requirements are now “first level” (can be tailored individually).** Only a few “level 2” sub-lists
4. **Tags** indicating the applicability of each requirement to the four DEVICE types: **[D-ASIC**, **A-ASIC, FPGA**, **IP]**
5. “General Requirements” covering:
    - **Tailoring** according to **DEVICE type** and **DEVICE criticality** (a single table in chapter 6 for both tailorings)
        - This table can be transformed in a “csv” or “XLSX” file to easily pre-tailor each specific case
    - DEVICE engineering **development flow “generic”** and **“variations”** in an informative annex with diagrams
    - **Phase Reviews** share a common set of general requirements

Major differences between ECSS-E-ST-20-40C and old Q-ST-60-02C engineering chapter 5 (2/2)

6. Improved and more **development flow figures** (in fig. 5-1 and figures in Annex J)
7. **New phase** and **review names** – more self explanatory (in line with DEVICE engineer community jargon), deviating sometimes from “system/equipment” milestones or document names as per ECSS-M-ST-10 (new Annex L added to explain the names equivalence)
8. **New phase** added between “DPR” (for “DEVICE **D**efinition **P**hase **R**eview”, called “SRR” in old std) and “DVR” (for DEVICE **D**esign and **V**erification Phase **R**eview, called “PDR” in old std): **DEVICE Architecture Definition Phase**, with its own **review** called **“ADR”** (for DEVICE **A**rchitecture **D**efinition Phase **R**eview)
9. **New review** at the end of the **DEVICE Implementation Phase** to ensure readiness of all docs, HW and SW to initiate the DEVICE Validation, Qualification and Acceptance Phase. This review is abbreviated as “IPR”
10. **New requirements** added and many old ones improved for:
    I. DEVICES that contain “**processing units**” (which will use SW to operate) to ensure better **HW-SW co-engineering**
    II. development and **re-use of “IP Cores”** and **“building-blocks”**
    III. development of **mixed-signal ASICs / analogue IPs**

ECSS-E-ST-20-40C : terms, definitions, conventions

Application Specific Integrated Circuit
block diagram
Building Block
cell
cell library
code
data sheet
design for test
design iteration
DEVICE
DEVICE Database
DEVICE development flow
DEVICE model
DEVICE technology
fault coverage
Field Programmable Gate Array
floorplan
FPGA Programming Test
HDL model
IP Core
macrocell
netlist
phase
processing unit
Production Test
prototype
redesign
software
stimuli
synthesis tool
system requirement
Validation
Verification

ECSS standards for developing “DEVICEs”

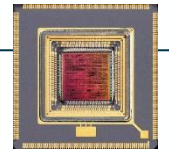
3.2 Terms specific to the present standard

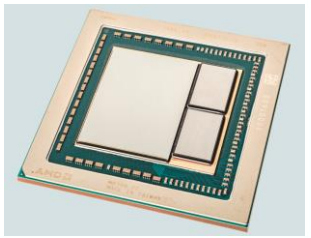
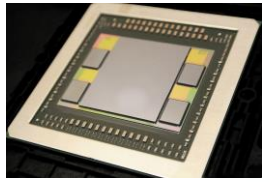
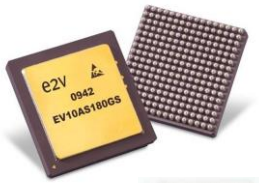
3.2.10 DEVICE

integrated circuit or an IP Core

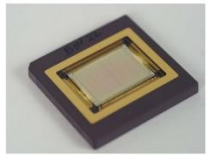
NOTE 1 A DEVICE can be a digital, analogue or mixed-signal ASIC, a programmed FPGA, a blank FPGA, a microprocessor, and a model of an IC function that is conceived for reuse as an IP Core.

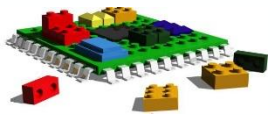
NOTE 2 A DEVICE can also be a group of dice or chiplets interconnected and integrated inside a single package, such as a system-in-package or a multi-chip-module.



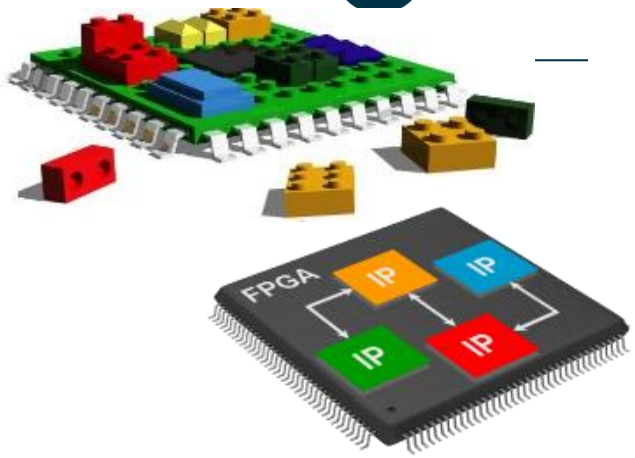






“IP Cores” – a tricky concept to understand…



“IP Core” definition is included in the new standard ECSS-E-ST-20-40:

3.2.20 IP Core

integrated circuit design element that implements a self-standing function or group of functions for which ownership rights exist and is developed for reuse and released with comprehensive verification, validation and documentation

NOTE 1 IP core can be acquired by a customer, for a given price and under an owner-defined license agreement specifying the customer's acquired rights.

NOTE 2 IP core can be supplied as an HDL model, as a synthesizable VHDL code or gate-level netlist, and with the essential complementary documentation that allows the customer to successfully integrate and use it in a system for example User’s Manual and verification files. From this point of view, it can be seen as a semi-finished product.

NOTE 3 IP Cores can be analogue functions provided by DEVICE technology providers as macrocells.

NOTE 4 In contrast with Building Blocks, IP Cores have gone through comprehensive verification, validation and documentation intended for reuse of third parties.

NOTE 5 IP Cores sometimes are referred as hard IPs if they are already placed and routed for one specific IC technology. For example, a macrocell already pre-diffused inside an FPGA or an already layouted function that is included in an ASIC, or a netlist that cannot be modified and is treated as a black-box.

NOTE 6 An IP Core can be composed by combination of different IP Cores.

Textual or graphical MODEL of an integrated circuit

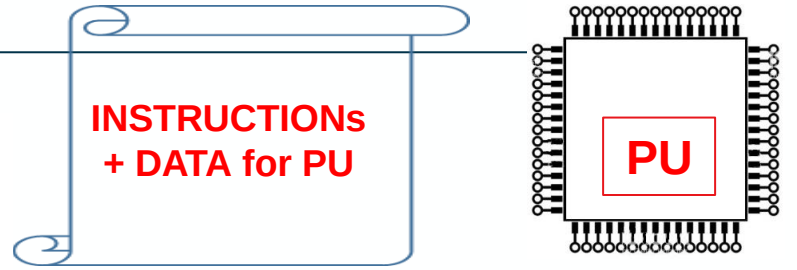
”**building block**”, similar BUT different to “IP Core”, also defined in the standard:

3.2.3 Building Block

reusable IC design element that implements a self-standing function or group of functions for which ownership rights exist and that has been developed in the context of a specific IC project or technology, without the intention to be shared with third parties for its reuse in other IC projects

NOTE For example, an HDL model such as synthesizable VHDL code, or gate-level netlist, or an analogue function.

SW-HW co-engineering in DEVICEs embedding "processing units"



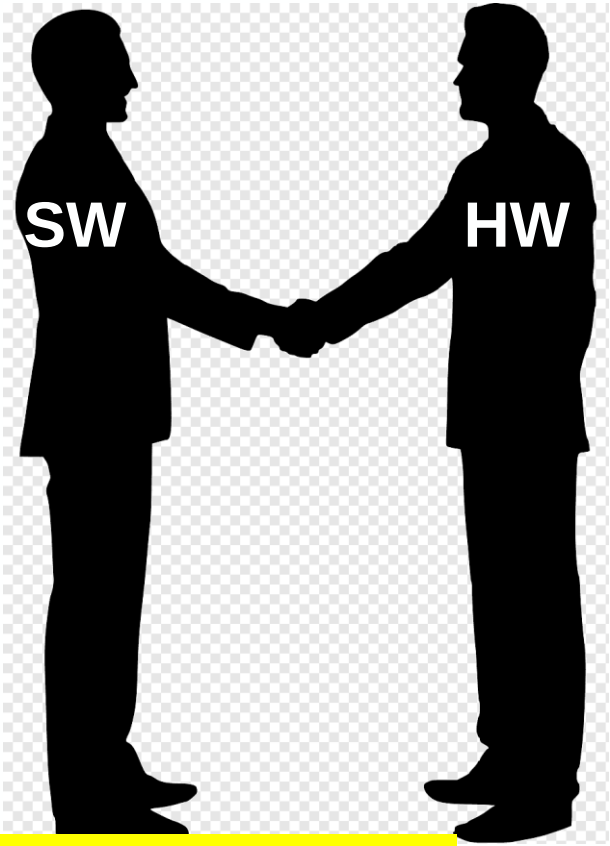
3.2.28 software

set of instructions and data executed on a processing unit

NOTE 1 A processing unit can be hardware, for example a processor chip, or software, for example a virtual machine or an interpreter.

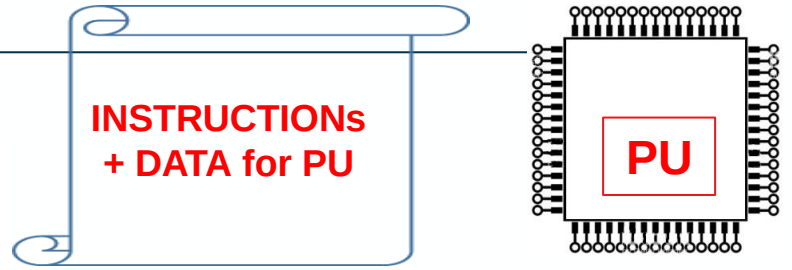
NOTE 2 Some processing units only require data, for example configuration of state machines or configuration data of a neural network.

NOTE 3 Files using Hardware Description Languages (VHDL, Verilog, System-C) used to model ASICs or bit stream files used to program FPGAs are not software.



This definition was discussed and agreed with **ECSS-E-ST-40 Software Engineering standard WG** !!

SW-HW co-engineering in DEVICEs embedding "processing units"

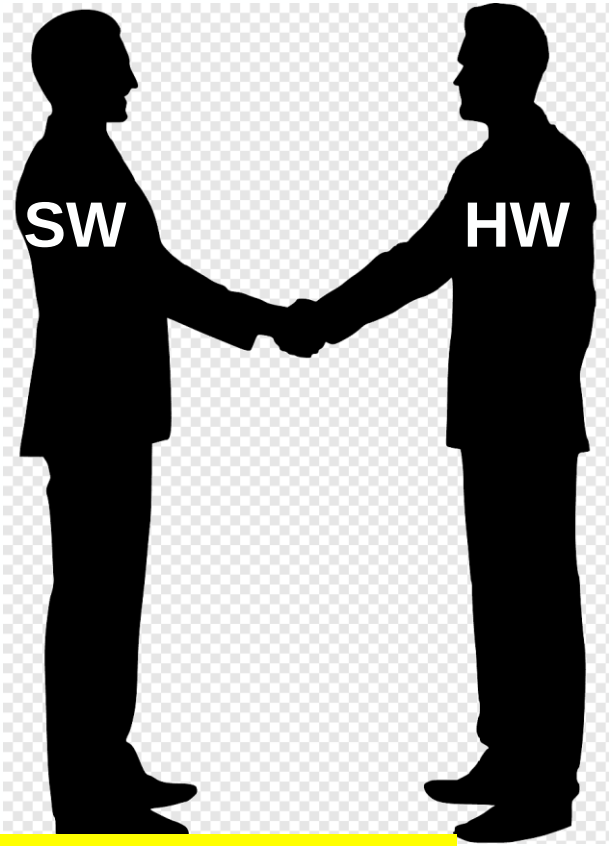


3.2.24 processing unit

function which is defined to execute software

NOTE 1 The term covers hardware functions such as general purpose processing cores, and more specialized Graphical Processing Unit (GPU), Vision Processing Unit (VPU), Tensor Processing Unit (TPU), Neural Processing Unit (NPU), Physics Processing Unit (PPU), Digital Signal Processor (DSP), or Image Signal Processor (ISP).

NOTE 2 In the context of SW engineering, it also covers software processing units such as interpreters, emulators and virtual machines.



This definition was discussed and agreed with **ECSS-E-ST-40 Software Engineering standard WG** !!

and… what about “FIRMWARE”?

FPGAs are NOT firmware!

FPGAs are hardware that can use firmware to be programmed

Firmware is a term originally created for **computer’s software** which was stored in non-volatile memory devices (making it “firmer”).

Today these type of memories can be stand- alone devices or be embedded inside larger devices, and they can store different things. For example, but not only:

- “**software**” used by “processing units” inside other devices (this is OK to be called “firmware”)
- “**bit streams**” to program FPGAs (please do not call this “firmware” as it is not “computer’s SW stored in memory”)
- “**data**” containing various types of info (satellite payload instruments measurements, satellite telemetry, etc.). This should not be called firmware either

In **ECSS-E-ST-20-40C** (2023):

3.1 Terms from other standards

NOTE The old term *firmware* is defined in ECSS-S-ST-00-01C, and it is not used in the context of ECSS-E-ST-20-40 because with the emergence of new technologies it is now ambiguous and unnecessary. It is important not to confuse terms like *FPGA*, *FPGA programming file* or *FPGA programming bit stream* with *firmware*.

In ECSS-S-ST-00-01 Rev.1 (2023):

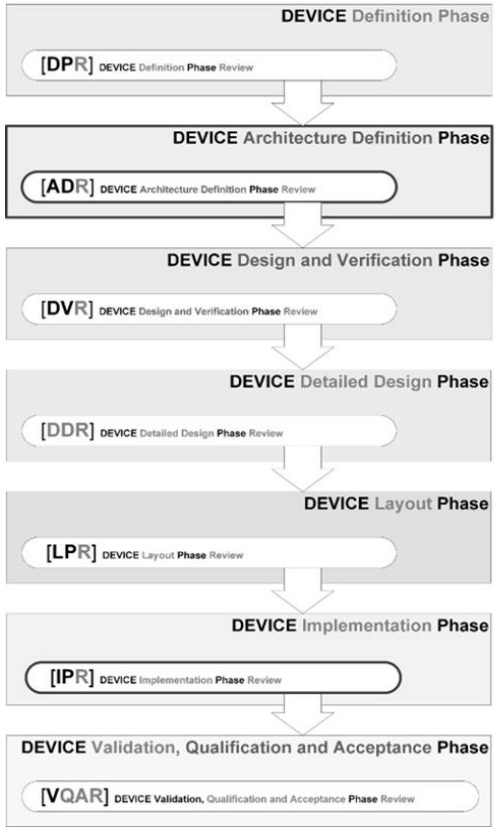
2.3.94 firmware

hardware that contains a computer program or data that cannot be changed in its user **environment**

NOTE The computer program and data contained in firmware are classified as software; the circuitry containing the computer program and data is classified as hardware.

ECSS-E-ST-20-40C : principles and conventions

4.1 DEVICE development



Generic flow:

- 7 phases
- 7 reviews

Main expected outputs:

- DEVICE requirements specification
- Plans
- Reports
- DEVICE database
- prototypes and final DEVICE

4.2 Verification methods

1. ANALYSIS
2. SIMULATIONS
3. TEST
4. REVIEW
5. INSPECTION

…of DEVICE documents, models or prototypes

"EXPECTED OUTPUTS" vs. "CONTRACT DELIVERABLES"

The contract between customer and supplier for the development of the DEVICE defines which "expected outputs" shall be made (or not) available to the customer and in which way (e.g. as a "deliverable", at supplier's premises, etc.). Expected outputs lists are in **Annex K**.

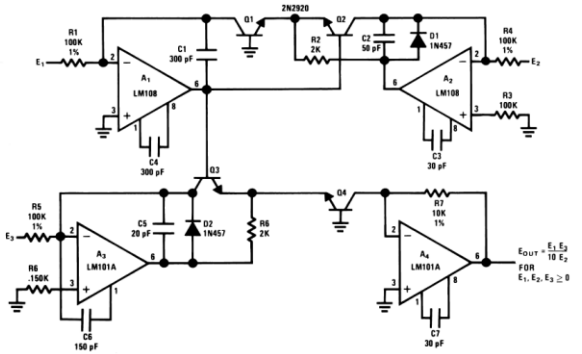
DEVICE types

Four main DEVICE types (tags next to each requirement indicate applicability as explained in chapter *3.4 Conventions* of ECSS-E-ST-20-40):

- **D-ASIC**: applicable to fully digital ASICs, or the digital part of mixed-signal ASICs
- **A-ASIC**: applicable to fully analogue ASICs, or the analogue part of mixed-signal ASICs
- **FPGA**: applicable to FPGAs
- **IP**: applicable to digital or analogue IP Cores

Tag examples: [D-ASIC, A-ASIC, FPGA, IP] = [ALL] , [D-ASIC, A-ASIC, FPGA, --] , [--, A-ASIC, --, --] , etc.

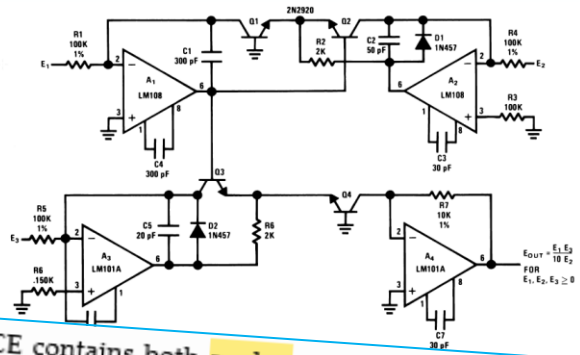
Analogue / MS DEVICE developments



- Several new requirements on:
  - **tailored development flow variations** (phases/reviews merging, parallel flows of individual modules, additional intermediate reviews, iterations if appropriate and agreed with customer) at the beginning
  - **interaction between digital and analogue design teams** (outputs/inputs exchanged, scheduled milestones for those exchanges)
  - subcontracted design work to **third parties**, their design methodology and compliance to the ECSS standards
  - development and use of **Analogue IP Cores**

- Several “old” requirements specific to A/MS ASICs were **revised and improved** by WG analogue experts in dedicated WG meetings

Analogue / MS DEVICE developments



- Several new requirements - EXAMPLES

e. If the DEVICE contains both analogue and digital blocks, the supplier shall plan and document how to synchronise the DEVICE development flow key milestones with the analogue and digital development flows key milestones in order to manage dependencies. **[ALL]**

f. The DVeP shall define the strategy to verify analogue functional and performance requirements, including the interfaces. **[--, A-ASIC, --, --]**

g. If the DEVICE contains both analogue and digital blocks, the DDP shall indicate what are the inputs and outputs exchanged between the analogue and digital development teams, indicating as well at which phase and step during the DEVICE development flow the exchanges are expected. **[D-ASIC, A-ASIC, --, --]**

NOTE For example, what design models, database elements, documents are produced and exchanged between the analogue and digital design teams.

c. The supplier shall model analogue block interfaces, drivers and loads including their estimated parasitics. **[--, A-ASIC, --, --]**

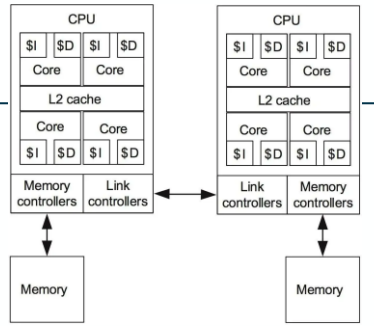
NOTE For example, parasitics introduced by the package, bonding or wiring tracks.

d. The supplier shall perform an analysis of key analogue parameters and their sensitivity to manufacturing and environmental variations in order to consequently protect the DEVICE analogue blocks against those variations. **[--, A-ASIC, --, --]**

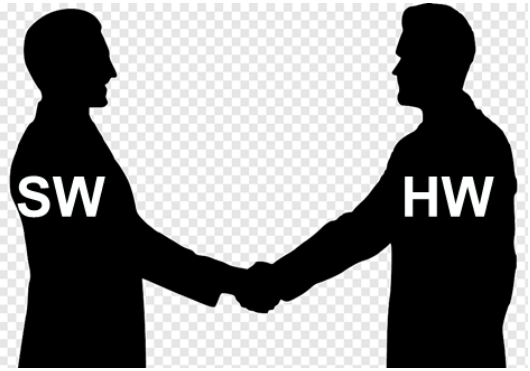
NOTE For example, parameters such as circuit dimensions or electrical parameters which can be affected by process manufacturing and external T, V or I variations.

i. The supplier shall implement design parameter centring based on simulations, allowing margins that account for final layout and process variations, in order to maximise yield. **[--, A-ASIC, --, IP]**

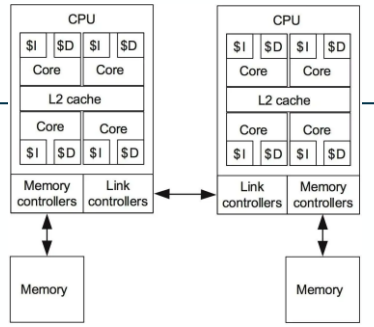
SW-HW co-engineering in DEVICEs embedding “processing units”



- There were no requirements specific to HW-SW co-engineering in the “old” std
- Definition of “software” and “processing unit” added
- Improvements to definitions of “IP Cores” and “building block” that can help to the better design and integration of ”processing units” used inside the DEVICE
- Several new requirements for the **interaction between HW and SW design teams** (outputs/inputs exchanged, schedule of related milestones)



SW-HW co-engineering in DEVICEs embedding "processing units"



- Several new requirements for the **interaction between HW and SW design teams** – Examples

c. The DRS shall specify the preliminary architectural and HW-SW partitioning, including external and internal memory mapping. **[D-ASIC, --, FPGA, IP]**

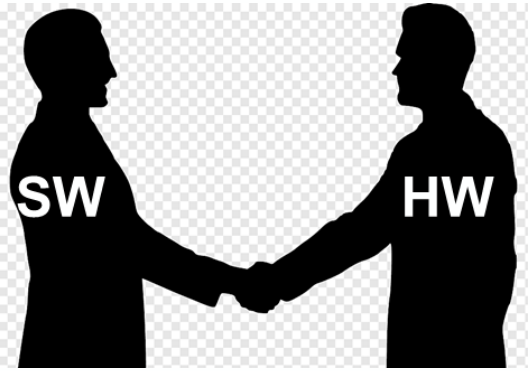
d. If the DEVICE contains one or more processing units, the supplier shall plan and document how to synchronise the DEVICE development flow key milestones with the System and SW development flows key milestones in order to manage dependencies between DEVICE, SW and System developments. **[D-ASIC, --, FPGA, IP]**

d. If the DEVICE contains one or more processing units, the DRS shall specify the requirements related to interfaces between the software items and the hardware interfaces of the DEVICE **[D-ASIC, --, FPGA, IP]**

NOTE See ECSS-E-ST-40 5.2.4.3.a

c. If the DEVICE contains one or more processing unit, the supplier shall flow the HW-SW partitioning requirements in the System Requirements down into the DEVICE Requirements Specification. **[D-ASIC, --, FPGA, IP]**

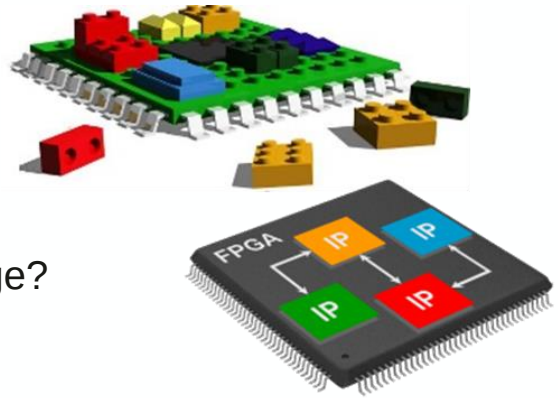
NOTE HW-SW partitioning is usually done by the System team, often the customer, in collaboration with HW and SW development teams (see requirement 5.2.2.4.a of ECSS-E-ST-40).



Development and reuse of IP Cores

In E-ST-20-40: in several phases, 20 specific requirements for development and/or reuse of IP Cores

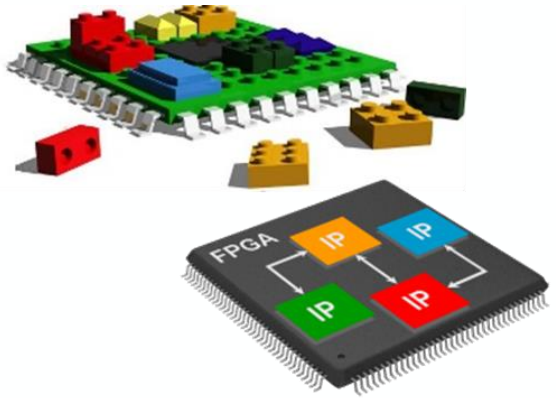
- Requirements (from systems requirements) to use certain IP Cores?
- Identification of IP Core developments as a “sub-product” of a DEVICE development, including target technologies
- Feasibility and risk assessment of IP Core development (plans) and/or reuse (existing docs + database) to decide on additional verification and/or validation (also assessed at Architectural Definition Phase); limits in use and distribution due to legal/patent status
- IP Core design modifications impact in Development, Verification and Validation Plans, and Feasibility and Risk
- IP Core configuration used?
- Integration approach of IP Cores up to top level
- IP Cores netlist generation specific constraints and deviations from IP vendor recommendations
- Specific verification and validation strategies for IP Cores
- Experience Summary Report: any lessons learned about reused IP Cores relevant for future usage?



Development and reuse of IP Cores

In Q-ST-60-03:

- 6.2.3 Reuse of existing DEVICEs
  - reuse category according to "*heritage*" as per ECSS-E-ST-10-02 Table 5-1,
  - **DEVICE Reuse File** (DRD Annex C) to compile all reuse aspects / info
- 7.2 IP Core or DEVICEs intended for Reuse
  - self-contained info,
  - portability and verification/validation in all intended technologies,
  - configuration management,
  - certificate of conformance



General requirements

5.1.2 Tailoring according to DEVICE type and DEVICE criticality

5.1.3 DEVICE engineering development flow

5.1.4 Phase Reviews

5.1.5 DEVICE Verification Control Document

General requirements

5.1.2 Tailoring according to DEVICE type and DEVICE criticality

ECSS-E-ST-20-40_1580001

a. Criticality category of the DEVICE under development shall be discussed and agreed with the customer. **[ALL]**

ECSS-E-ST-20-40_1580002

b. Customer and supplier shall define the final tailoring of the requirements of ECSS-E-ST-20-40 according to the type of DEVICE and according to its criticality category in compliance with clause 6. **[ALL]**

Pre-tailoring according to DEVICE criticality category

As explained in chapter 6.1

ONLY 2 main DEVICE criticality categories (based on criticality categories defined in ECSS-Q-ST-30 Dependability clause 5.4, also used in ECSS-Q-ST-80 Software PA):

- **A** or **B** or **C** criticality (respectively, “catastrophic”, “loss of mission” or “major effects”) -> all requirements apply! No pre-tailored waivers.
- **D** criticality (“minor effects”) -> some requirements are waived or made lighter (e.g. less or no documentation requested)

Pre-tailoring table in 6.2 chapter

The same table indicates tailoring per DEVICE **type** and **criticality**, and if it is a **conditional requirement**

Approximately **14%** of all requirements are waived or relaxed for category **D** DEVICES (“minor” impact to the mission where DEVICE will fly, and all “R&D developments”)

ECSS Source ID	Requirement main text	Requirement NOTES	Digital ASIC	Analog ASIC	FPGA	IP Core	if CRITICALITY Category D	Conditional requirement
▪ ▪ ▪								
5.2.4c	Modified IP Cores shall be treated as Building Blocks that undergo full verification and validation. [ALL]		yes	yes	yes	yes	yes	
5.2.5	**Preliminary DEVICE Support and Maintenance Plan**							
5.2.5a	If agreed between supplier and customer a preliminary DEVICE Support and Maintenance Plan shall be produced by the supplier in compliance with DRD from Annex E. [ALL]		yes	yes	yes	yes	yes	yes
5.2.6	**Feasibility and Risk Assessment**							
5.2.6a	The supplier shall perform a feasibility and risk assessment of the development of the DEVICE and document it in the DEVICE Feasibility and Risk Assessment Report in compliance with DRD in Annex F. [ALL]		yes	yes	yes	yes	yes	
▪ ▪ ▪								
5.6.2b	Floorplan of the DEVICE shall be finalised. [D-ASIC, A-ASIC, FPGA, --]		yes	yes	yes	no	partial (no report required)	
5.6.2c	The core and I/O-pad power distribution shall be generated. [D-ASIC, A-ASIC, --, --]		yes	yes	no	no	yes	
5.6.2d	Test pads, if needed, shall be generated. [D-ASIC, A-ASIC, --, --]		yes	yes	no	no	partial (no report required)	yes
▪ ▪ ▪								
A.2.1<8>	**A.2.1<8> Power**							
A.2.1<8>a	The DRS shall specify the power consumption requirements. [D-ASIC, A-ASIC, FPGA, --]		yes	yes	yes	no	yes	

Some statistics of ECSS-E-ST-20-40C requirements

TOTAL NUMBER OF REQUIREMENTS **302**

D-ASIC	A-ASIC	FPGA	IP Core	
x	x	x	x	238 (79%)
	x			3
x		x	x	7
x	x			16
x	x	x		23

36 (12%)
"conditional" requirements
(start with "**If**" …)

42 (14%)
requirements for "low criticality" DEVICE (Cat. D) that are waived or relaxed (none or less reporting required)

Number of requirements in both E and Q standards

	E-ST-20-40C	Q-ST-60-03C
Total number of requirements	**302**	**162**
waived/relaxed requirements due to lower CRITICALITY Category (lower than Cat. A)	**42** (Cat. D)	**38** (Cat. D), **8** (C), **7** (B)
Conditional requirements	**36**	**2**

Number of requirements – old vs new standards

	old Q-ST-60-02C (2008)	E-ST-20-40C (2023)	Q-ST-60-03C (2023)
Total number of requirements	**333** (**57** were PA/QA)	**302**	**162**
waived/relaxed requirements due to lower CRICALITY Category	0	**42** (Cat. D)	**38** (Cat. D), **8** (C), **7** (B)
Conditional requirements	0	**36**	**2**

General requirements

b. If the DEVICE Development Plan includes any variations with respect to the generic flow shown in Figure 5-1, all the outputs expected at every new phase and associated review shall reflect these changes too. **[ALL]**

NOTE 1 For example, in case of having phase iterations or additional sub-phases and reviews, the Verification and Validation Plans include what requirements are covered in each new phase.

NOTE 2 Annex J describes the main types of DEVICE development flow variations.

5.1.2 Tailoring according to DEVICE type and DEVICE criticality

5.1.3 DEVICE engineering development flow

d. If the DEVICE development is planned to undergo a first Engineering Model development followed by a Flight Model development, customer and supplier shall agree whether EM and FM are treated as two independent DEVICE developments or as a single DEVICE development where the EM is mainly a prototype verification step for the development of the final FM DEVICE. **[ALL]**

NOTE 1 Treating EM and FM as independent developments can be adequate whenever their respective implementation technologies are significantly different, and therefore the models of EM and FM DEVICEs are significantly different too.

NOTE 2 Treating EM and FM as independent developments can also be adequate if EM DEVICE is planned to be used as a stand-alone product and not just as an intermediate verification step for the FM DEVICE.

5.1.4 Phase Reviews

5.1.5 DEVICE Verification Control Document

g. In order to reopen a phase that was successfully closed already, supplier and customer shall discuss and reach an agreement on it. **[ALL]**

DEVICE development flow: any differences wrt old standard?

The new **ECSS-E-ST-20-40C** standard defines a "**generic development flow**" which is also the milestone's backbone reference used by its complementary and also new **ECSS-Q-ST-60-03C**.

The flow is basically the same as the one defined in the old ECSS-Q-ST-60-0**2**C, but with a few important differences:

- New names for Phases and Reviews (we will all have to get used to the new acronyms ☺, a simple table to help with that follows…)

- One new Phase added, two new Reviews added

Different names of phases and reviews

NEW

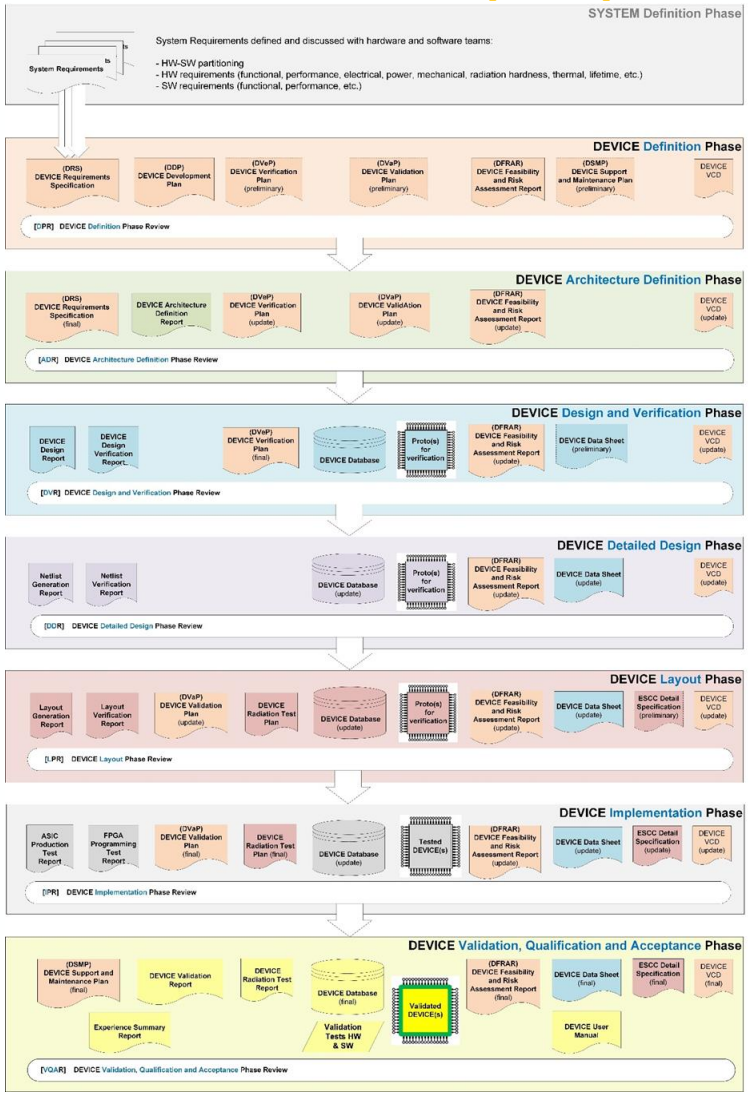
OLD

Main differences wrt Phases and Reviews

What	Why
Names of phases and reviews include the words: “**DEVICE**”, “**Phase**”	to ensure they are not mistaken with reviews of “equipment/units/systems”
Acronyms of reviews are **new** (except “DDR”), based on the actual names of the DEVICE development phases	to avoid these “DEVICE reviews” can get confused with other “equipment/units/systems reviews”
Acronyms of reviews use a subset of the initials of the phase review words, not all initials	to avoid too long acronyms (most are 3 letters)
One new phase (and its review) added between “D Definition P” and “D Design and Verification P”: “DEVICE **Architecture Definition** Phase”	to define the architecture of the DEVICE main functional blocks, hierarchies and dependencies of these blocks, their interfaces and interconnections. To facilitate the modular and detailed design of all blocks and their integration in the following phases. Its review will cover the DEVICE Requirements Spec (final), Architecture Definition Report, updated Verification and Validation Plans.
DEVICE Implementation Phase **Review added**	To review all ASIC/FPGA implementation reports and validation test plans (final) before initiating the final D Val, Qual and Acceptance P

New development flow figures

ECSS-E-ST-20-40 (2023)



old ECSS-Q-ST-60-02C (2008)

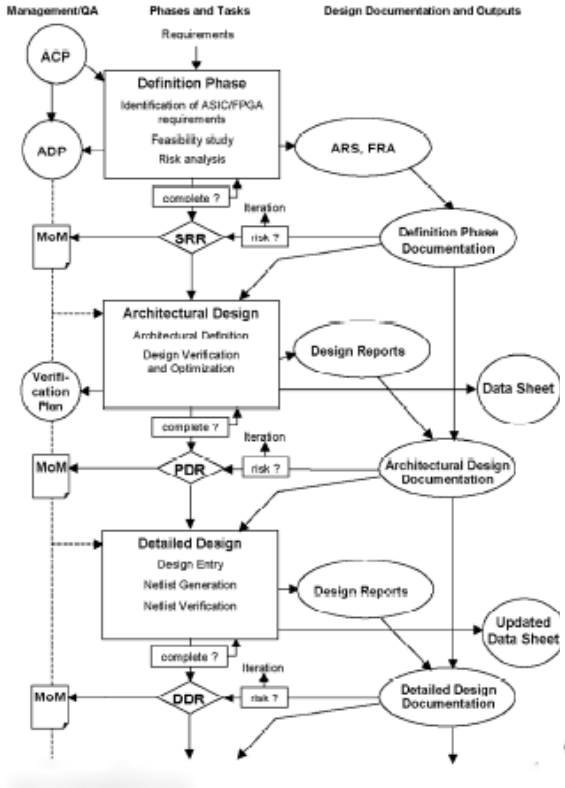


Figure 5-1: Development flow (example)

Figure 5-1 (cont'd)

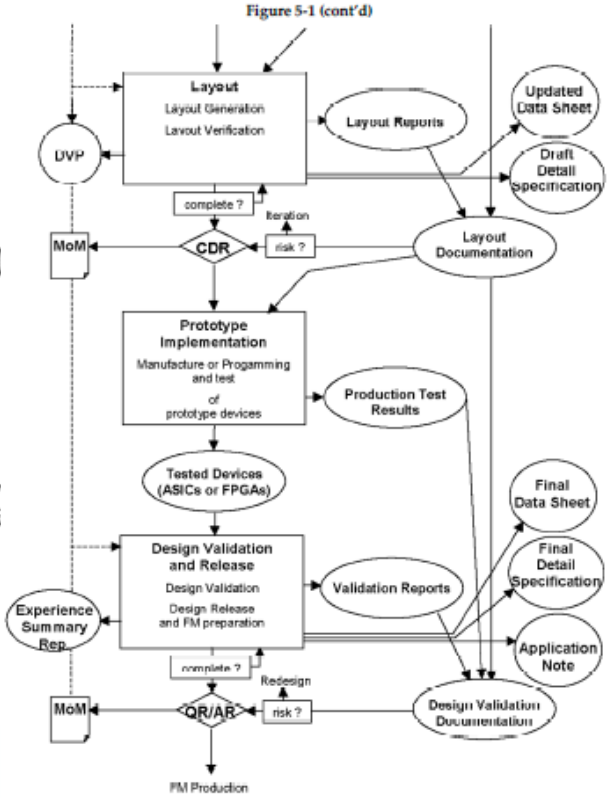
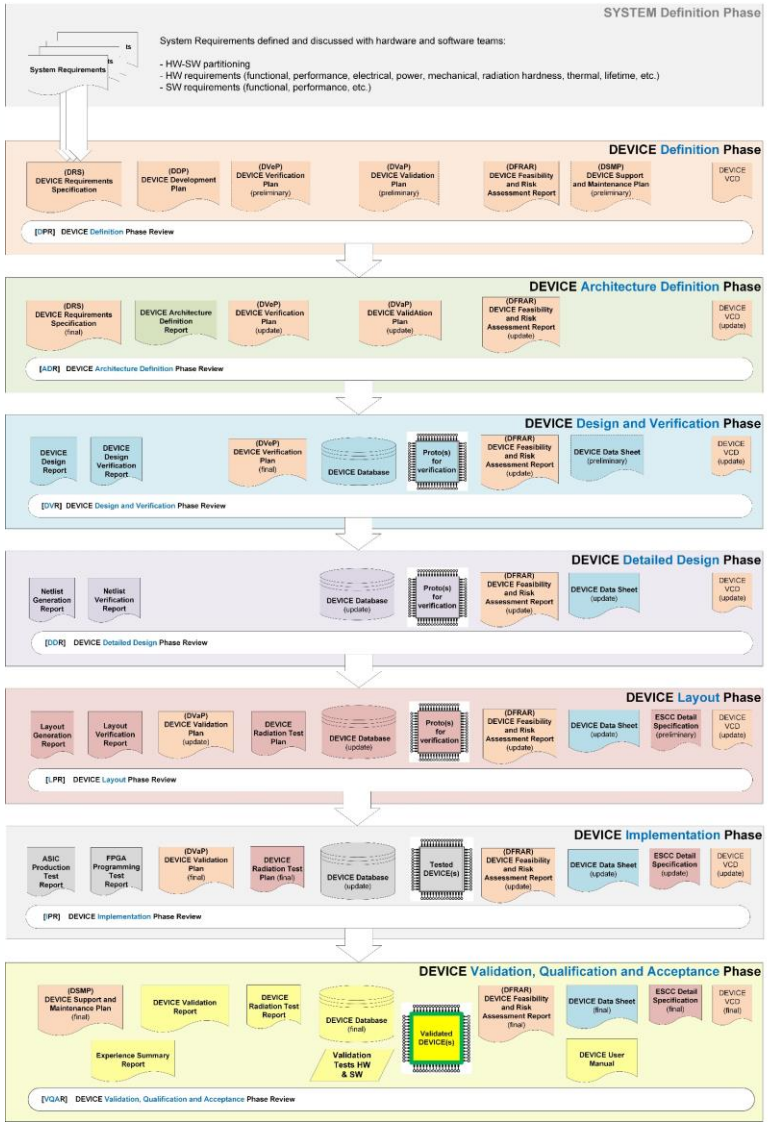


Figure 5-1: Development flow (example) – continued

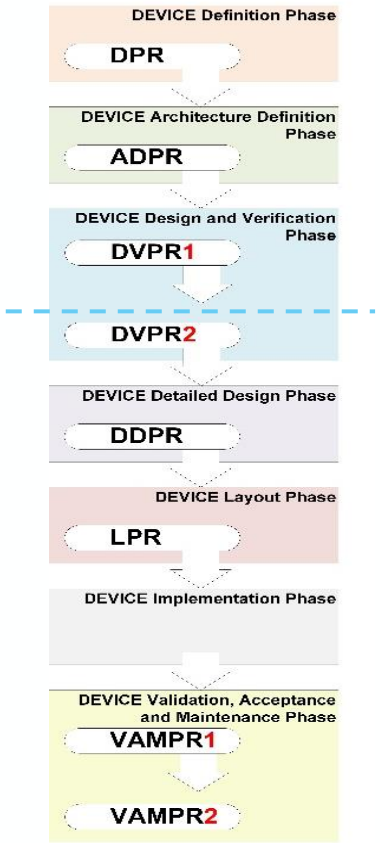
Phases, reviews, expected outputs

Generic development flow

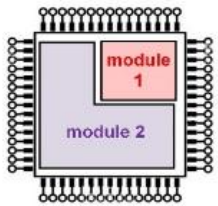


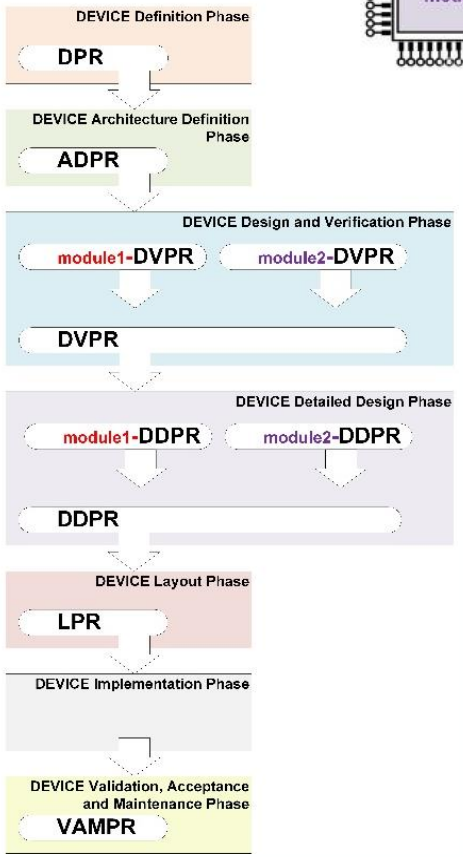
Annex J – Generic development flow variations

intermediate additional reviews

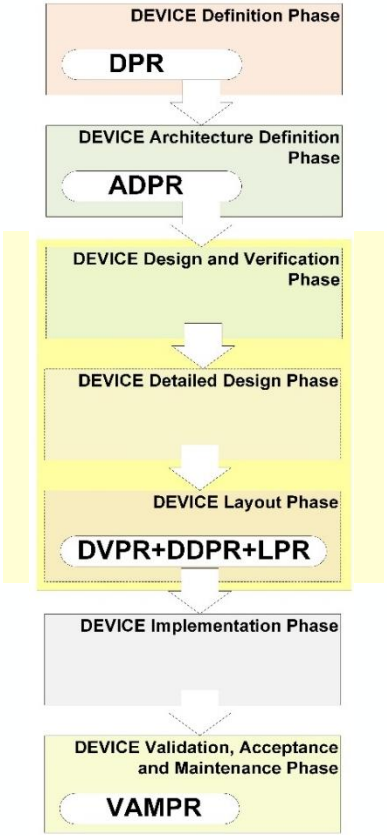


parallel modules developments and reviews

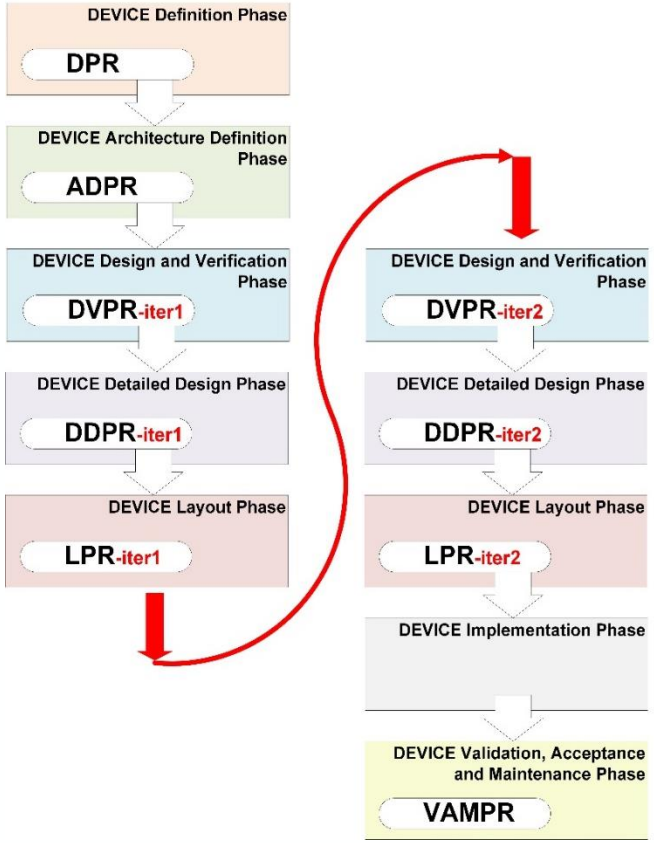




phases merging



iterations of phases



General requirements

5.1.2 Tailoring accordi

5.1.3 DEVICE engineering development flow

5.1.4 Phase Reviews

5.1.5 DEVICE Verification Contr

b. The reviewers shall analyse the preventive measures and contingency plans for all identified open issues and risk items identified in the DEVICE Feasibility and Risk Assessment to define and agree with the customer the risks that are taken for starting the next phase. **[ALL]**

c. The reviewers shall check that all expected outputs contain all the relevant information and with a level of detail that avoids ambiguity. **[ALL]**

d. Any missing information and open points and their impact on following phases shall be assessed, registered and agreed with the customer in the MoM of the phase review with an indication of the expected time of completion of the open points. **[ALL]**

General requirements

5.1.2 Tailoring according to DEVICE type

5.1.3 DEVICE engineering development fl

5.1.4 Phase Reviews

5.1.5 DEVICE Verification Control Document

a. At DEVICE Definition Phase review the supplier shall provide for customer approval an initial DEVICE VCD, in compliance with ECSS-E-ST-10-02 Annex B VDC DRD, including **[ALL]**

1. the DEVICE requirements with the combination of the selected verification and validation methods for the different verification and validation levels at the applicable development phases and the applicable verification stages.

2. The traceability between DEVICE requirements and System requirements in compliance with ECSS-E-ST-10-06 clause 8.2.3.

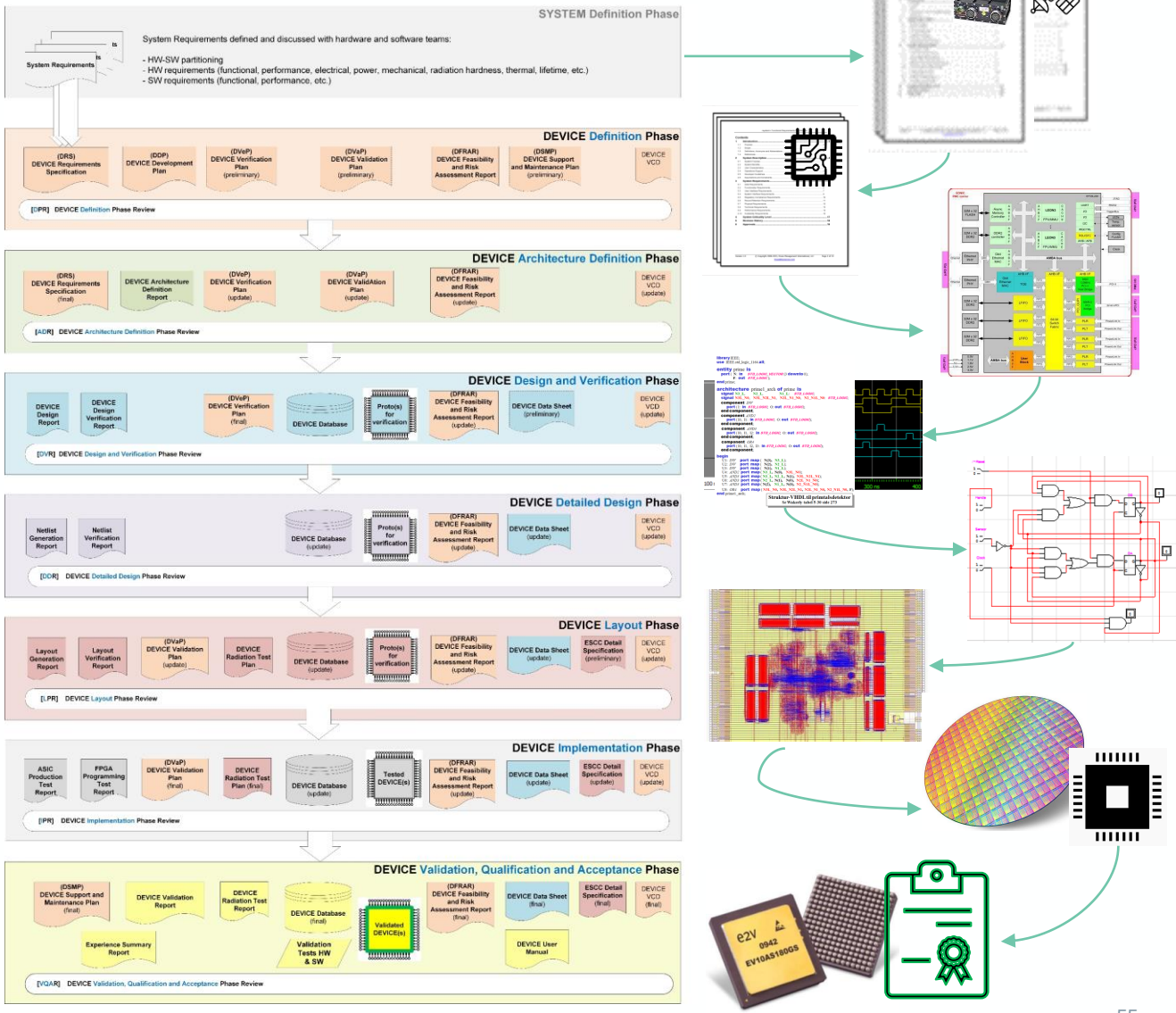
...

NOTE 3 Some verification and validation information can be found in ECSS-E-ST-20-40 reports and used to populate parts of the VCD. These reports are Design Verification Report, Netlist Verification Report, Layout Verification Report, ASIC Production Test Report, FPGA Programming Test Report, DEVICE Validation Report and Radiation Test Report.

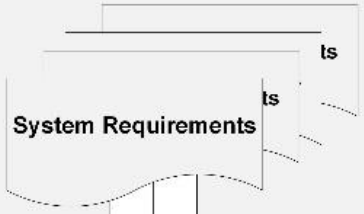
NOTE 4 References to relevant sections of the DVerP, DValP, or reports, waivers, RFD, NCR, NRB or customer closeout reports can be added to VCD to demonstrate compliance with the requirements.

Walk through the generic flow…

Generic development flow



phases, reviews and outputs (1/5)



SYSTEM Definition Phase

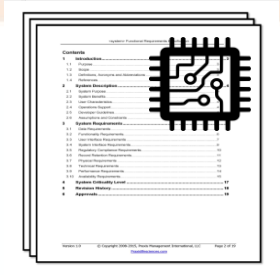
System Requirements defined and discussed with hardware and software teams:

- HW-SW partitioning
- HW requirements (functional, performance, electrical, power, mechanical, radiation hardness, thermal, lifetime, etc.)
- SW requirements (functional, performance, etc.)

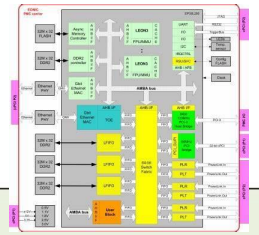
DEVICE Definition Phase

- (DRS) DEVICE Requirements Specification
- (DDP) DEVICE Development Plan
- (DVeP) DEVICE Verification Plan (preliminary)
- (DVaP) DEVICE Validation Plan (preliminary)
- (DFRAR) DEVICE Feasibility and Risk Assessment Report
- (DSMP) DEVICE Support and Maintenance Plan (preliminary)
- DEVICE VCD

[DPR] DEVICE Definition Phase Review (formerly SRR)



phases, reviews and outputs (2/5)



DEVICE Architecture Definition Phase

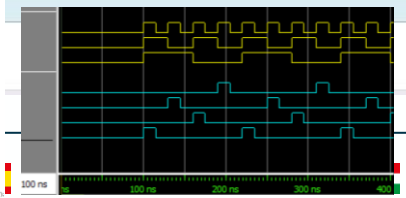
- (DRS) DEVICE Requirements Specification (final)
- DEVICE Architecture Definition Report
- (DVeP) DEVICE Verification Plan (update)
- (DVaP) DEVICE ValidAtion Plan (update)
- (DFRAR) DEVICE Feasibility and Risk Assessment Report (update)
- DEVICE VCD (update)

[ADR] DEVICE Architecture Definition Phase Review

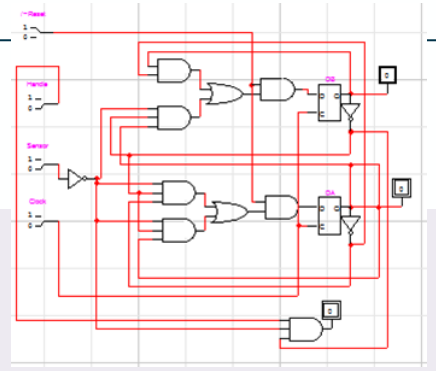
DEVICE Design and Verification Phase

- DEVICE Design Report
- DEVICE Design Verification Report
- (DVeP) DEVICE Verification Plan (final)
- DEVICE Database
- Proto(s) for verification
- (DFRAR) DEVICE Feasibility and Risk Assessment Report (update)
- DEVICE Data Sheet (preliminary)
- DEVICE VCD (update)

[DVR] DEVICE Design and Verification Phase Review (formerly PDR)



phases, reviews and outputs (3/5)



DEVICE Detailed Design Phase

Netlist Generation Report

Netlist Verification Report

DEVICE Database (update)

Proto(s) for verification

(DFRAR) DEVICE Feasibility and Risk Assessment Report (update)

DEVICE Data Sheet (update)

DEVICE VCD (update)

[DDR] DEVICE Detailed Design Phase Review (same DDR acronym as in former standard!)

DEVICE Layout Phase

Layout Generation Report

Layout Verification Report

(DVaP) DEVICE Validation Plan (update)

DEVICE Radiation Test Plan

DEVICE Database (update)

Proto(s) for verification

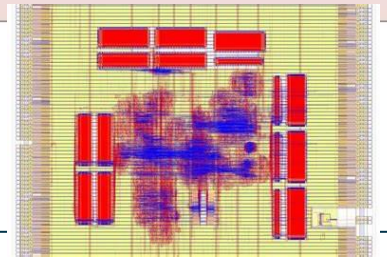
(DFRAR) DEVICE Feasibility and Risk Assessment Report (update)

DEVICE Data Sheet (update)

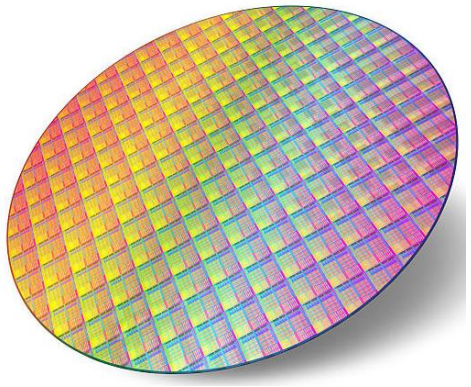
ESCC Detail Specification (preliminary)

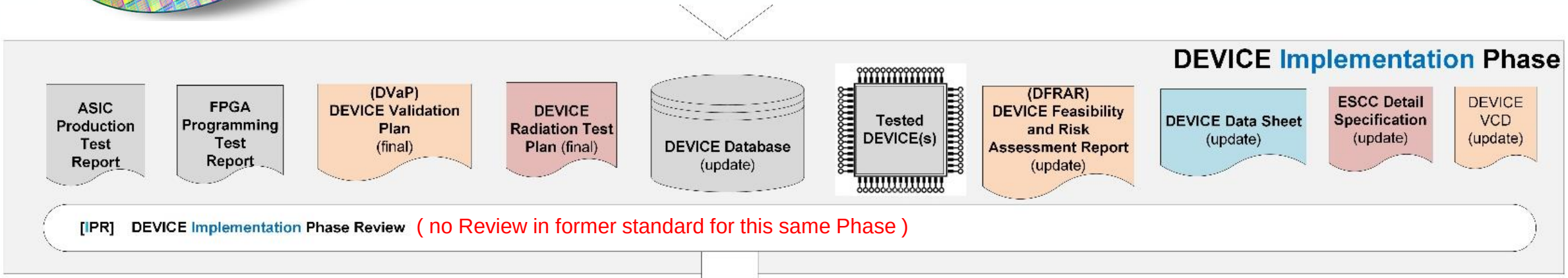
DEVICE VCD (update)

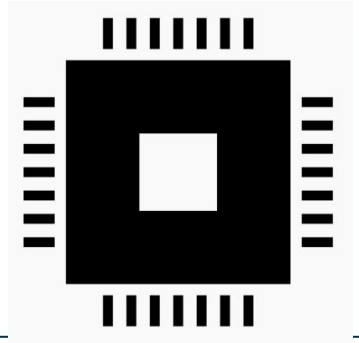
[LPR] DEVICE Layout Phase Review (formerly CDR)



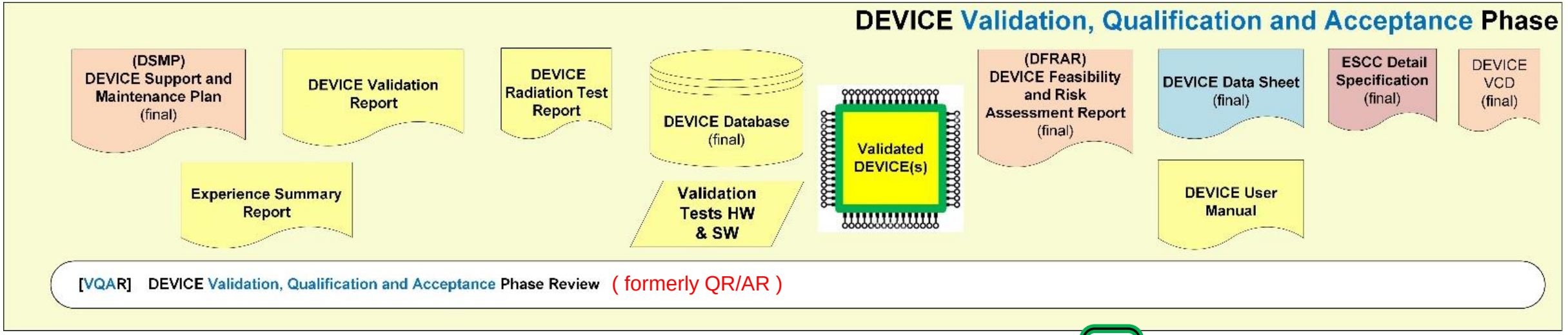
phases, reviews and outputs (4/5)

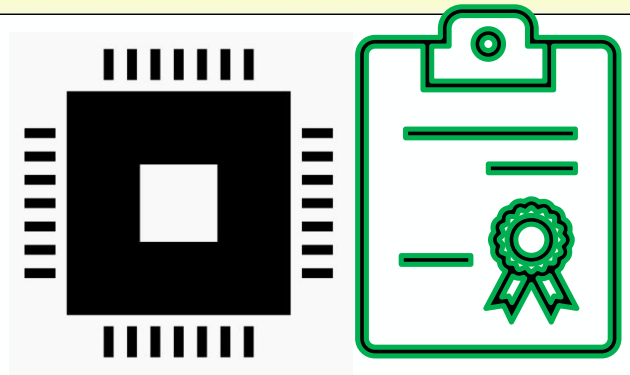






phases, reviews and outputs (5/5)





Name differences of phases, reviews and outputs (1/3)

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Definition phase	System Requirements Review **(SRR)**	a. the definition phase documentation, containing: 1. ASIC and FPGA requirements specification (ARS); 2. Feasibility and risk analysis (FRA); b. ASIC and FPGA development plan (ADP); c. MoM of SRR.	a) DEVICE Requirements Specification (DRS) b) DEVICE Feasibility and Risk Assessment Report (DFRAR) c) DEVICE Development Plan (DDP) d) DEVICE Verification Plan (DVeP) (preliminary) e) DEVICE Validation Plan (DVaP) (preliminary) f) DEVICE Verification Control Document (VCD) **g)** DEVICE Support and Maintenance Plan (DSMP) (preliminary)	**DEVICE Definition** Phase Review **(DPR)**	**DEVICE Definition** Phase
Architectural design	Preliminary Design Review **(PDR)**	a. Architecture definition report; b. Verification plan; c. Architecture verification and optimization report; d. Preliminary data sheet; e. Design database, containing: 1. Simulation models; 2. Verification results; f. MoM of PDR.	a) DEVICE Architecture Definition Report b) DRS (final) c) DVeP (update) d) DVaP (update) e) DFRAR (update) f) VCD (update)	**DEVICE Architecture Definition** Phase Review **(ADR)**	**DEVICE Architecture Defi** Phase
			a) DVeP (final) b) DEVICE Design Report c) DEVICE Design Verification Report d) DEVICE Data Sheet (DS) (preliminary) e) DEVICE database f) DFRAR (update) g) VCD (update)	**DEVICE Design and Verification** Phase Review **(DVR)**	**DEVICE Design and Verifi** Phase

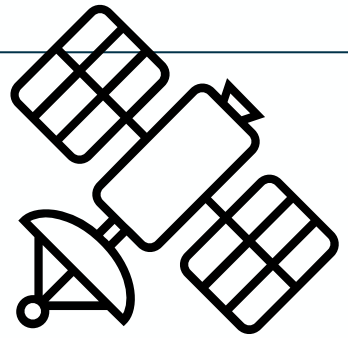
Name differences of phases, reviews and outputs (2/3)

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Detailed design	Detailed Design Review **(DDR)**	a. Design entry report; b. Netlist generation report; c. Netlist verification report; d. Updated data sheet with pin-out; e. Updated design database, containing: 1. Pre-layout netlist; 2. Constraints for layout (i.e. floorplan and constraints for timing driven layout) as defined in the ADP; 3. Test vectors for production test; f. MoM of DDR.	a) Netlist Generation Report b) Netlist Verification Report c) DEVICE Data Sheet (update) d) DEVICE Database (update) e) VCD (update) f) DFRAR (update)	**DEVICE Detailed Design** Phase Review **(DDR)**	**DEVICE Detailed Design** Phase
Layout	Critical Design Review **(CDR)**	a. Layout generation report; b. Layout verification report; c. Design validation plan; d. Updated data sheet; e. Updated design database, containing: 1. Post-layout netlist in the agreed format depending on the targeted technological approach (GDS II, FPGA P&R files or other); 2. Corresponding parasitic information; f. MoM of CDR.	a) Layout Generation Report b) Layout Verification Report c) DVaP (update) d) DEVICE Radiation Test Plan e) DEVICE Data Sheet (update) f) ESCC Detail Specification (preliminary) g) DEVICE database (update) h) VCD (update) i) DFRAR (update)	**DEVICE Layout** Phase Review **(LPR)**	**DEVICE Layout** Phase

Name differences of phases, reviews and outputs (3/3)

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Prototype implementation	n/a	a. Agreed number of tested devices (ASICs or FPGAs); b. Production test results and reports; [not applicable for FPGA designs] ; c. Burn-in or any other production test results, specifications and patterns.	a) DVaP (final) b) DEVICE Radiation Test Plan (final) c) ASIC Production Test Report or d) FPGA Programming Tests Report e) DEVICE Data Sheet (update) f) DEVICE Detail Specification (update) g) DEVICE database (update) h) VCD (update) i) DFRAR (update) j) Tested DEVICEs	**DEVICE Implementation** Phase Review **(IPR)**	**DEVICE Implementation Phase**
Design validation and release	Qualification snf Acceptance Review **(QAR)**	a. Validation report; b. Radiation test report (if applicable); c. Release report; d. Experience summary report; e. Final data sheet; f. Final detail specification; g. Application note; h. MoM of QR/AR; i. Validation breadboard; j. Burn-in or screening test boards for FM parts.	a) DEVICE Validation Report b) DEVICE Radiation Test Report c) Experience Summary Report d) DEVICE Data Sheet (final) e) ESCC Detail Specification (final) f) DEVICE User Manual g) VCD (final) h) DFRAR (final) i) DSMP (final) j) DEVICE Database (final) k) Validation tests HW and SW l) Tested and validated DEVICEs	**DEVICE Validation, Qualification and Acceptance** Phase Review **(VQAR)**	**DEVICE Validation, Qualification and Acceptance** Phase

Equipment/Systems vs DEVICEs development life cycles



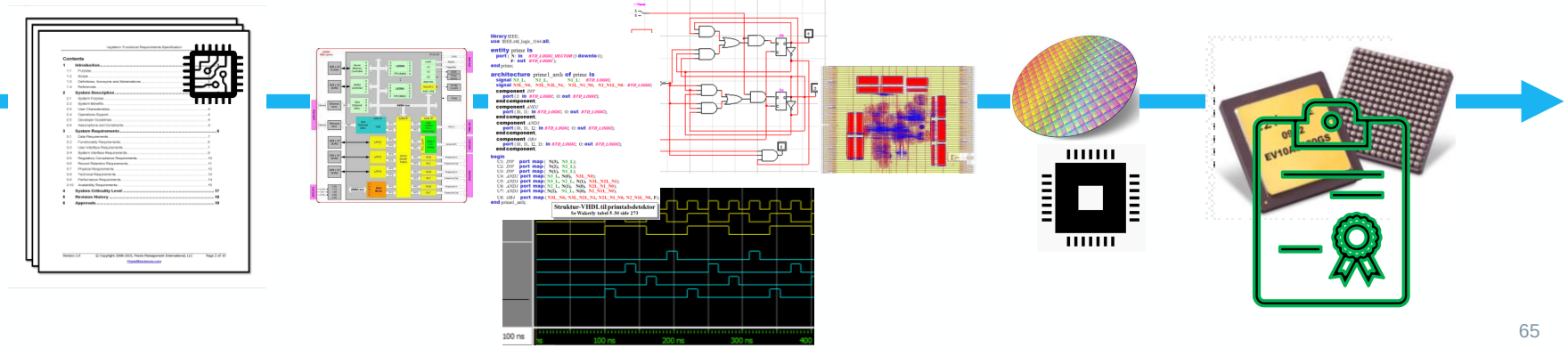
1 - How do DEVICE development milestones **align in time** with the development milestones of the system(s) where the DEVICE will be used? -> no predefined alignment

2 - Is the **milestone terminology** the same for DEVICE and for equipment/system developments? -> NO

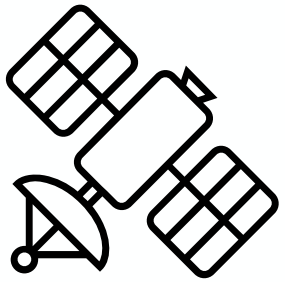
phase and milestone names of ECSS-E-ST-20-40 are unique, only for DEVICE (ASIC, FPGA, IP Cores) developments

ECSS-E-ST-20-40C **ASIC, FPGA and IP Core Engineering**	**Phases**	DEVICE Definition Phase	DEVICE Architecture Definition Phase	DEVICE Design and Verification Phase	DEVICE Detailed Design Phase	DEVICE Layout Phase	DEVICE Implementation Phase	DEVICE Validation, Qualification and Acceptance Phase
	Reviews	DEVICE Definition Phase Review **(DPR)**	DEVICE Architecture Definition Phase Review **(ADR)**	DEVICE Design and Verification Phase Review **(DVR)**	DEVICE Detailed Design Phase Review **(DDR)**	DEVICE Layout Phase Review **(LPR)**	DEVICE Implementation Phase Review **(IPR)**	DEVICE Validation, Qualification and Acceptance Phase Review **(VQAR)**
	outputs	•DEVICE Requirements Specification (DRS) •DEVICE Development Plan (DDP) •	•DEVICE Architecture Definition Report •DRS (update) •	•DEVICE Verification Plan (final) •DEVICE Design Verification Report **•DEVICE Data Sheet (preliminary)** •	•Netlist Generation and Verification Reports **•DEVICE Data Sheet (update)** •	•Layout Generation and Verification Reports **•DEVICE Data Sheet (update)** •	**•Tested DEVICEs** •ASIC Production Tests Report •FPGA Programming Test Report •DEVICE Validation Phase (final) •DEVICE Radiation Test Plan (final) **•DEVICE Data Sheet (update)** •	•DEVICE Validation Report **•DEVICE Radiation Test Report** **•Validated DEVICEs** •DEVICE database (final) **•DEVICE Support and Maintenance Plan (final)** **•DEVICE Data Sheet (final)** **•DEVICE User Manual** **•VCD (final)**

TIME



phase and milestone terminology of ECSS-M-ST-10 (systems, sub-systems development) is different than that used in ECSS-E-ST-20-40



ECSS-M-ST-10C Project Planning and Implementation	outputs needed for DEVICE development		**System** (Equipment HW and SW, environmental) **Requirements for the DEVICE**										
	Reviews	Mission Definition Review **(MRR)**	Preliminary Requirements Review **(PRR)**	System Requirements Review **(SRR)**	Preliminary Design Review **(PDR)**	Critical Design Review **(CDR)**	Qualification Review **(QR)**	Acceptance Review **(AR)**	Operations Readiness Review (ORR)	Flight readiness Review (FRR)	Launch Readiness Review (LRR)	Commissioning Result Review (CRR)	End of Life Review (ELR)
	Phases	**0** Mission analysis/needs identification	**A** Feasibility	**B** Preliminary Definition		**C** Detailed Definition	**D** Qualification and Production		**E** Utilization				**F** Disposal

TIME

Annex L: Equivalence of phase and milestone terminology of ECSS-M-ST-10 (systems, sub-systems) and ECSS-E-ST-20-40 (DEVICES)

ECSS-E-ST-20-40C ASIC, FPGA and IP Core Engineering	DEVICE Definition Phase	DEVICE Architecture Definition Phase	DEVICE Design and Verification Phase	DEVICE Detailed Design Phase	DEVICE Layout Phase	DEVICE Implementation Phase	DEVICE Validation, Qualification and Acceptance Phase
Phases							
Reviews	DEVICE Definition Phase Review **(DPR)**	DEVICE Architecture Definition Phase Review **(ADR)**	DEVICE Design and Verification Phase Review **(DVR)**	DEVICE Detailed Design Phase Review **(DDR)**	DEVICE Layout Phase Review **(LPR)**	DEVICE Implementation Phase Review **(IPR)**	DEVICE Validation, Qualification and Acceptance Phase Review **(VQAR)**
outputs	• DEVICE Requirements Specification (DRS) • DEVICE Development Plan (DDP) •	• DEVICE Architecture Definition Report • DRS (update) •	• DEVICE Verification Plan (final) • DEVICE Design Verification Report • **DEVICE Data Sheet (preliminary)** •	• Netlist Generation and Verification Reports • **DEVICE Data Sheet (update)** •	• Layout Generation and Verification Reports • **DEVICE Data Sheet (update)** •	• **Tested DEVICEs** • ASIC Production Tests Report • FPGA Programming Test Report • DEVICE Validation Phase (final) • DEVICE Radiation Test Plan (final) • **DEVICE Data Sheet (update)** •	• DEVICE Validation Report • **DEVICE Radiation Test Report** • **Validated DEVICEs** • DEVICE database (final) • **DEVICE Support and Maintenance Plan (final)** • **DEVICE Data Sheet (final)** • **DEVICE User Manual** • VCD (final)

TIME

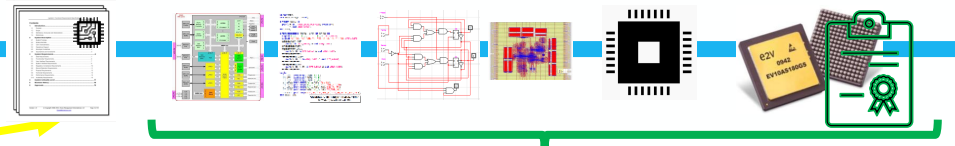
ECSS-M-ST-10C Project Planning and Implementation														
outputs needed for DEVICE development		**System** (Equipment HW and SW, environmental) **Requirements for the DEVICE**												
Reviews	Mission Definition Review **(MRR)**	Preliminary Requirements Review **(PRR)**	System Requirements Review **(SRR)**	Preliminary Design Review **(PDR)**	Critical Design Review **(CDR)**	Qualification Review **(QR)**	Acceptance Review **(AR)**	Operations Readiness Review (ORR)	Flight readiness Review (FRR)	Launch Readiness Review (LRR)	Commissioning Result Review (CRR)	End of Life Review (ELR)		
Phases	**0** Mission analysis/needs identification	**A** Feasibility	**B** Preliminary Definition		**C** Detailed Definition	**D** Qualification and Production		**E** Utilization					**F** Disposal	

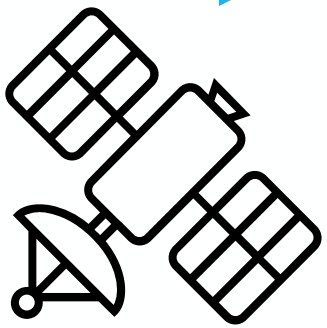
equipment (ECSS-M-ST-10) vs DEVICEs (ECSS-E-ST-20-40) development life cycles: **no pre-defined standardized alignment!**

DEVICE Definition Phase	DEVICE Architecture Definition Phase	DEVICE Design and Verification Phase	DEVICE Detailed Design Phase	DEVICE Layout Phase	DEVICE Implementation Phase	DEVICE Validation, Qualification and Acceptance Phase
DEVICE Definition Phase Review **(DPR)**	DEVICE Architecture Definition Phase Review **(ADR)**	DEVICE Design and Verification Phase Review **(DVR)**	DEVICE Detailed Design Phase Review **(DDR)**	DEVICE Layout Phase Review **(LPR)**	DEVICE Implementation Phase Review **(IPR)**	DEVICE Validation, Qualification and Acceptance Phase Review **(VQAR)**
•DEVICE Requirements Specification (DRS) •DEVICE Development Plan (DDP) •	•DEVICE Architecture Definition Report •DRS (update) •	•DEVICE Verification Plan (final) •DEVICE Design Verification Report •**DEVICE Data Sheet (preliminary)** •	•Netlist Generation and Verification Reports •**DEVICE Data Sheet (update)** •	•Layout Generation and Verification Reports •**DEVICE Data Sheet (update)** •	•**Tested DEVICEs** •ASIC Production Tests Report •FPGA Programming Test Report •DEVICE Validation Phase (final) •DEVICE Radiation Test Plan (final) •**DEVICE Data Sheet (update)** •	•DEVICE Validation Report •**DEVICE Radiation Test Report** •**Validated DEVICEs** •DEVICE database (final) •**DEVICE Support and Maintenance Plan (final)** •**DEVICE Data Sheet (final)** •**DEVICE User Manual** •VCD (final)

Every project, satellite, sub-system to align schedules with DEVICE(s) development(s) as needed

TIME





System (Equipment HW and SW, environmental**) Requirements for the DEVICE**

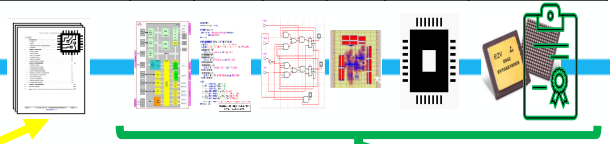
Preliminary Requirements Review **(PRR)**	System Requirements Review **(SRR)**	Preliminary Design Review **(PDR)**	Critical Design Review **(CDR)**	Qualification Review **(QR)**	Acceptance Review **(AR)**
A Feasibility	**B** Preliminary Definition		**C** Detailed Definition	**D** Qualification and Production	

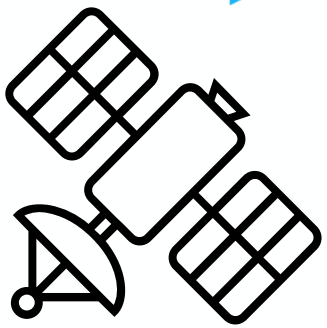
equipment vs DEVICEs development life cycles: **no pre-defined alignment!**

Example 1: early DEVICE development start wrt equipment development

DEVICE Definition Phase	DEVICE Architecture Definition Phase	DEVICE Design and Verification Phase	DEVICE Detailed Design Phase	DEVICE Layout Phase	DEVICE Implementation Phase	DEVICE Validation, Qualification and Acceptance Phase
DEVICE Definition Phase Review **(DPR)**	DEVICE Architecture Definition Phase Review **(ADR)**	DEVICE Design and Verification Phase Review **(DVR)**	DEVICE Detailed Design Phase Review **(DDR)**	DEVICE Layout Phase Review **(LPR)**	DEVICE Implementation Phase Review **(IPR)**	DEVICE Validation, Qualification and Acceptance Phase Review **(VQAR)**
•DEVICE Requirements Specification (DRS) •DEVICE Development Plan (DDP) •ΔΣ	•DEVICE Architecture Definition Report •DRS (update) •ΔΣ	•DEVICE Verification Plan (final) •DEVICE Design Verification Report •**DEVICE Data Sheet (preliminary)** •ΔΣ	•Netlist Generation and Verification Reports •**DEVICE Data Sheet (update)** •ΔΣ	•Layout Generation and Verification Reports •**DEVICE Data Sheet (update)** •ΔΣ	•**Tested DEVICEs** •ASIC Production Tests Report •FPGA Programming Test Report •DEVICE Validation Phase (final) •DEVICE Radiation Test Plan (final) •**DEVICE Data Sheet (update)** •ΔΣ	•DEVICE Validation Report •**DEVICE Radiation Test Report** •**Validated DEVICEs** •DEVICE database (final) •**DEVICE Support and Maintenance Plan (final)** •**DEVICE Data Sheet (final)** •**DEVICE User Manual** •**WCD (final)**

TIME



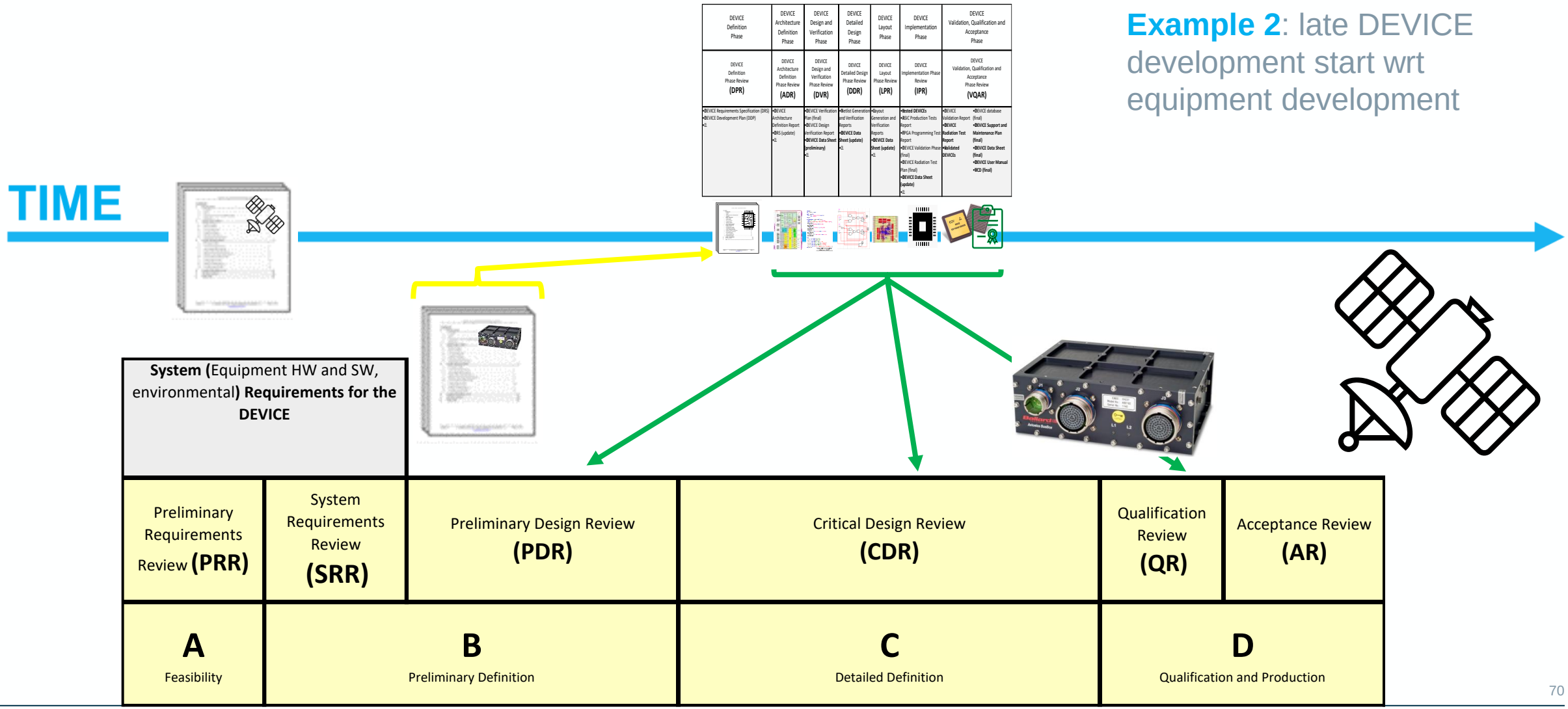


System (Equipment HW and SW, environmental**) Requirements for the DEVICE**

Preliminary Requirements Review **(PRR)**	System Requirements Review **(SRR)**	Preliminary Design Review **(PDR)**	Critical Design Review **(CDR)**	Qualification Review **(QR)**	Acceptance Review **(AR)**
A Feasibility	**B** Preliminary Definition		**C** Detailed Definition	**D** Qualification and Production	

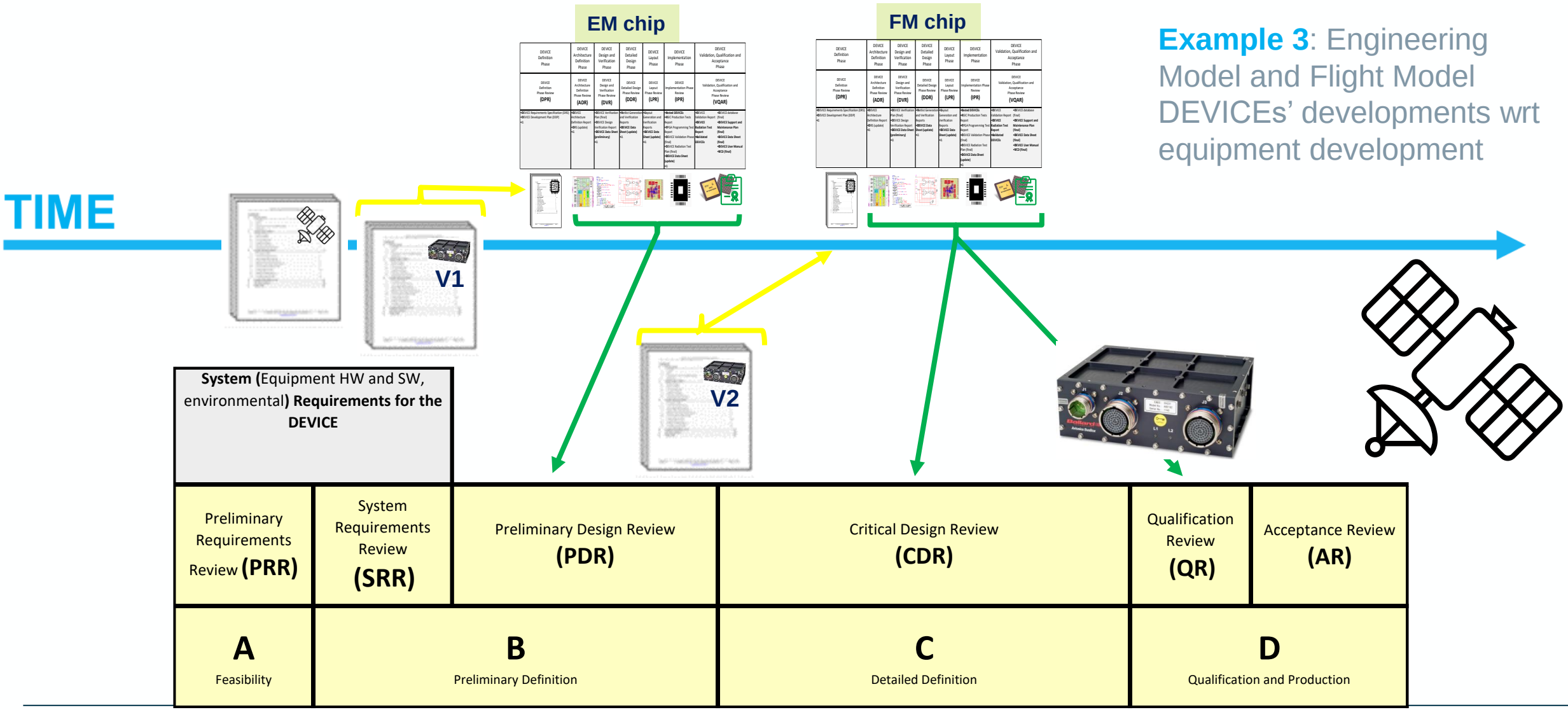
equipment vs DEVICEs development life cycles: **no pre-defined alignment**!

Example 2: late DEVICE development start wrt equipment development



equipment vs DEVICEs development life cycles: **no pre-defined alignment**!

Example 3: Engineering Model and Flight Model DEVICEs' developments wrt equipment development



Applying the standards and some challenges (1/2)

- **2 standards to be applied** in parallel: E-ST-20-40C Engineering and Q-ST-60-03 Product Assurance requirements and expected outputs (one same flow and set of reviews for both E and Q standards)

- E-ST-20-40C Engineering **std is the backbone**, PA complements and successful compliance to both results in acceptance of “ECSS-qualified” DEVICE by customer

- ESA Microelectronics section (TEC-EDM) experts will supervise ASIC, FPGA and IP Core developments for ESA projects and R&D activities for an optimal application and tailoring of the ECSS-ST-20-40 Engineering standard in each specific development case. And coordinated and collaborating with them, ESA Quality, Dependability and PA support division experts will ensure the correct application and tailoring of ECSS-Q-ST-60-03.

Applying the standards and some challenges (2/2)

- We all will learn to **optimize tailoring** (in addition to the pre-tailoring already contained in the standards):
  - For each specific DEVICE **type case** (perhaps new Handbooks will follow to guide with pre-tailored flows for popular DEVICE type development cases: A-ASIC, SRAM and Flash and OTP FPGAs, etc.)
  - Depending on **DEVICE criticality** and **project resources**. For example, pure “R&D DEVICE” developments may apply only the **E-20-40 std**, while high criticality DEVICES to be flown in ESA missions will be developed applying both E and Q stds.
  - **Coordination and collaboration between DEVICE engineers (designers) and PA engineers** from both, the customer (ESA, Agencies, Primes) and the supplier (ASIC/FPGA/IP Core design companies) sides will be needed when both standards are tailored and applied.
  - To minimize the impact on work and cost due to redundant requirements in the E and Q standards, which were left to comply with higher-level ECSS standards, additional tailoring can be done. This can be achieved by ensuring that activity plans and results that may be required from clauses in both the E and Q standards are documented only once and in a single document agreed upon by the customer and supplier.

- **Change Requests** to improve these standards can be submitted through the ECSS website pages of each standard (click on “CR” button in the web page of the standard)

Where to find the standards, handbook and more

ECSS website

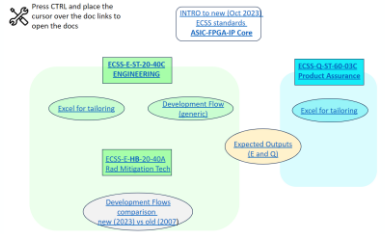
- ECSS-E-ST-20-40C – ASIC, FPGA and IP Core engineering (11 October 2023) | European Cooperation for Space Standardization
- ECSS-Q-ST-60-03C – ASIC, FPGA and IP Core product assurance (11 October 2023) | European Cooperation for Space Standardization
- ECSS-E-HB-20-40A – Engineering techniques for radiation effects mitigation in ASICs and FPGAs handbook | European Cooperation for Space Standardization

ESA Microelectronics Development Methodology webpage)

ESA - Microelectronics Development Methodology

(internal to ESA only) “EMTO” Microsoft ESA365 Team

https://teams.microsoft.com/l/channel/19%3a39584d2329a644edb65d73c6b21d81f1%40thread.tacv2/ASIC%252C%2520FPGA%252C%2520IP%2520Core%2520ECSS%2520Toolbox?groupId=dcf394aa-9aaf-44d6-8456-fc433299e043&tenantId=9a5cacd0-2bef-4dd7-ac5c-7ebe1f54f495



CONCLUDING

public info + Q&A webinars/mtgs can be organised on request to explain the new stds, answer questions and help with their adoption, transition from the old to the new stds.

THANKS for your attention,

QUESTIONS?

agustin.fernandez-leon[at]esa.int (ECSS-E-ST-20-40 book captain)
isabelle.Conway[at]esa.int (ECSS-Q-ST-60-03 book captain)