ECSS-Q-HB-60-02

HANDBOOK

"Techniques for Radiation Effects Mitigation in ASICs and FPGAs"

A. Fernández León
Microelectronics Section
ESA / ESTEC

OUTLINE

- **Scope and goals of Handbook**
- **When and who prepared this Handbook?**
- **Classification of mitigation techniques, structure of HB**
- **Overview of main chapters (lists of techniques)**

Deciphering the handbook coded name

Space product assurance (branch “Q”)

ECSS-Q-HB-60-02

Handbook

EEE Components (discipline “60”)

“Techniques for Radiation Effects Mitigation in ASICs and FPGAs”

ECSS-Q-HB-60-02 scope and goals

compilation of

techniques to mitigate effects of radiation in ASICs & FPGAs
techniques **grouped** according to the different stages (levels) of an IC development flow

in addition

- overview of the space radiation environment and its effects in ICs
- general guidelines for selecting techniques , how to use the handbook
- how to validate the mitigation techniques

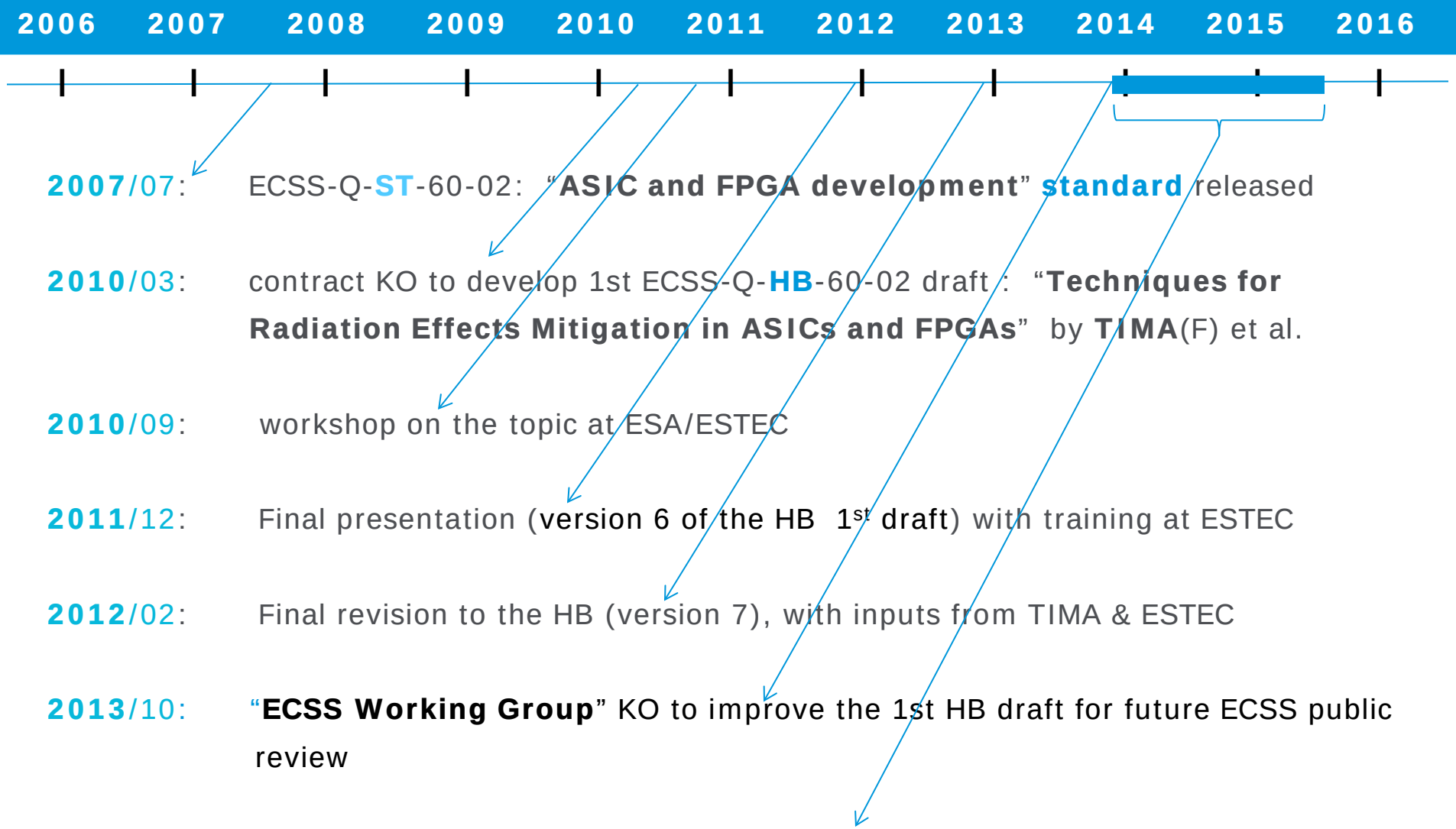
intended users

Engineers and IC designers doing selection, use or development of ASIC or FPGA to be used in radiation environment

Intended use

As guidelines and references only, not requirements

History of ECSS-Q-HB-60-02



2007/07: ECSS-Q-**ST**-60-02: "**ASIC and FPGA development**" **standard** released

2010/03: contract KO to develop 1st ECSS-Q-**HB**-60-02 draft : "**Techniques for Radiation Effects Mitigation in ASICs and FPGAs**" by **TIMA**(F) et al.

2010/09: workshop on the topic at ESA/ESTEC

2011/12: Final presentation (version 6 of the HB 1st draft) with training at ESTEC

2012/02: Final revision to the HB (version 7), with inputs from TIMA & ESTEC

2013/10: "**ECSS Working Group**" KO to improve the 1st HB draft for future ECSS public review

2014-today: ECSS Working Group and Secretariat preparing improved HB draft

Who worked in the ECSS-Q-HB-60-02 ?

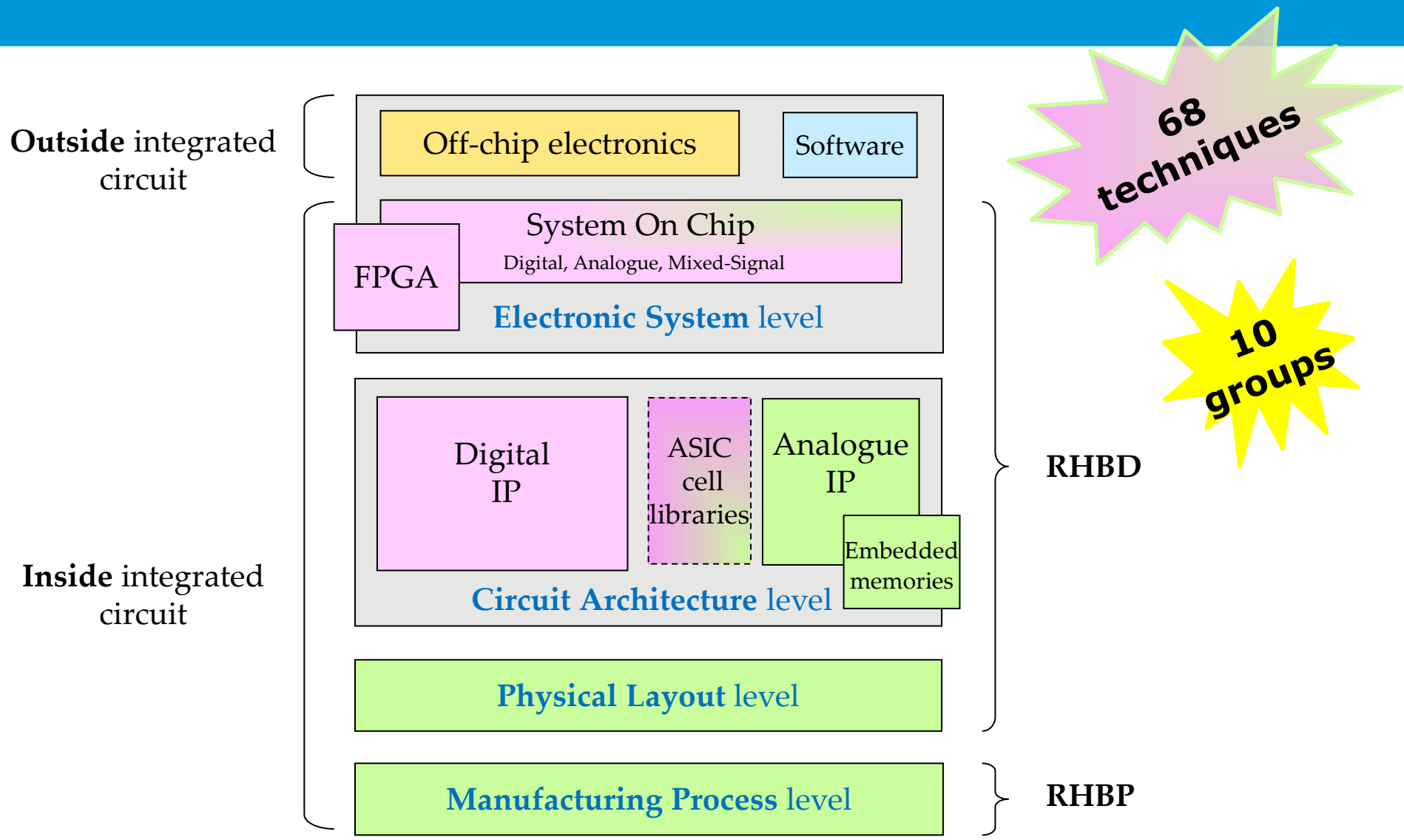
First HB draft (2012 Q1) put together by **TIMA (F)**, under **ESA** contract, with key inputs from:

M. Alles	University of Vanderbilt (USA)	process and layout level
D. Loveless		analogue & mixed-signal circuits
M. Nicolaidis	**TIMA** (F)	digital circuits
R. Velazco		HB contract manager
B. Glass	**European Space Agency** (NL)	
F. L. Kastensmidt	Universidade Federal do Rio Grande do Sul (Brazil)	Digital circuits and FPGAs
M. Violante	Politecnico di Torino (I)	Embedded Software
M. Pignol	CNES (F)	System architecture

Final HB version (2015 Q3) by the ECSS WG with inputs/corrections from **ESA, Thales, AirbusDS, RUAG, OHB, CNES(F), CERN(CH) and IMEC(B)** ….and **anyone interested** through “Public Review”

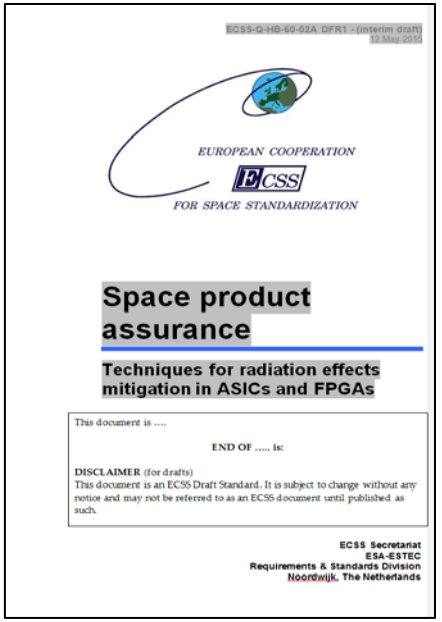
Over 350 citations of industry, academia, vendors and agencies worldwide

classification of mitigation techniques, abstraction levels



Handbook table of contents

size (pages)	chapter #	chapter title
	1	Scope
10	2	References
	3	Terms, definitions and abbreviated terms
5	4	Radiation environment and integrated circuits
2	5	Choosing a design hardening strategy
15	6	**Technology selection and process level mitigation**
12	7	**Layout**
29	8	**Analogue circuits**
22	9	**Embedded memories**
6	10	**Radiation-hardened ASIC libraries**
20	11	**Digital Circuits**
18	12	**System on a Chip**
26	13	**Field Programmable Gate Arrays**
15	14	**Software-implemented hardware fault tolerance**
17	15	**System architecture**
25	16	**Validation methods**
33	Annex A	Bibliography
3	Annex B	Vendor Solutions

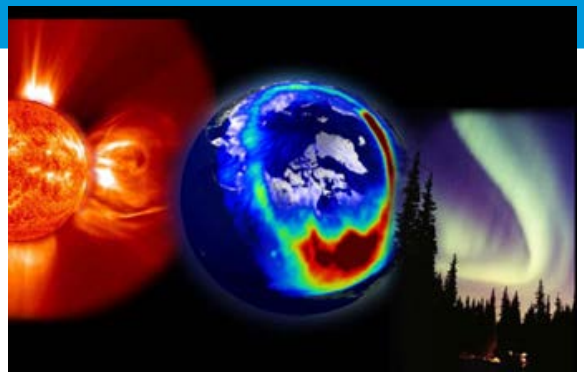


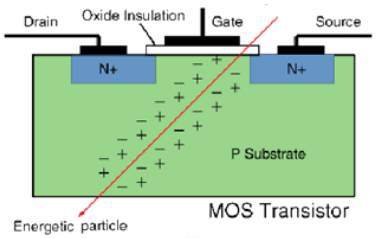
ECSS-Q-HB-60-02 Version 9 (May 2015)

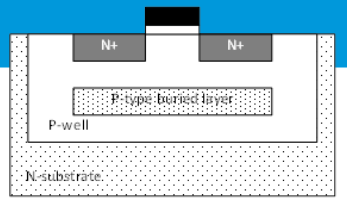
Common structure of main chapters

a. Overview
b. Table of Mit. Techniques vs. Rad Effects
c. Mitigation techniques descriptions, with examples, figures…
   - Available Test Data (simulations, radiation testing, in-flight)
   - Added value (efficiency)
   - Known issues (Weaknesses, elements to be considered)
   - “ID card”
     - Abstraction level
     - Pros
     - Cons
     - Mitigated effects
     - Validation Methods
     - Automation tools
     - Vendor solutions

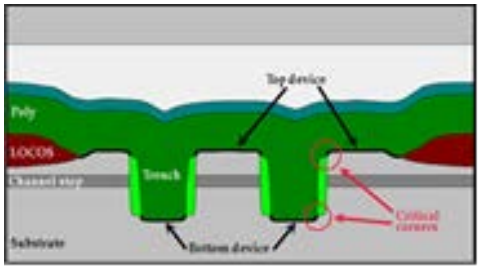
ECSS-Q-HB-60-02: the first chapters

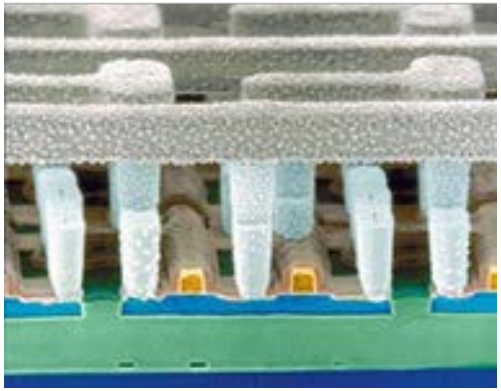




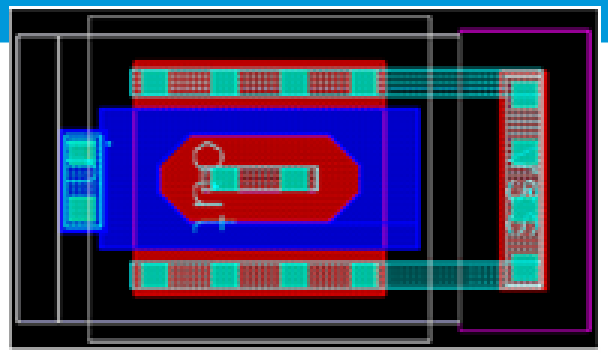


6 Technology selection and process level mitigation





7 Layout, 8 Analogue circuits



7 Layout

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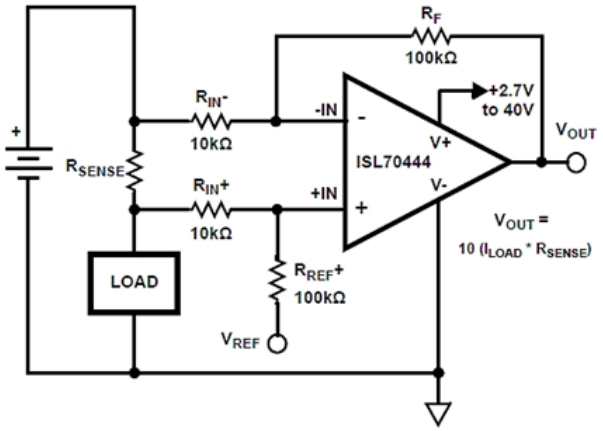
7.3.1 Ringed or Enclosed Layout Transistor
7.3.2 Contacts and guard rings
7.3.3 Dummy transistors
7.3.4 Large W/L ratio transistors



8 Analogue circuits

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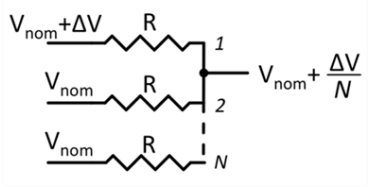
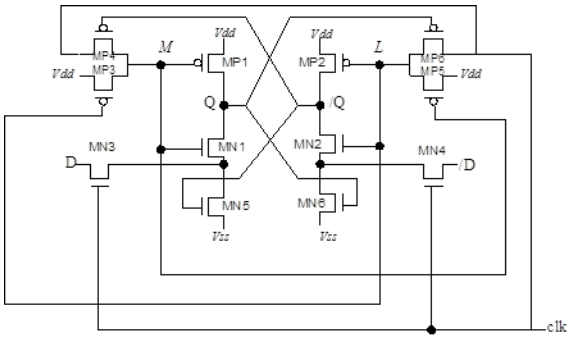
8.3.1 Node Separation and Inter-digitation
8.3.2 Analogue Redundancy (Averaging)
8.3.3 Resistive Decoupling
8.3.4 Filtering
8.3.5 Modifications in Bandwidth, Gain, Operating Speed, and Current Drive
8.3.6 Reduction of Window of Vulnerability
8.3.7 Reduction of High Impedance Nodes
8.3.8 Differential Design
8.3.9 Dual Path Hardening

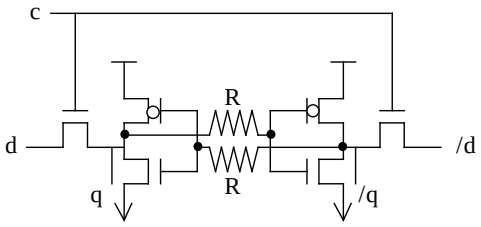


9.3.1 Hardening of individual Memory Cells



9.3.1.1 Resistive hardening
9.3.1.2 Capacitive hardening
9.3.1.3 IBM hardened memory cell
9.3.1.4 HIT hardened memory cell
9.3.1.5 DICE hardened memory cell
9.3.1.6 NASA-Whitaker hardened memory cell
9.3.1.7 NASA-Liu hardened memory cell

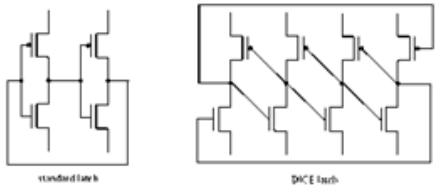
9.3.2 Bit-interleaving in memory arrays

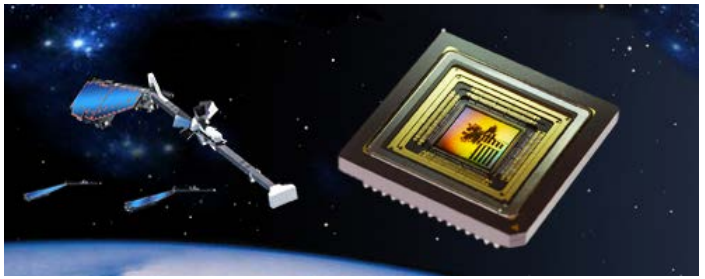


9.3.3 Data Scrubbing

9.4 Comparison between hardened memory cells

10 Radiation-hardened ASIC libraries

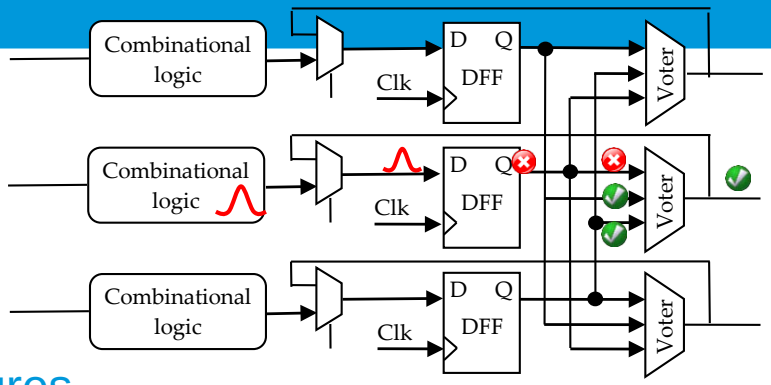




10.1 IMEC Design Against Radiation Effects (DARE) 0.18 µm library
10.2 CERN 0.25 µm, 65nm rad hard library
10.3 BAE 0.15 µm rad hard library
10.4 Ramon Chips 0.18 µm and 0.13 µm rad hard libraries
10.5 Aeroflex 600, 250, 130 and 90 nm rad hard libraries
10.6 Atmel MH1RT, ATC18RHA, ATMX150RHA (0.35, 0.18 & 0.15 µm) rad hard lib
10.7 ATK 0.35 µm rad hard cell library
10.8 ST Microelectronics C65SPACE 65nm rad hard library
10.9 RedCat Devices 0.18 µm and 0.13 µm rad hard libraries

11 Digital Circuits

b)



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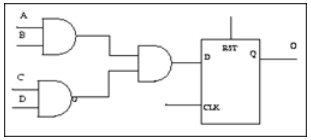
11.3.1 Spatial redundancy

11.3.1.1 Duplex architectures

11.3.1.2 Triple Modular Redundancy architectures

11.3.1.2.1 Basic **TMR**

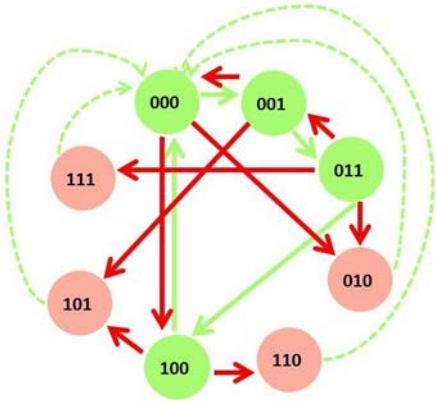
11.3.1.2.2 Full **TMR**



11.3.2 Temporal redundancy

11.3.2.1 Triple Temporal Redundancy combined with spatial redundancy

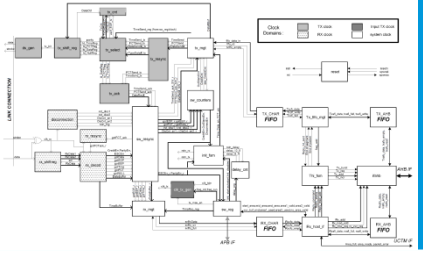
11.3.2.2 Minimal level sensitive latch



11.3.3 Fail-Safe, Deadlock-free Finite State Machines

11.3.4 Selective use of logic cells

12 System on a Chip



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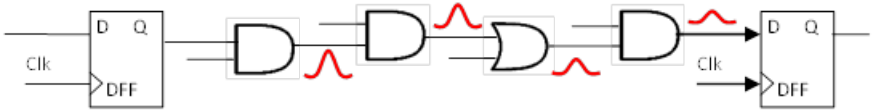
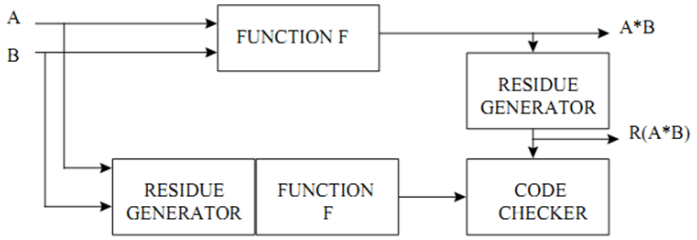
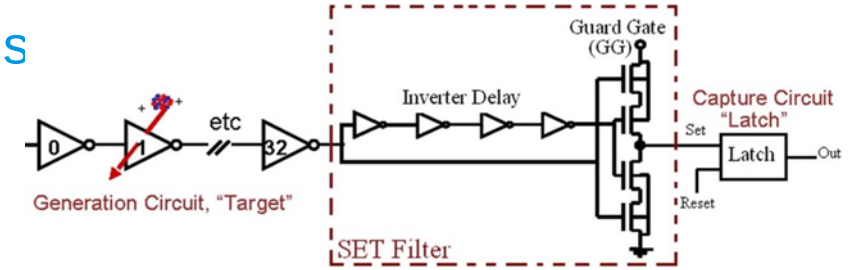
12.3.1 Error Correcting Codes
12.3.1.1 Parity check
12.3.1.2 Cyclic Redundancy Check
12.3.1.3 BCH codes
12.3.1.4 Hamming codes
12.3.1.5 SEC-DED codes
12.3.1.6 Reed-Solomon codes
12.3.1.7 Arithmetic codes
12.3.1.8 Low Density Parity Codes
12.3.2 Mitigation for Memory Blocks
12.3.3 Filtering SET pulses in data paths
12.3.4 Watchdog timers
12.3.5 **TMR** in mixed-signal circuits

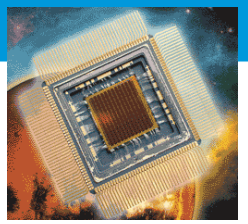




7 bits of data	Number of "1"	8-bits including parity bit	
		even	odd
000 0000	0	**0**000 0000	**1**000 0000
101 0001	3	**1**101 0001	**0**101 0001
110 1001	4	**0**110 1001	**1**110 1001
111 1111	7	**1**111 1111	**0**111 1111

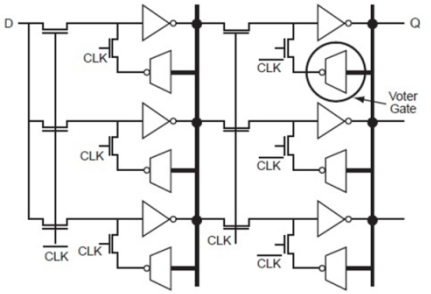


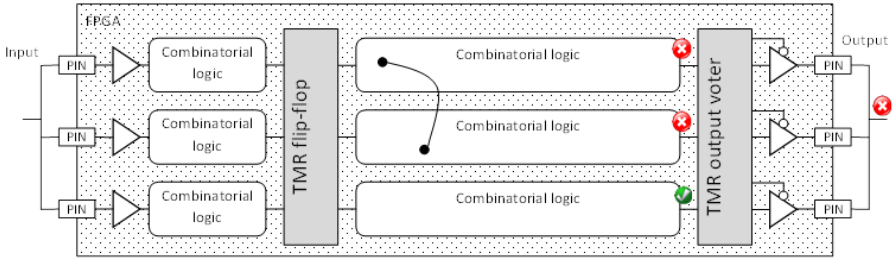
13 Field Programmable Gate Arrays

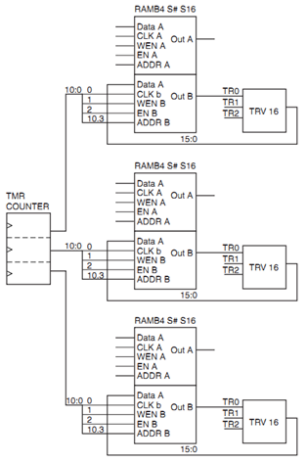


13.3.1 Local **TMR**
13.3.2 Global **TMR**
13.3.3 Large grain **TMR**
13.3.4 Embedded user memory **TMR**
13.3.5 Additional Voters in TMR data-paths to minimise DCE

13.3.6 Reliability-oriented place and Route Algorithm (RoRA)
13.3.7 Embedded processor protection
13.3.8 Scrubbing of configuration memory

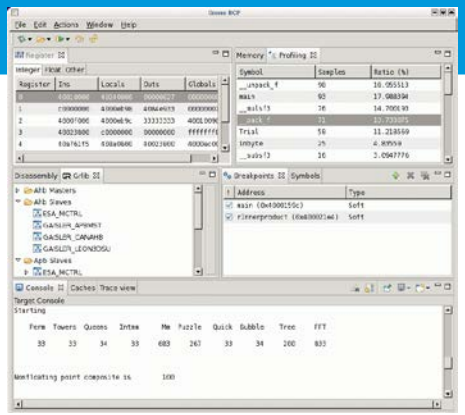




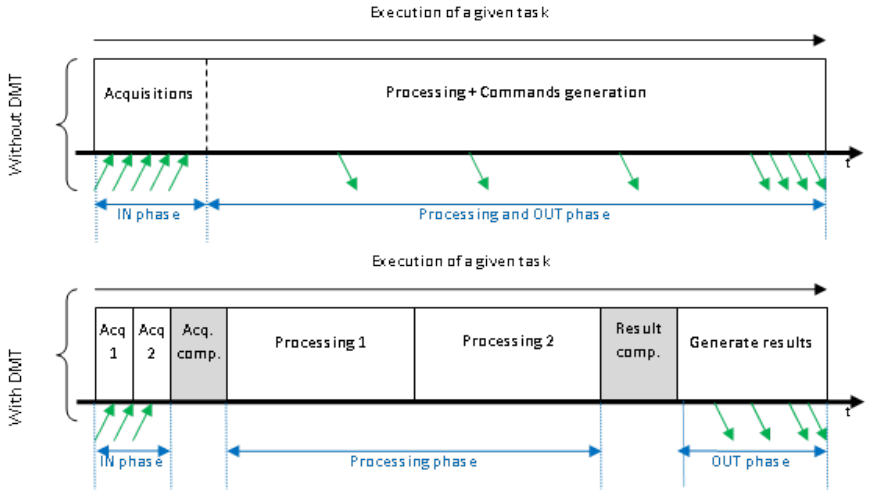


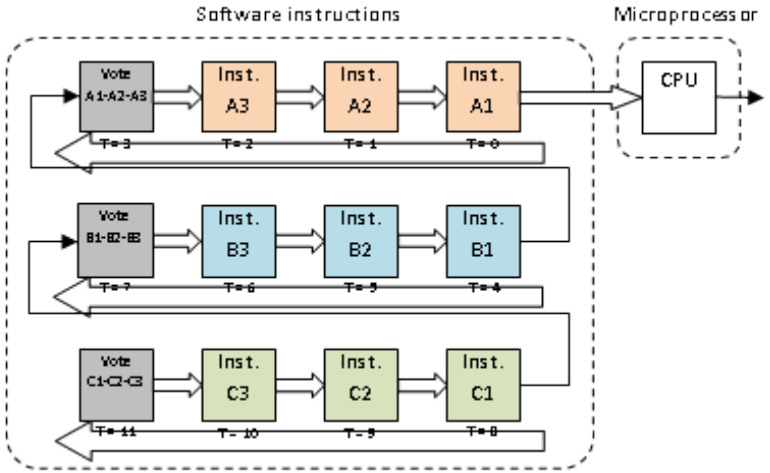
\+ techniques in Chapters 11 (digital) & 12 (SoC)

14 Software-implemented hardware fault tolerance

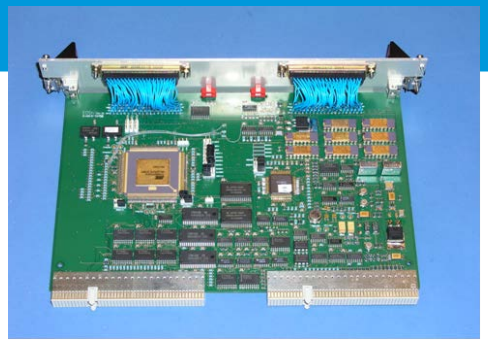


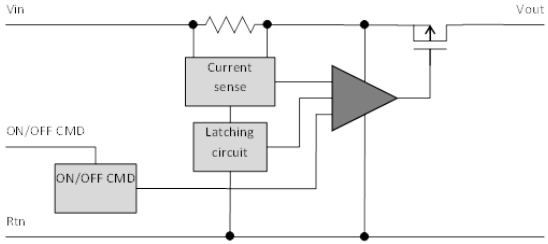
14.3.1 Redundancy at **instruction** level
14.3.2 Redundancy at **task** level
14.3.3 Redundancy at **application** level: using a hypervisor

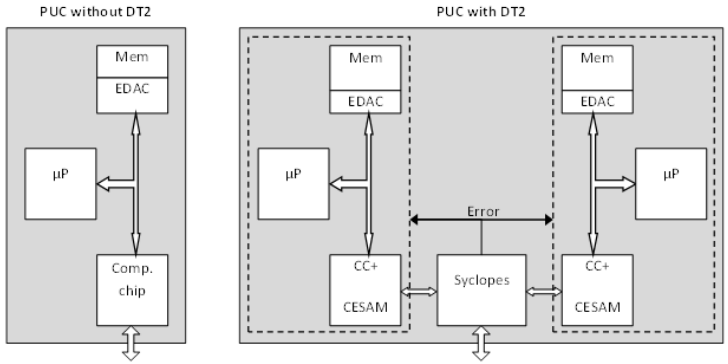


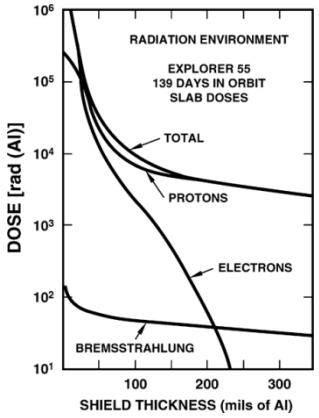


15 System architecture (off-chip)









TMR variants in this Handbook

	11 – Digital Circuits	12 - SoC	13 - FPGA	15 – Off-chip		3x flip flops	3x combinatorial logic	3x voter	Extra voters in data paths	Triplets physical layout separated	3x memory blocks	comparing analog signals	3x chip	Synchronizing logic	3x outputs
Basic TMR	x					x									
Full TMR	x					x	x	x							
Local TMR			x			x									
Global TMR			x			x	x	x							x
Large grain TMR			x			x	x	x		x					x
Embedded memory TMR			x								x				
TMR with **voters against DCE**			x			x	x	x	x						
Mixed-signal TMR		x										x			
Chip-level TMR				x									x	x	

16 Validation methods

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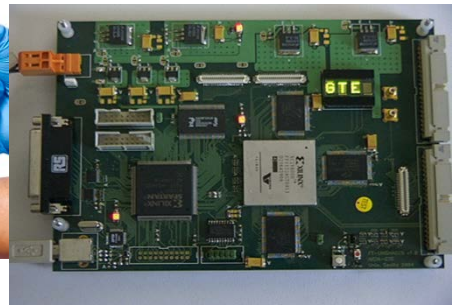
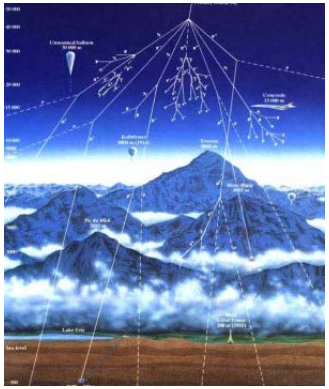


16.2 Fault injection

16.2.1 Fault injection at transistor level
16.2.1.1 Physical level 2D/3D device simulation
16.2.1.2 Transient fault injection simulations at electrical level
16.2.2 Fault injection at gate level
16.2.3 Fault injection at device level
16.2.3.1 Fault injection in processors
16.2.3.2 Fault injection in FPGAs
16.2.3.3 Analytical methods for predicting effects of soft errors on SRAM-based FPGAs
16.2.4 Fault injection at system level



16.3 Real-life radiation tests

16.3.1 Tests on-board scientific satellites
16.3.2 On-board stratospheric balloons
16.3.3 Ground level tests

16.4 Ground accelerated radiation tests

16.4.1 Standards and specifications
16.4.2 SEE test methodology
16.4.2.1 Static test
16.4.2.2 Dynamic test
16.4.3 TID test methodology
16.4.4 TID and SEE test facilities
16.4.4.1 Total ionizing dose
16.4.4.2 Single event effects
16.4.5 Complementary SEE test strategies
16.4.5.1 **Laser beams** SEE tests
16.4.5.2 **Ion-Microbeam** SEE tests
16.4.5.3 **Californium-252 and Americium-241** SEE tests
16.4.6 SEE tests practical constraints and DUT preparation

Future of ECSS-Q-HB-60-02

2015/06: ECSS-Q-HB-60-02 release for ECSS "**public review**" (2 months approx)

==> please check here: http://www.ecss.nl/
to download Handbook during public review
and form to submit **your feedback** !

2015/Q3: ECSS-Q-HB-60-02 **final release** as an official new ECSS Handbook

THANKS!

Questions?
Suggestions?

ECSS-Q-HB-60-02 Handbook
“Techniques for Radiation Effects Mitigation in ASICs and FPGAs”

working group convener & book captain → agustin.fernandez-leon@esa.int