ECSS-Q-HB-60-02A Annex (informative)

Vendor- or institute-ready ASIC and FPGA technology solutions that include mitigation against radiation effects or that can help to introduce mitigation and/or to validate it.

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A.1 Overview

There is a wide offer of ASIC and FPGA technology which either incorporates already one or more mitigation techniques against radiation effects, or that can help the IC user or developer to apply some mitigation. This technology is sometimes available through commercial vendors or sometimes through research groups (universities or institutes).

This Annex lists some of these vendor-ready solutions or tools that are known to the space ASIC and FPGA users/developer community. It is very important to understand that in many cases, the user will have to combine a vendor-ready technology with additional mitigation techniques and/or tools in order to get to the level of radiation hardness that he or she might need.

This reference of existing "vendor-ready solutions" is of course not exhaustive and was written in June 2015. This Annex can be updated in future editions of this handbook, as some of the items become obsolete, and as new ones become available.

A.2 Manufacturing and process level mitigation

Multiple space ASIC and FPGA vendors use silicon wafers with Epitaxial layers, SOI or SOS, or are capable of managing deep N-wells and substrate contacts during the IC manufacturing in order, among other purposes, to also enhance the radiation hardness, for example: Atmel, Cobham (former Aeroflex), Global Foundries, Honeywell, IBM, Microsemi (former Actel), Silanna, SOITEC (provides SOI wafers), STMicroelectronics, TSMC, UMC, XFab or Xilinx.

A.3 Physical Layout Level

Enclosed Layout Transistors are used in several rad-hard cell ASIC libraries. See a list of libraries further down below. Some other tools can help with the modelling of rad effects and how layout modifications can improve the radiation hardness. For example:

- IROC Technologies TFIT and SOCFIT
  http://www.iroctech.com/soft-error-tools/

- Robust Chip Accuro, rExplore and Roplace
  http://www.robustchip.com/

A.4 Circuit Architecture Level (digital and analogue design, ASIC cell libraries, embedded memories)

Several Analogue IP cores (ADC, DAC, filters, amplifiers, etc.) for use in space are being developed in the frame of some ESA projects, and with the intention of being able to reuse them in future analogue or mixed-signal ASIC developments.

- Arquimea (Spain)
  http://www.arquimea.com/?q=products-services/microelectronics/rad-hard-ip-cores

- IC-Sense (Belgium)
  http://www.icsense.com/ic-design/ic-design-IP

All space ASIC vendors provide several analogue IP blocks (PLLs, SerDes, LVDS IOs, etc.) and different types of flip-flops and/or embedded RAM blocks that have been radiation hardened at circuit architecture level (using for example the HIT or DICE cell). What follows is a list of **examples of rad-hard ASIC libraries** available from different vendors or institutes, which, in many cases, also offer **Application Specific Standard Products (ASSP) or off-the-shelf rad hard ICs** (e.g. microprocessors, memories, data/signal processing ICs) which have been designed and manufactured with all the above discussed resources to achieve radiation hardness:

- Atmel ATC18RHA (0,18 μm UMC) and ATMX150RHA (150nm SOI UMC) CMOS radiation hardened libraries
  http://www.atmel.com/products/other/space_rad_hard_ics/rad_hard_asics.aspx

- BAE Systems RH25, RH15, RH45 ASIC libraries, based on IBM processes
  http://www.baesystems.com

- CERN radiation hardened libraries, based on IBM CMOS 250nm and TSMC CMOS 65nm
  https://ph-dep-ese.web.cern.ch/ph-dep-ese/structure/ME.html

- Cobham (former Aeroflex) radiation hardened libraries with multiple foundries (On Semi, MagnaChip, Dongbu, X-Fab, TSMC, IBM): UT90nmHBD, UT130nHBD, UT180nHBD, UT0,25µHDB, UT0,35µHDB, UT0,6µHDB,
  http://ams.aeroflex.com/pagesproduct/asics/prods-asics-space.cfm

- Honeywell rad hard libraries in (0,15µm, 0,35µm and 0,8µm)
  https://aerospace.honeywell.com/en/products/microelectronics

- IHP (in partnership with Arquimea) SiGe BiCMOS SGB25RH (0,25 µm) and SG13RH (0,13 µm)
  http://www.ihp-microelectronics.com/de/loesungen/luft-und-raumfahrt.html

- IMEC Design Against Radiation Effects (DARE) library, based on UMC CMOS 180nm
  http://www2.imec.be/be_en/services-and-solutions/imec-iclink/dare.html

- Orbital ATK 0,35 µm radiation hardened cell library
  http://www.orbitalatk.com/space-systems/space-components/

- Ramon Chips RadSafe CMOS 0,18 µm and 0,13 µm (Tower Jazz) , and 65nm (TSMC) radiation hardened libraries
  http://www.ramon-chips.com/

- RedCat Devices radiation hardened libraries
  http://www.redcatdevices.it/libraries/

- ST Microelectronics C65SPACE CMOS 65nm radiation hardened library
  http://www.st.com/st-web-ui/active/en/catalog/sense_power/FM137/CL1945/SC2002

Some commercial EDA IC Design Tools allow different styles of automatic TMR insertion, or special handling of Finite State Machines during gate-synthesis in order to improve their radiation hardness. For example:

- Mentor Precision Hi-Rel
  http://www.mentor.com/solutions/aerospace/safety-critical-systems-design

- Synopsys Synplify Premier
  http://www.synopsys.com/Tools/Implementation/FPGAImplementation/FPGASynthesis/Pages/HighReliability.aspx

- Xilinx XTMR
  http://www.xilinx.com/ise/optional_prod/tmrtool.htm

A.5 Electronic System Level (FPGA, SoC, SW and Off-chip mitigation)

A few vendors provide FPGA that include multiple mitigation techniques to enhance their radiation hardness, and that have also obtained different space quality certifications. For example:

- Atmel ATF280 , AT40K
  http://www.atmel.com/products/other/space_rad_hard_ics/rad_hard_fpgas.aspx)

- Cobham (formerly Aeroflex) RadTol Eclipse FPGA
  http://ams.aeroflex.com/pagesproduct/prods-hirel-fpga.cfm

- Microsemi (formerly Actel) RTG4, RTAX, RT ProASIC3 and RTSX-SU
  http://www.microsemi.com/products/fpga-soc/rad-tolerant-fpgas

- Xilinx Virtex-5QV, Virtex-4QV
  http://www.xilinx.com/applications/aerospace-and-defense/space.html

Some institutes have developed complementary tools that can evaluate and help to enhance the radiation hardness of some FPGA technologies during the place and route, for example:

- Politecnico di Torino, VERI-Place
  http://www.cad.polito.it/~sterpone/Research_Tools.html

Some vendors offer rad-hard computers or data handling systems (often in one single PCB) which combine the use of rad-hard ICs and commercial-off-the-shelf (COTS) components and use several mitigation techniques at electronic system level. Some examples:

- COTS-based payload computer developed by GDAIS for CALIPSO
  http://www.gd-ais.com/Products/Space-Electronics
  http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20080014189.pdf

- Maxwell SCS750
  http://www.maxwell.com/products/microelectonics/space-sbc

- Patria Power CDH single board computer for Space Applications
  http://patria.fi/en/products-and-services/space/power-cdh

- Surrey Satellite Technology OBC 750 LEO Flight Computer
  http://www.sst-us.com/shop/satellite-subsystems/obdh/obc750-leo-flight-computer

- Space Micro Proton 200K, 300k & 400K computers
  http://www.spacemicro.com/products/digital-systems.html

A.6 Validation methods

There are several tools developed by universities and/or research institutes that are available to help with the validation of inserted mitigation techniques by evaluating the IC response to SEE-like fault injections. For example:

- IASF, FLIPPER
  http://cosy.iasf-milano.inaf.it/flipper_index.htm

- Universidad Antonio Nebrija, SEU Simulation Tool (SST)
  http://www.nebrija.es/~jmaestro/esa/sst.htm

- University of Seville, FT-UNSHADES
  http://woody.us.es/~aguirre/Web_unshades/ftunshades.htm