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Abstract of Document

Project:

In high speed data links e.g. optical, radar or satellite communication systems, medium resolution (4-12 bits) DACs with sampling rates of 0.5-10 GHz are going to be used. Application examples include baseband D/A signal conversion, signal generation in ultra wideband (UWB) communication systems and also direct digital synthesis (DDS). DDS becomes more and more popular in the communication arena due to the simple and well-defined signal control compared to an analog domain phase locked loop (PLL) based signal synthesis.

Next generation telecom satellites will not only provide a spaceborne data relay but will also allow to process data and make use of beam forming techniques to steer the antenna beam to the areas with high need of capacity. In order to achieve this satellite payload must be highly flexible. Therefore, new space qualified components are necessary. One of the key components are high precision and high speed Digital to Analog Converters (DACs) which are critical components in those systems.

The main objective of this project is to develop, build, and test a DAC prototype for the next generation of digital telecommunication payloads.

First step towards this goal is the selection of an adequate process which copes with the main driving design parameters of high performance, low power consumption, high reliability at long operational lifetime and resistance to the harsh radiation environment – all at reasonable costs. Process selection is followed by an architecture study and trade-off, layout of the design and simulations and finally ends in production of first prototypes. After full electrical characterization preliminary radiation tests shall be performed to proof the theoretical radiation considerations.

Document:

This document is the Summary Report of the Broadband Low-Power DAC Design & Prototyping project (project in the following called: DAC). It covers the whole project (phase 1a and phase 1b) and gives an overview of the project organization, structure and main findings, and outcomes.

1 Introduction

In high speed data links e.g. optical, radar or satellite communication systems, medium resolution (4-12 bits) DACs with sampling rates of 0.5-10 GHz are going to be used. Application examples include baseband D/A signal conversion, signal generation in ultra wideband (UWB) communication systems and also direct digital synthesis (DDS). DDS becomes more and more popular in the communication arena due to the simple and well-defined signal control compared to an analog domain phase locked loop (PLL) based signal synthesis.

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The DAC is a high performance, low power 12-bit, 1.5 GSps digital-to-analog converter designed for space application. It is designed to combine high speed with low power consumption. The device in-corporates advanced design techniques to ensure superior performance making it an ideal choice for the synthesis of wideband signals with low inherent noise levels. Advanced operational modes allow for signal synthesis in intermediate frequency levels enabling the realization of lean system concepts without a dedicated baseband-to-I/F converter stage.

The device has four LVDS 12-bit multiplexed input channels, that relax the timing requirement for the board layout as well as for the preceding signal processing stage. The advanced configuration parameters can be set via a Serial-Processor-Interface (SPI). The low speed interface and static mode selection inputs use a standard 3.3 V CMOS technology.

The unit features three fundamental modes of operation:

- **Non-Return-to-Zero (NRZ)** mode: This is the traditional mode of operation. Each sample is converted and the DAC output stays at the corresponding output value until the next sampling instance.
- **Return-to-Zero (RZ)** mode: In this mode the DAC generates output pulses with a pulse width of 50 % of the symbol period, i.e. after half the symbol clock period the output is switched to the zero value. This mode of operation results in a flattened output spectrum compared to the NRZ-mode.
- **Radio-Frequency (RF)** mode: In this mode the DAC output is switched to the inverted input value for the second half of the symbol period. This results in a spectral shift of the output signal to a carrier frequency, which is half the sampling frequency.

The DAC requires the sampling frequency supplied to the clock input of the device. The timing of the data inputs can be adjusted in a flexible way to ease the integration in a given system. These adjustments are performed via the SPI interface of the unit.

The DAC is fabricated in a 0.25 µm SiGe-BICMOS technology, which is robust against radiation effects. Susceptible CMOS parts of the system are radiation hardened by redundancy techniques.

2 Project Organization

2.1 Team

The DAC project was performed by a team led by Kayser-Threde (KT) with the subcontractors advICo microelectronics GmbH Germany, Innovations for High Performance microelectronics (IHP GmbH) Germany, MASER Engineering B.V Netherlands, and RUAG Space, Sweden. Later in the project the possible customers EADS Astrium Ltd., UK and Thales Alenia Space, France joint the team as consultants.

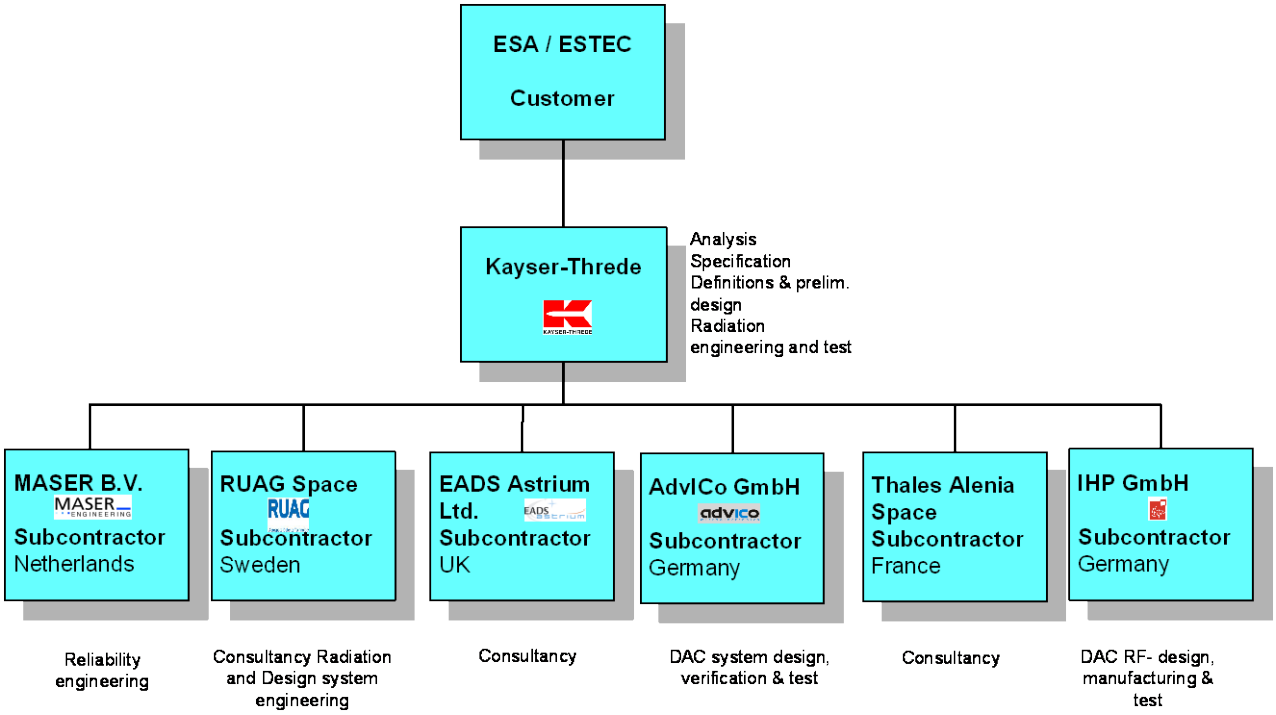

Figure 2-1 Team structure

3 Architecture

3.1 General description

The DAC is a high performance, low power 12-bit, 1.5 GSps digital-to-analog converter designed for space application. It is designed to combine high speed with low power consumption. The device incorporates advanced design techniques to ensure superior performance making it an ideal choice for the synthesis of wideband signals with low inherent noise levels. Advanced operational modes allow for signal synthesis in intermediate frequency levels enabling the realization of lean system concepts without a dedicated baseband-to-I/F converter stage.

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The DAC is fabricated in a 0.25 µm SiGe-BICMOS technology, which is robust against radiation effects. Susceptible CMOS parts of the system are radiation hardened by redundancy techniques.

3.2 Requirements (ESA requirements)

- High speed, high precision: 12 Bit, 1.5 GSps
- Range of allowable sampling rates: 0.1 … 1.5 GSps
- Excellent dynamic performance
  - ≥ 60 dB SFDR
  - ≥ 50 dB NPR
  - < ±0.5 dB (peak-peak) gain flatness
  - 11 bit typical ENOB
  - 750 MHz analog DAC bandwidth
- High static precision
  - ≤ 0.5 LSB INL (integral non-linearity)

  - ≤ 0.25 LSB DNL (differential non-linearity), (min.) 0.5 typical
- Extremely low power consumption (goal) : ~ 600 mW typical [at 1:1 mux. mode at output voltage]
- [600 mVpp], currently 870 mW simulated, subject to change
  - 2.5 V supply for digital core
  - 3.5 V supplies for digital I/O and DAC analog circuitry
- LVDS inputs for high speed data and DataReady clock
- Differential low noise clock input
- CMOS I/O for low speed configuration signals
- Compact 255 pin CiCGA package (use of the same package as the ADC).

3.3 DAC concept with calibration

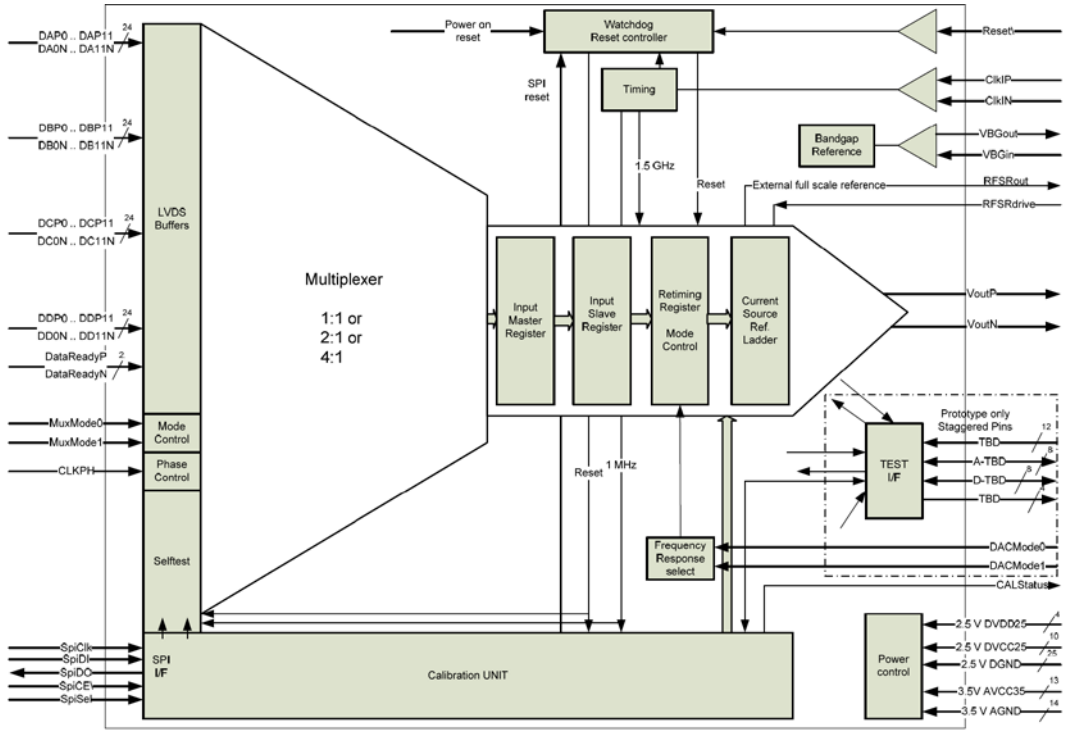

Figure 3-1 Functional block diagram of the 12 Bit 1.5GSps DAC

The realized broadband low power DAC consists of the current steering concept to achieve the required speed by getting the most possible parallelism.

The current steering comes in different variants. Those are namely: binary weighted, unary weighted, and segmented architecture. The **unary weighted** architecture has the best performance in terms of **static and dynamic accuracy**. But it has highest area overhead as well as complex decoding circuitry. A compromise in terms of accuracy and the complexity can be found in **segmented current steering architecture**. In this kind of architecture the DAC is divided into two or more sub-DACs. In the commonly used segmented architecture the DAC with N-bit resolution is divided into two parts: a given number of LSBs (M) are converted into analog signal by the LSB DAC and the rest of the input bits (N-M) are converted by the MSB DAC. The LSB DAC is implemented with the binary weighted DAC and the MSB DAC is implemented with the unary weighted architecture.

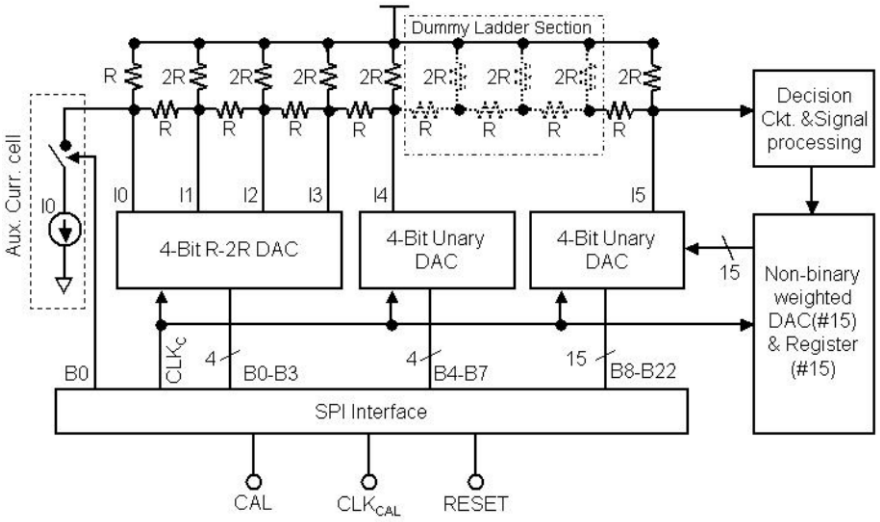

Figure 3-2 Implemented 12-bit architecture (B_0-B_3 = LSBs), (B_4-B_{11} = MSBs)

Figure 3-2 represents a simplified block diagram of the high-speed 12-bit DAC. The main architecture is based on the **segmented current steering** DAC. In this particular application the 12-bit DAC is divided into three 4-bit sub-DACs.

- 4-bit R-2R DAC (B0-B3)
- 4-bit unary weighted DAC (twice)
- Global R-2R load resistor network
- Central clock generation circuit.

Four LSBs (B_0-B_3) are connected with the R-2R DAC. The rest of the 8 bits (B_4-B_{11}) are converted to corresponding analog signals by means of two identical 4-bit unary weighted DACs. These two unary weighted DACs have the same unit currents (I_{LSB}) and the weighting function is accomplished with the R-2R ladder network. A central clock is used to control the current switching timing of all three DACs.

3.3.1 Calibration

With the above described DAC architecture and the selected IHP technology only an accuracy of 8 to 9 bits can be achieved.

The R-2R ladder network, which is shown in Figure 3-2 can be implemented with an accuracy, which corresponds to 10-bit of matching accuracy The area of the 2R unit resistor must be chosen corresponding to the mismatch coefficient given in the SGB25VD process specs. The matching accuracy can be enhanced with larger resistors at the cost of conversion rate. Assuming that the current cells have 8.5-bit of matching accuracy and the R-2R ladder has 10-bit of accuracy it can be said that the 12-bit DAC would provide an 8-bit of static accuracy at the output. Thus a calibration technique can be employed at the MSB DAC current cells to enhance the static accuracy to 12 bits.

The simplified block diagram of the calibration block along with the core 12-bit is presented in Figure 3-2. The full calibration process is controlled by an SPI bus interface. This SPI interface accepts three input signals; the asynchronous RESET signal, the input clock, which is essentially a CMOS, signal with a signal swing of 0-2.5 V. The third one is as mentioned earlier the data signal for the calibration (CAL).

The SPI interface generates a 23-bit code word (D0-D22), which is used as the input bit pattern of the DAC in calibration mode. Eight LSBs (D0-D7) of this code word are directly connected with the 8-LSBs (B0-B7) of the core 12-bit DAC. The rest of the bits (D8-D22) are connected with the fifteen retiming DFFs of the MSB DAC. An auxiliary current cell is used in parallel with the LSB current cell. It is also controlled by the SPI interface signal D0. The output of this auxiliary current cell is connected to the I0 port of the R-2R ladder.

The calibration technique implemented consists of the following functions:

- Power up calibration
- and background calibration.

Power up calibration

After power up with the reset signal of the DAC, the current sources are adjusted to a golden current source and the calibration values are stored in non-volatile memory (SEU protected). This eliminates the initial deviations in the DAC circuit to achieve 12 bits.

Background calibration

However, each DAC will drift according to temperature, aging, and radiation. This is a relatively slow drift and can be compensated with a background calibration with low duty cycles (some minutes)

The main calibration process can be considered as the calibration of all fifteen current cells of the MSB DAC current cells taking the LSB and the intermediate DAC output as the reference.

A supplementary non-binary weighted current steering DAC is used as a variable current source, which is used to reduce the error current IERR during calibration. The advantage of using non-binary weighted current steering DAC for calibration is very low area and power consumption. This non-binary weighted DAC can provide the same accuracy even in presence of higher process mismatch at the cost of additional redundant inputs. In this present application the non-binary DAC is implemented with the radix 1.8. The simplified block diagram of this DAC is presented in Figure 3-3.

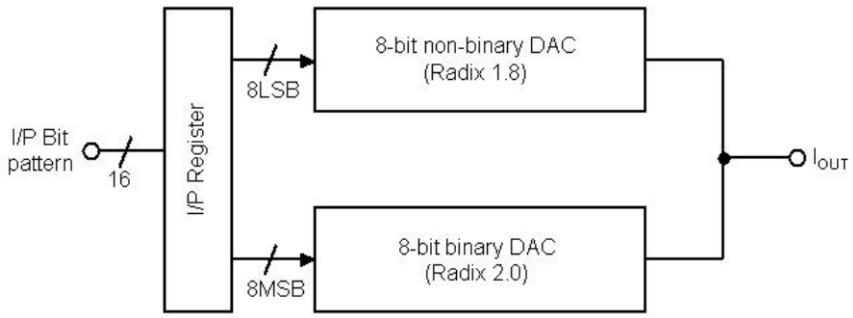

Figure 3-3 Block diagram of 16-bit non-binary weighted DAC

This non-binary weighted DAC has a 16-bit input. It is divided into two sub-DACs; a non-binary weighted 8-bit DAC and a binary weighted 8-bit DAC. Both of the sub-DACs are having architecture similar to the conventional binary weighted DAC. Thus the input bit pattern can directly control the current switching.

In Figure 3-4 the block diagram of an 8-bit non-binary weighted DAC is presented. It is implemented with the radix 1.8. The weighted current sources are implemented with a modified resistive ladder. This resistive ladder has the same architecture like R-2R ladder. But to implement the weighting factor of 1.8 among the current cells the 2R resistance is replaced with a resistance value of 1.8R. The current switches are implemented with conventional CMOS differential pairs. At the output of the DAC

one of the differential paths is dumped by a resistor and the other path is used as the single ended output (IOUT).

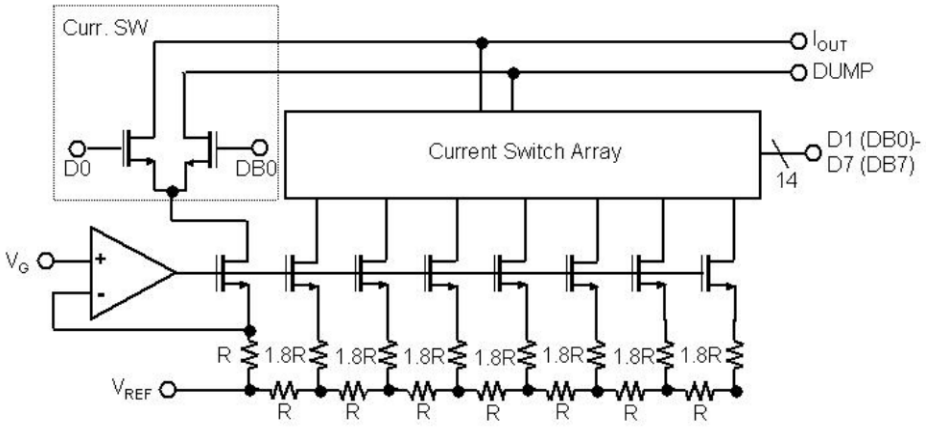

Figure 3-4 Block diagram of 8-bit non-binary weighted DAC

The 8-bit binary weighted sub-DAC has been implemented in the same fashion of the non-binary weighted sub-DAC. As this sub-DAC is a purely binary weighted so an R-2R ladder network is used unlike R-1.8R ladder network.

The 8 LSBs of the input bit pattern are connected with non-binary sub-DAC and rest of the input bits are connected with the binary sub-DAC. Single-ended outputs of these two sub-DACs are combined together to achieve the desired output.

This 16-bit calibration DAC provides about 14-bit resolution, which is by far enough to calibrate the 12-bit main DAC up to the required level of static accuracy. While this calibration maintains the DC parameters of the DAC during all operating conditions, the AC parameters do not need to be calibrated.

The AC performance of the DAC will be determined by the precision (on-off current ratio, switching symmetry and switching transients) of the high-speed current cells in the Sub-DAC blocks.

The major element for introducing a 12-bit low power high-speed DAC with calibration is the availability of a micro-DAC in IHP BiCMOS technology to adjust the process dependent parameters such as device mismatch, long-term stability or temperature drift. This self-calibration function added to the DAC analog high-speed circuits relax greatly the dependence on tight process tolerances, allowing to use leading edge technology for the high-speed part (RF-part) of the DAC. This self-adjustment has simplified the scaling of the DAC analog circuit.

The micro-DAC used in the DAC design is not a conventional true DAC as one usually would think to be used for highly accurate calibration, imposing strong requirements either on the process parameters or on the chip area or on the power consumption. This would make calibration of single analog circuits more expansive both in power and area. This problem becomes more important if multiple circuits per chip are to be connected since the DACs have to be operated continuously and can hardly be shared.

In fact, a true DAc is not required to convert the digital value to analog. Even an overall monotonicity is not necessary. The counter based correction loop already has the intrinsic ability to cope with large weighting errors, as long as all the steps larger than one LSB are pointing to the negative direction of the transfer curve. If a DAC can be replaced by a simple small weighting circuit, digital adjustment at high accuracy is possible on small area and at very low power consumption. This would allow a much wider application range of self-calibration, including simple RF circuits, e.g. amplifiers and mixers.

Sufficiently small positive steps demand the effective weighting radix $r_{eff} = r\ (1+e_r)$ of each weighting element to be less than two in any case. Here, e_r is the relative error of the weight r of a weighting element. If e_{max} is an upper limit to e_r, then it is sufficient to design the weighting radix r of an element as

$$r = 2/(1+e_{max})$$

With a value of r significantly below two, large relative errors are tolerated, allowing simple circuits and small devices. Together with the binary input, this non-binary radix generates intentional negative steps in the transfer curve. On the other hand, it limits the positive steps to an LSB value of the weighting block. The bit width of the counter determines the resolution of the adjustment. Such a weighting block with an asymmetric dynamic non-linearity (DNL) is not a true DAC anymore, because it has a non-linearity characteristic with large negative steps, even in the ideal case. In a DAC, DNL is usually caused by errors rather than imposed by design.

Due to the smaller radix, the non-linear weighting block needs a slightly wider counter than a DAC. Thereby, the calibration speed is reduced. Digital adjustment is mainly aimed at calibrating at large time intervals, e.g. to cope with process variations or to track temperature changes.

The big advantage of the non-binary weighting compared to a binary DAC is the greatly improved tolerance to device mismatch in the weighting element. The radix of 1.6 guarantees that positive steps in the weighting transfer curve are definitely smaller than 1 LSB as long as the device error is less than 25 %. On the other hand, it causes substantial non-linearity of the offset correction circuit by introducing large negative steps into the transfer curve.

Figure 3-5 compares the ideal transfer curves of a DAC and of a weighting block with a radix of 1.6 for each weighting element.

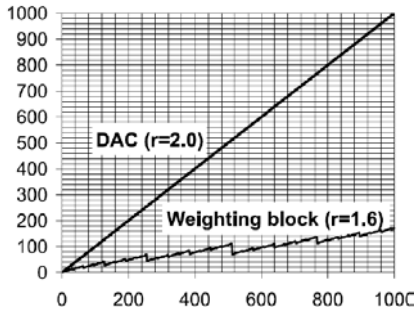

Figure 3-5 Ideal transfer curves of a DAC and of a non-linear weighting block with r=1.6

Together with the counter in the loop, the negative steps do not affect the correction accuracy. The counter will continue counting up until the desired correction value is reached. Negative steps will only increase the counting time, but do not prevent to achieve the desired value with an accuracy of better than 1 LSB.

3.4 Detailed design

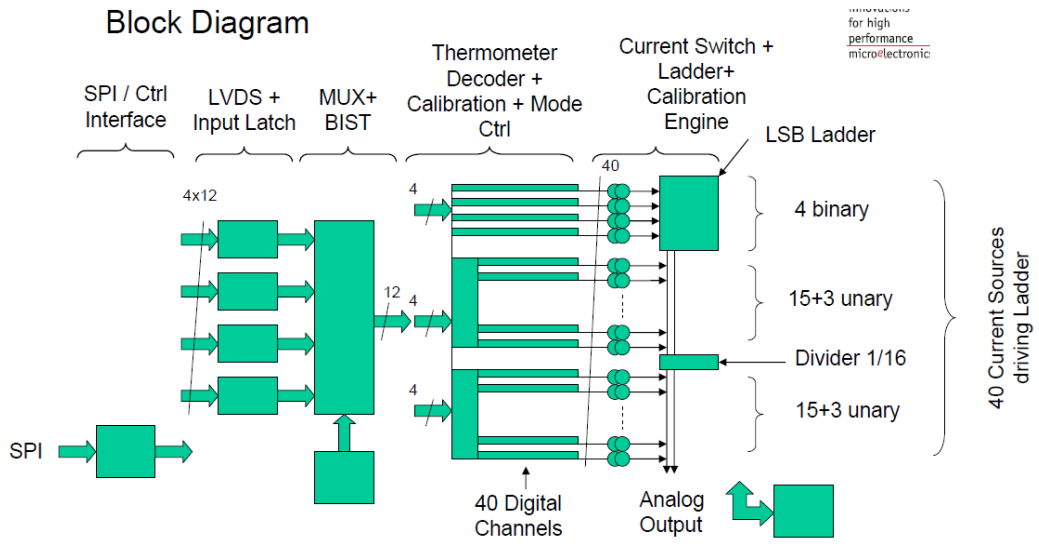

Figure 3-6 Detailed block diagram of the DAC architecture

The DAC consists (from left to right in Figure 3-6) of the following functions:

- SPI interface
- LVDS level converter and input latch
- Multiplexer (Mux) and Built-in Self-test (BIST)
- Thermometer decoder and calibration + mode control (40 digital channels)
- Current switches + resistor ladder + calibration engine
- Analog output circuit.

3.5 Top level design / layout and package

3.5.1 Top level design and layout

The final layout of the first prototype design counts 386,380 devices, including approximately 250,000 MOS transistors, filling up a space of 5 mm x 5 mm.

The whole design was split into several sub-blocks to make parallel design and verification feasible.

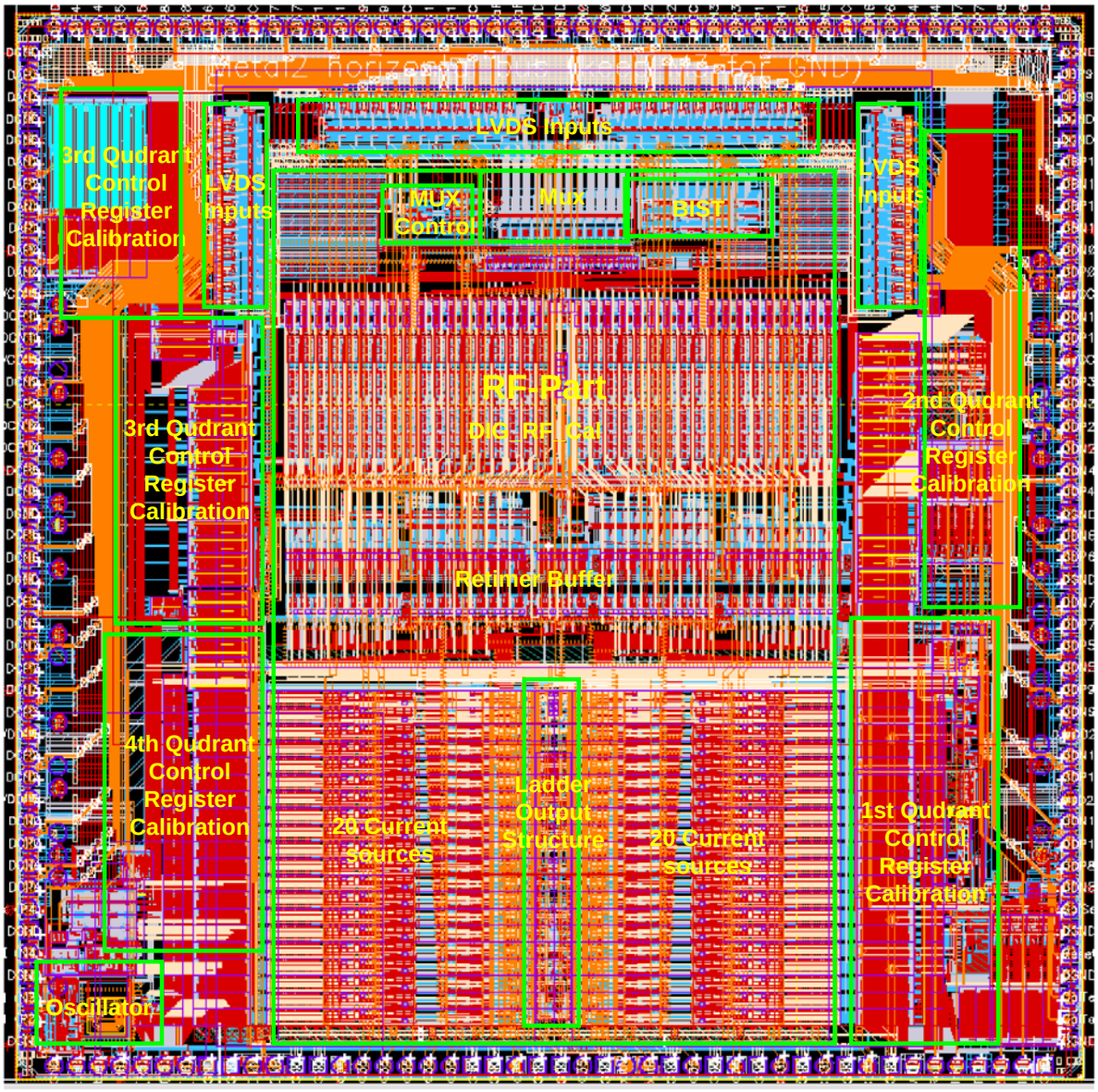

Figure 3-7 Final full chip layout (filler structures not shown)

On the full chip fill patterns have been created for Activ and all metal layers (1.8 million shapes). Wide metal, where not fixed manually, has been cheesed by a script which creates only minimal openings to fulfill the max. density rules.

3.5.2 Package

The baseline for the package of the DAC is the common package approach of a 255 CICGA together with the ADC. The following definition supports this approach.

3.5.2.1 Signal description and pin list

For the DAC the following pin allocation has been defined:

- the operational standard pin allocation (Table 3-1)
- and the test pin allocation for putting the DAC into operation (Table 3-2)

The following table demonstrates the operational standard pin allocation.

Table 3-1 Signal description and pin list - [Req.# DAC-0420]

Pin	Name	Function
A6, C7, B3, B4, B5, C2, C5, D2, B7, E1, F3, F2	DAP(0:11)	Data Input A, LVDS positive signal, used in 1:1, 2:1, 4:1 Mux input mode
A3, A4, A5, A7, B6, C1, C6, C8, D1, E2, E3, F1	DAN(0:11)	Negative side of Data Input A
A10, A12, B9, B11, B13, B14, C9, C11, C15, D15, E14, E15	DBP(0:11)	Data Input B, LVDS positive signal, used in 2:1, 4:1 Mux input mode
A9, A11, A13, A14, B10, B12, C10, C12, C16, D16, E16, F14	DBN(0:11)	Negative side of Data Input B
G1, H2, H3, J1, K2, K3, L1, M2, M3, N1, P2, P3	DCP(0:11)	Data Input C, LVDS positive signal, used in 4:1 Mux input mode
G2, G3, H1, J2, J3, K1, L2, L3, M1, N2, N3, P1	DCN(0:11)	Negative side of Data Input C
F16, G14, G15, H16, J14, J15, K16, L14, L15, M16, N15, P15	DDP(0:11)	Data Input D, LVDS positive signal, used in 4:1 Mux input mode
F15, G16, H14, H15, J16, L16, K14, K15, M14, M15, N16, P16	DDN(0:11)	Negative side of Data Input D
ClkIP	T6	High Speed Clock Input at sampling

Pin	Name	Function
ClkIN	R6	frequency, LVDS signal pair
DataReadyP, DataReadyN	A8 B8	Part of DAC Data I/F, Data strobe
VoutP VoutN	T10 T9	Differential voltage output pair
VBGout	R13	Internal Bandgap voltage
VBGin	M12	Bandgap input (connect to VBGout)
AGNDreturn	T13	Reference ground for external bandgap
RFSRout	T12	Internal reference resistor
RFSRdrive	R12	Internal reference current output (connect to RFSRout)
AVCC35return	M11	Reference VDD for external reference resistor (connect between AVDD35return and RFSRdrive)
ClkPH	P14	Dataready clock phase control
SpiClk	P4	SPI data clock
SpiDI	N4	SPI serial data in
SpiDO	M6	SPI serial data out
SpiCEN	N6	SPI chip enable, low-active
SelctTestMode	N14	
MuxMode0 MuxMode1	R5 T5	Interface option bits (1:1,2:1,4:1)
Clksourceselect	R4	*SelectTestMode=0* CalTest1=BIST_T CalTest0=ComparatorSelectMux (error amplifier monitor *SelectTestMode=1* CalTest1=MedianOverflow CalTest0=ScrubbingClock
ClkExternal	T4	

Pin	Name	Function
DGND	A16, B1, B16, C4, C13, R1, T1, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R2, R3, R15, R16, T2, T3, T15, T16	Common Digital Ground of DAC
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11	Common Analog Ground of DAC
DVCC25	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	ECL 2.5 V supply
DVDD25a	J6, K4, K5, K6	CMOS 2.5 V supply (core+I/O), left plane
DVDD25b	J11, K11, K12, K13	CMOS 2.5 V, right plane
AVCC35	L7, L8, L9, L10, M8, M10, N8, N10	Analog 3.5 V DAC supply

The following test pads are necessary for the RF-DAC Block. They are to be placed in 2nd row (behind C, D channels) and bonded as an option for test only. Chip is intended to work without connecting those pads.

Table 3-2 Test pads for bias adjust of various blocks

Pad #	Name	Type	Description	Comment
	BIST_T	CMOS 2.5V logic output*	366kHz test output, MSB of BIST counter	To be used for radiation tests
G1	TP1_MUX	Analog input	Is able to shift bias voltage by some amount, use external resistor to external voltage source, no ESD!	Mux bias control
F1	TP2_MUX	Analog input		
J2	TP1_DR	Analog input		Digital RF bias control

Pad #	Name	Type	Description	Comment
K2	TP2_DR	Analog input		
F16	TP1_Th	Analog input		Thermometer decoder bias control
G16	TP2_Th	Analog input		
H1	TP1_RT	Analog input		Retiming FF bias control
H3	TP2_RT	Analog Input		
J14	TP1_BUF	Analog input		Buffer bias control
L16	TP2_BUF	Analog Input		
L2	TP1_BIAS_CS	Analog input		CS bias control
M2	TP2_BIAS_CS	Analog input		
K1	TP1_ECTC	Analog input		ECTC bias control
N2	TP2_ECTC	Analog input		
P1, P2, P3	R1, BC1, DGND1	R1-BC1 rppd 50Ohm w=25u	BC1-DGND1 npnVs AE=2x8x0.42x0.84u, BC-short (temperature diode) DGND1 internally connected to DGND, emitter of diode (lower left)	No ESD protection
K14, J14, L15	R2, BC2, DGND2	R2-BC2 rppd2 50Ohm w=25u	BC2-DGND2 npnVs AE=2x8x0.42x0.84u, BC-short (temperature diode). DGND2 internally connected to DGND, emitter of diode (upper right)	No ESD protection
L14	TestPad_ComparatorSelectMUX	CMOS input, internal 200kOhm pull-down	Can be used to override error amplifier signal	

*) CMOS output buffer to be placed.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		DVCC25	DAN5	DAN6	DAN7	DAP9	DAN10	Data ReadyP	DBN0	DBP2	DBN3	DBP5	DBN6	DBN7	DVCC25	DGND
B	DGND	DVCC25	DAP5	DAP6	DAP7	DAN9	DAP10	Data ReadyN	DBP0	DBN2	DPB3	DBN5	DBP6	DBP7	DVCC25	DGND
C	DAN4	DAP4	DVCC25	DGND	DAP8	DAN8	DAP11	DAN11	DBP1	DBN1	DBP4	DBN4	DGND	DVCC25	DBP8	DBN8
D			DGND	DVCC25	DVCC25	DGND	DGND	DGND	DGND	DGND	DGND	DVCC25	DVCC25	DGND	DBP9	DBN9
E				DGND	DGND	DGND	DVCC25	DVCC25	DVCC25	DVCC25	DGND	DGND	DGND	DBP11	DBP10	DBN10
F	TP2_MUX			DGND	DVCC25	DGND	DGND	DVCC25	DVCC25	DGND	DGND	DVCC25	DGND	DBN11		TP1_Th
G	TP1_MUX			DGND	DVCC25	DVCC25	AGND	AGND	AGND	AGND	DVCC25	DVCC25	DGND	BC2		TP2_Th
H	TP1_RT		TP2_RT	DGND	DGND	DVCC25	AGND	AGND	AGND	AGND	DVCC25	DGND	DGND	R2	DGND_2	
J		TP1_DR		DGND	DGND	VDD25a	AGND	AGND	AGND	AGND	VDD25b	DGND	DGND	TP1_Buf		TP_MID_CLK
K	TP1_ECTC	TP2_DR		VDD25a	VDD25a	VDD25a	AGND	AGND	AGND	AGND	VDD25b	VDD25b	VDD25b		TP_LSB_CLK	
L		TP1_Bias_CS	DGND1	DGND	DGND	DGND	AVCC35	AVCC35	AVCC35	AVCC35	DGND	DGND	DGND	TestPad_Comparator SelectMUX		TP2_Buf
M		TP2_Bias_CS		DGND	DGND	SpiDO	AGND	AVCC35	AGND	AVCC35	AVCC35 return	VBGin	DGND			
N		TP2_ECTC		SpiDI	DGND	SpiCE\	AGND	AVCC35	AGND	AVCC35	DGND	DGND	DGND	SelectTest Mode		
P	R1	BC1		SpiClk	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	ClkPH		
R	DGND	DGND	DGND	CLKSourceSelect	Mux Mode0	ClkP, ClkN	AGND	AGND	AGND	AGND	AGND	RFSR drive	VBGout	CalTest1	DGND	DGND
T	DGND	DGND	DGND	ClkExternal	Mux Mode1		AGND	AGND	VoutN, VoutP		AGND	RFSR out	AGND return	CalTest0	DGND	DGND

Figure 3-8 Pin allocation for DAC prototypes

3.5.2.2 Mechanical package information

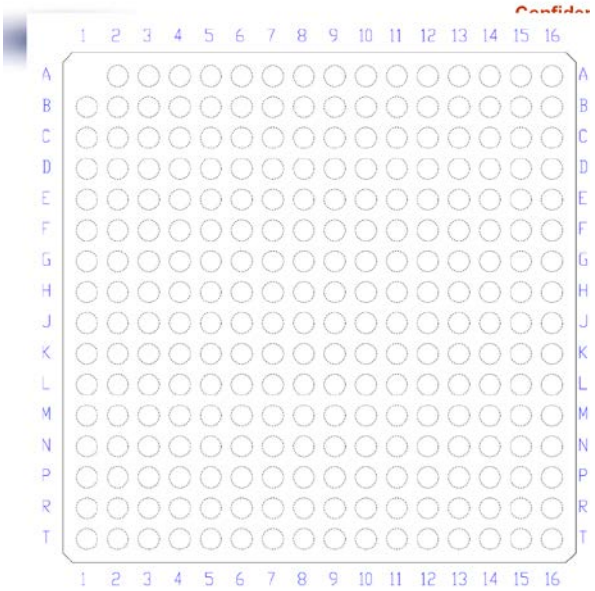

Figure 3-9 Ci-CGA 255 bottom pattern

4 Test of prototype

4.1 Prototype 2

4.1.1 Test set-up of prototype 2

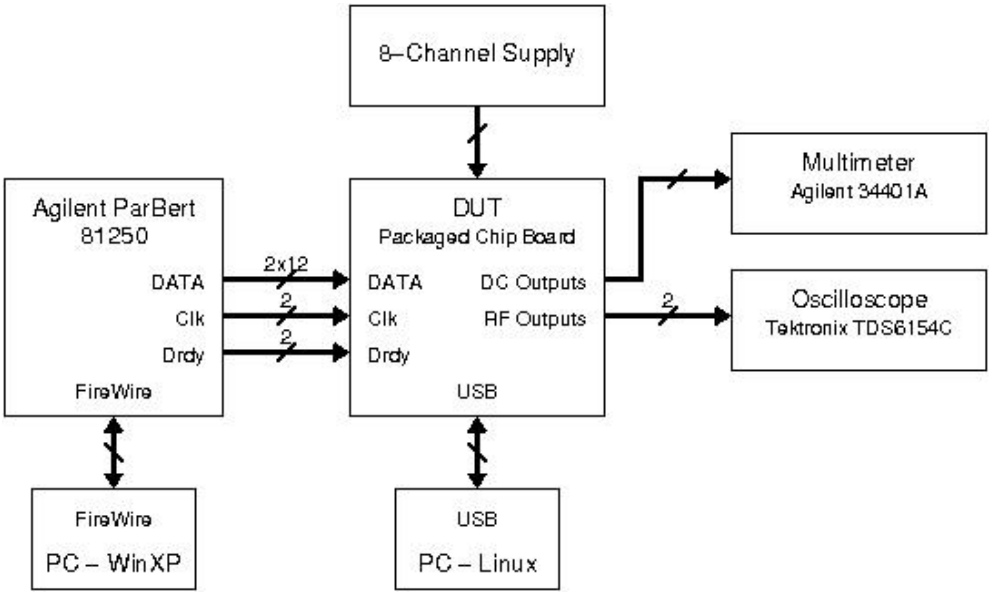

Figure 4-1 General test set up for dynamic and static testing of the high speed part by using the packaged chip board

The following figures show pictures of the test set-up.

Figure 4-2 Test set-up with a packaged chip test board

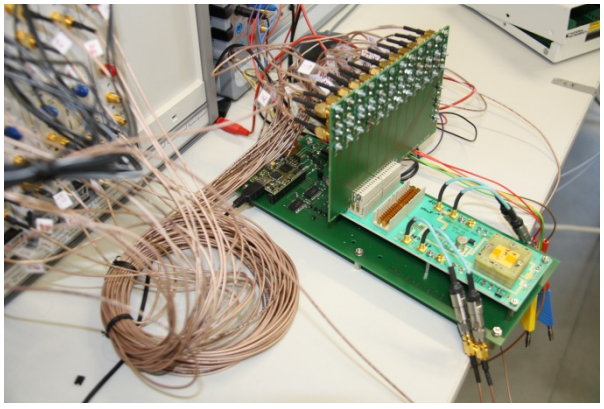

Figure 4-3 A packaged chip test board

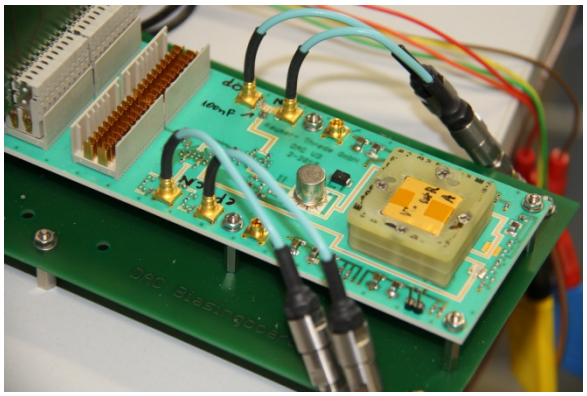

Figure 4-4 A DUT area of the test board

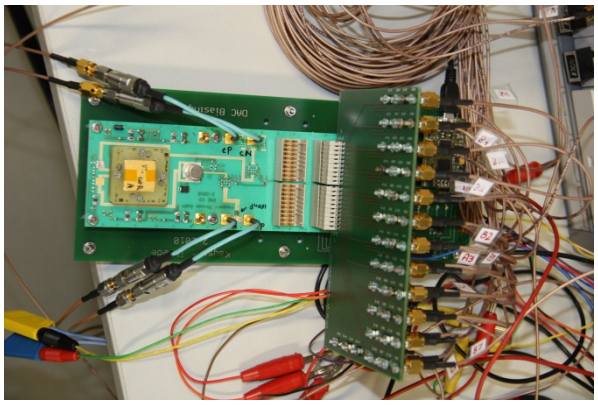

Figure 4-5 Packaged chip board – top view

4.1.2 DAC prototype 2 – tests at IHP and KT – performed measurements

Table 4-1 List of performed measurements with the un-calibrated DAC IHP

Spec. No. [3]	Spec. Item	Conditions	Required value
	Supply voltage and current		
DAC-0065	digital power supply VDD25	min.	2.4V
DAC-0070	analog power supply AVCC35	min.	3.3V
DAC-0075	interface power supply DVCC25	min.	2.4V
DAC-0077	A-GND	typ.	0V
DAC-0080	supply current @ AVCC35	4:1 MUX, max	118mA
DAC-0085	supply current @ AVCC35	2:1 MUX, max	118mA
DAC-0090	supply current @ AVCC35	1:1 MUX, max	118mA
DAC-0095	supply current @ DVCC25	4:1 MUX, max.	264mA
DAC-0100	supply current @ DVCC25	2:1 MUX, max	244mA
DAC-0105	supply current @ DVCC25	1:1 MUX, max	234mA
DAC-0106	add on supply RZ mode	typ, for RZ mode	23mA
	Static DAC Performance		
DAC-0110	Static resolution		12Bit
DAC-0115	INL Golden source calibration Binary source calibration	max. - INL for uncalibrated and calibrated binary source	±1.5LSB - ± 1.5LSB
DAC-0120	DNL	max.	±1.0LSB
DAC-0125	DAC full scale output DAC gain	max. 100 Ω differential load	0.8Vpp ± 0.8Vpp
DAC-0130	output impedance		100Ohm±10%
	Dynamic DAC Performance		
DAC-0145	sampling rate	max.	1.5 GHz
DAC-0150	SFDR	min.	60dBc
	Bandgap reference		
DAC-180	voltage	typ.	1.18V
	CLK input		
DAC-210	amplitude	min.	800mV

Spec. No. [3]	Spec. Item	Conditions	Required value
DAC-215	common mode	min., max.	1V, 1.5V
DAC-220	clk frequency	max.	1.5 GHz
DAC-230	input resistance		50Ohm±10%
	LVDS input specification		
DAC-240	input voltage difference	min, max.	0.2Vpp, 0.45Vpp
DAC-245	common mode voltage	min, max.	1.0V, 1.32V
DAC-246	input voltage range	min, max.	775mV, 1545mV
DAC-247	common mode frequency	max.	1 GHz
DAC-250	input impedance	max.	100Ohm±10%
DAC-253	data rate	MUX1:1	1500Mb/s
DAC-261	skew	max.	150ps
	DAC Timing specification		
DAC-365	dataready to clk edge hold time	max.	-150ps
DAC-366	dataready to clk edge set-up time	min.	-520ps
DAC-367	total data ready window	typ.	370ps
DAC-370	dataready to data set up time	max.	30ps
DAC-371	dataready to data hold time	max.	170ps
DAC-372	Data window	max.	200ps

In the following some of the major tests are shown. The detailed information is available in DAC-RP-KT-014, Issue 1. The summary of the test results of prototype 2 is listed at the end of this chapter in Table 4-4.

4.1.2.1 DAC full scale output DAC-0125

- Measurement description

1. DUT is initialized and switched to the MUX 1:1 mode by the external pins.
2. Input clock frequency is set to 1.5 GHz with duty cycle of 50 %.
3. The frequency of DataReady signal is set to ½ of the input clock (750 MHz with the duty cycle of 50%).

- Results

The full scale output of the DAC is measured at different values of the gain. The gain register is working as expected as is seen in the figures. The maximum output peak-to-peak voltage is 0.935 V for the gain of 0x00 and the minimum value is 0.507 V for the gain of 0xFF at room temperature.

Table 4-2 DAC output full scale voltage at various gain values

Gain	Vout Diff [V]	Vout pp [V]
0x00	**1.871**	**0.9355**
0x80	**1.462**	**0.731**
0xFF	**1.014**	**0.507**

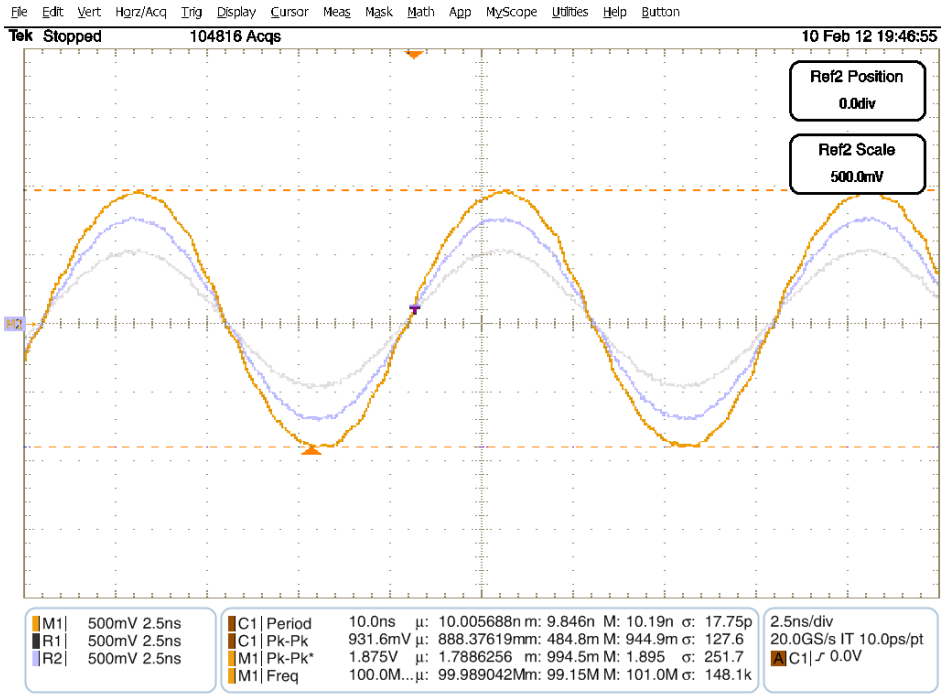

Figure 4-6 DAC output differential voltage at three gain values of 0x00, 0x80, and 0xFF

4.1.2.2 DAC gain DAC-0125

- Measurement Description

1. DUT is initialized and switched to static E Mode.
2. Input clock frequency is set to 100 MHz.
3. The Data Ready signal is set to 50 MHz with 50% duty cycle.
4. Supply voltages: AVCC35=3.5V, DVCC25=2.5V, VDD25=2.5V.
5. The gain of the DAC is set by programming the 8-bit GDAC register.
6. The DAC output ramp is sampled every 50 LSB by the DAQ card and the results are stored in a text file.
7. A matlab script is used to calculate the DAC gain by a first order leas-square-fit (LSF) off each DAC output ramp.
8. The measurements are repeated for different gain settings from 0x00 to 0xFA in 10 LSB steps.

- Results

The gain register is working as expected as can be seen in the following figure.

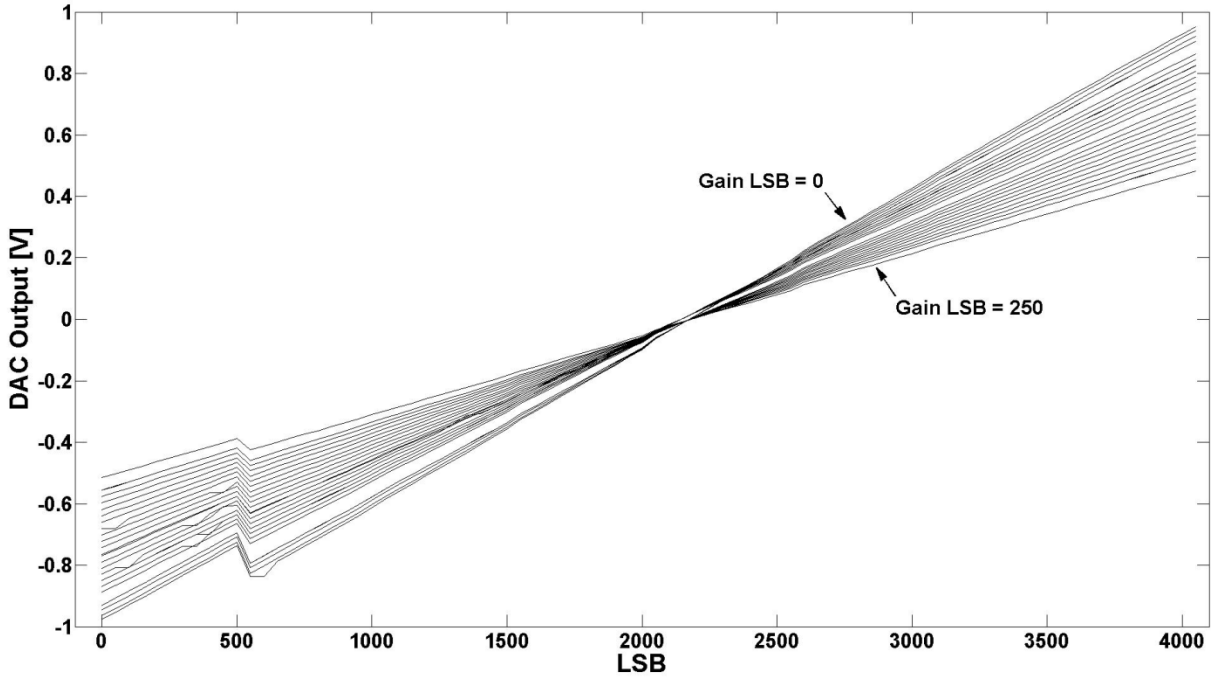

Figure 4-7 Measured DAC output ramps with varies gain settings

Due to the uncalibrated state of the DAC the output ramp of the DAC is not perfectly linear and a voltage jump at the beginning of the output ramp is observed. Nevertheless, the gain of the ramp is constant over the whole FSR. For this reason we fitted the output curve of the DAC after the nonlinearity to calculate the DAC gain for each gain setting. The result is shown in the following figure.

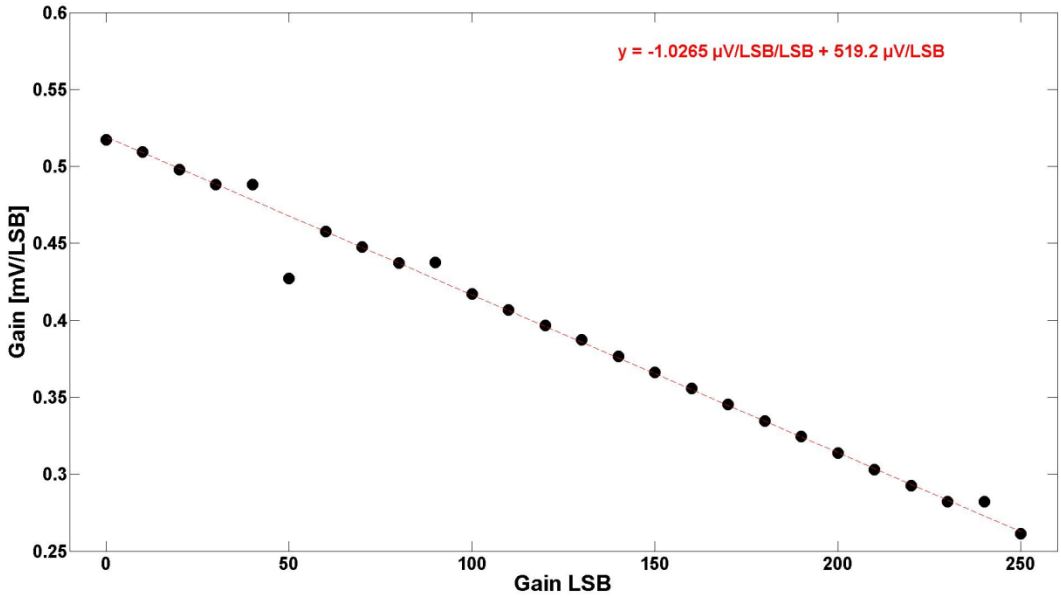

Figure 4-8 Measured and fitted DAC gain in dependency of the gain setting

4.1.2.3 SFDR tests DAC-0150

- Measurement description

1. DUT is initialized and switched to the MUX mode 1:1 by external pins.
2. Input clock frequency is set to 1.5 GHz.
3. 12 bit sinusoidal signal is applied at DUT input with various carrier frequencies.
4. Supply voltages: VDD25=2.5V, DVCC25=2.5V, AVCC35=3.5V
5. The gain register (NE: 0x34) is set to the middle value of 0x80.
6. The outputs of DUT are observed at oscilloscope and spectrum analyzer.

- Results

The minimum measured SFDR of uncalibrated DAC is very low, which might be caused partially also by the propagation delays mismatch in the measurement set-up. The best performance is obtained with 100 MHz sinusoidal signal.

Table 4-3 Measured SFDR of uncalibrated DAC at gain of 0x80

Freq Sin [MHz]	SFDR [dBc]
15	44.5
100	49
143	45
340	43
750	49

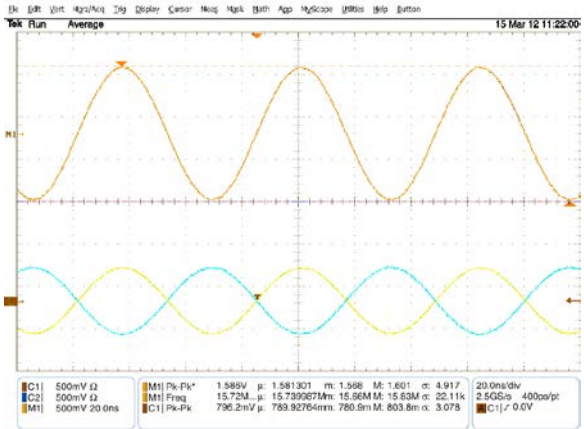

Figure 4-9 The DAC differential outputs at 15 MHz 12-bit sinusoidal signal

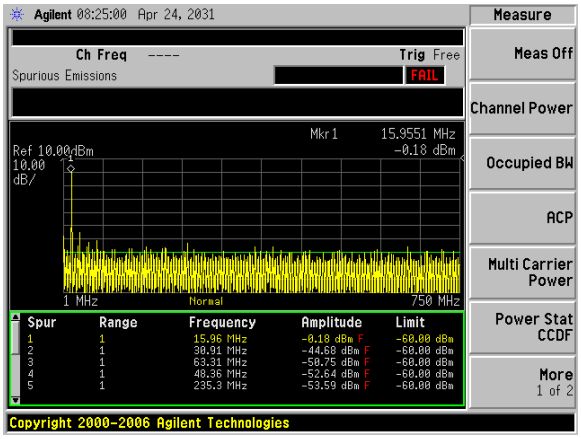

Figure 4-10 SFDR measurement at 15 MHz sinusoid

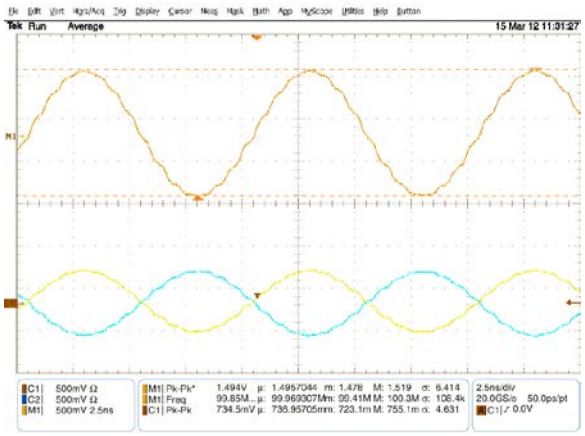

Figure 4-11 The DAC differential outputs at 100 MHz 12-bit sinusoidal signal

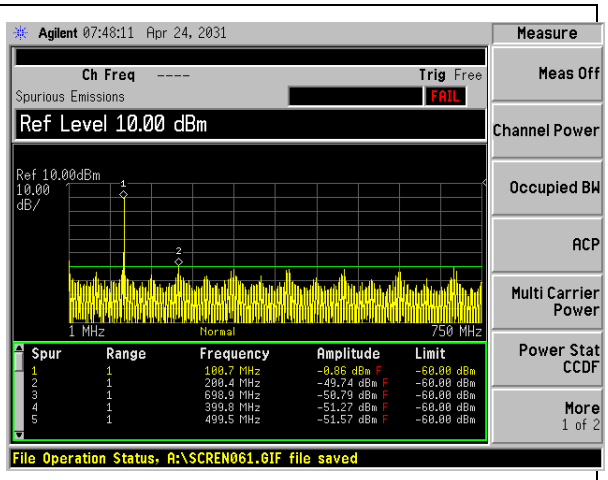

Figure 4-12 SFDR measurement at 100 MHz sinusoid

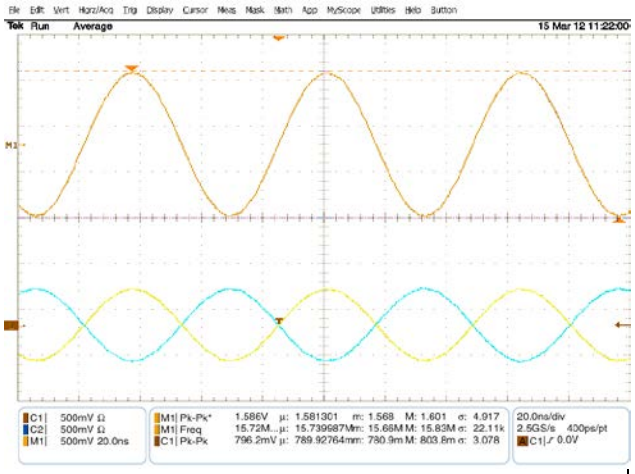

Figure 4-13 The DAC differential outputs at 143 MHz 12-bit sinusoidal signal

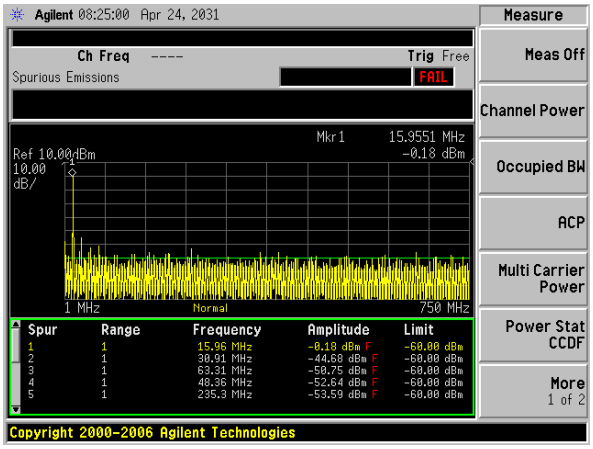

Figure 4-14 SFDR measurement at 143 MHz sinusoid

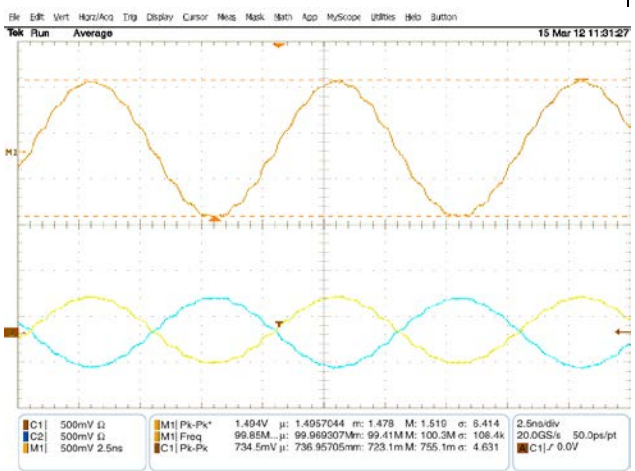

Figure 4-15 The DAC differential outputs at 340 MHz 12-bit sinusoidal signal

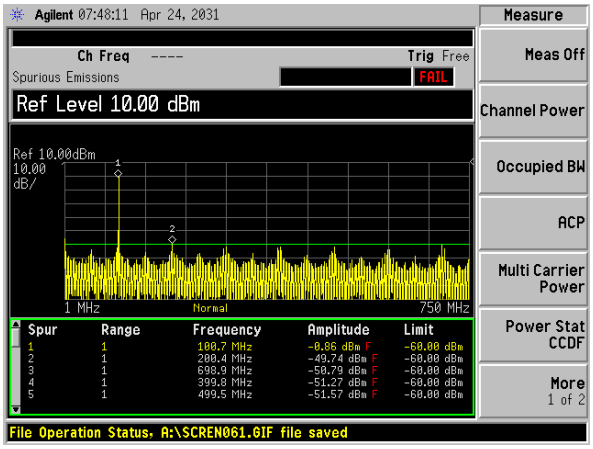

Figure 4-16 SFDR measurement at 340 MHz sinusoid

Table 4-4 lists the summary of the test results of prototype 2.

Table 4-4 List of measured parameters and comparison to the expected values

Spec. No. [3]	Spec. Item	Conditions	Required value	Measured value
	Supply voltage and current			
DAC-0065	digital power supply VDD25	min. /max.	2.4V / 2.7V	2.45V /2.8V
DAC-0070	analog power supply AVCC35	min. /max.	3.3V / 3.7V	3.3V / 3.8V
DAC-0075	interface power supply DVCC25	min./max.	2.4V / 2.7V	2.4V / 2.8V
DAC-0077	A-GND	typ.	0V	0V
DAC-0080	supply current @ AVCC35	4:1 MUX, max	118mA	216mA
DAC-0085	supply current @ AVCC35	2:1 MUX, max	118mA	216mA
DAC-0090	supply current @ AVCC35	1:1 MUX, max	118mA	216mA
DAC-0095	supply current @ DVCC25	4:1 MUX, max.	264mA	421mA
DAC-0100	supply current @ DVCC25	2:1 MUX, max	244mA	403mA
DAC-0105	supply current @ DVCC25	1:1 MUX, max	234mA	387mA
DAC-0106	add on supply RZ mode	typ, for RZ mode	23mA	25.4mA
	Static DAC Performance			
DAC-0110	Static resolution		12Bit	12 Bit
DAC-0115	INL	max.	±1.5LSB	+10/-15LSB
DAC-0120	DNL	max.	±1.0LSB	+15/-10LSB
DAC-0125	DAC full scale output	min. / max.	±0.6Vpp/±0.8Vpp	±0.5Vpp/±1.7Vpp
DAC-0130	output impedance		100Ohm±10%	100,17Ω
DAC-0140	Output voltage gain error	typ / max	±0.1/±1.0 %FSR	±0.09/±0.22 %FSR
	Dynamic DAC Performance			
DAC-0145	sampling rate	max.	1,5 GHz	1.5 GHz
DAC-0150	SFDR	min.	60dBc	43dBc – 49dBc
	Bandgap reference			
DAC-180	voltage	typ.	1.18V	1.19V
	CLK input			
DAC-210	amplitude	min.	800mV	800mV
DAC-215	common mode	min., max.	1V, 1.5V	AC coupling
DAC-220	clk frequency	max.	1.5 GHz	1.5 GHz
DAC-230	input resistance		50Ohm±10%	50.1Ω
	LVDS input specification			
DAC-240	input voltage difference	min, max.	0.2Vpp, 0.45Vpp	0.27Vpp 0.54Vpp
DAC-245	common mode voltage	min, max.	1.0V, 1.32V	1.1V 1.45
DAC-246	input voltage range	min, max.	775mV, 1545mV	0.95V 1.54V
DAC-250	input impedance	max.	100Ohm±10%	102Ω
DAC-253	data rate	MUX1:1	1500Mb/s	1500Mbs
DAC-261	skew	max.	150ps	100ps
DAC-262	Reflection coefficient @ 750 MHz		-20dB	-12.4dB
	DAC Timing specification			
DAC-365	dataready to clk edge hold time	max.	-150ps	-185ps
DAC-366	dataready to clk edge set-up time	min.	-520ps	-525ps

Spec. No. [3]	Spec. Item	Conditions	Required value	Measured value
DAC-367	total data ready window	typ.	370ps	340ps
DAC-370	dataready to data set up time	max.	30ps	130ps
DAC-371	dataready to data hold time	max.	170ps	465ps
DAC-372	Data window	max.	200ps	595ps

END OF DOCUMENT