

RECENT DEVELOPMENTS IN HIGH-END CMOS IMAGE SENSORS

3rd Round Table on Micro/Nano-Technologies for Space

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ABSTRACT

CMOS imagers are generally touted as being particularly suited to the harsh space environment, if only they could get their performance up to CCD levels. This paper highlights present-day high-end CMOS APS sensors from the commercial and industrial world. In addition, the current state of radiation tolerance is discussed.

Keywords: CMOS APS image sensors, high-speed imaging, ultra-high-resolution, radiation hardness, star trackers, visual telemetry.

1. INTRODUCTION

At the 2nd Round Table on Micro/Nano-Technologies for Space in 1997 it was suggested that CMOS image sensors, while not quite as performant as CCDs, were amenable to use in several low to medium end space imaging applications, typically applications that could cash-in on CMOS's inherent qualities/potential of system-on-a-chip-integration and simpler and/or lower power requirements (quoting from Ref.1):

- *low-grade earth and planetary imaging*
- *lander and rover near imaging*
- *robotics (requires high frame rates and windows for the simultaneous tracking of several objects)*
- *visual telemetry*
- *spacecraft optical guidance and navigation (requires low noise, high sensitivity, and high readout rates).*

At this time we have to exclude high-quality scientific imaging from the potential applications: CMOS optical sensors currently lack the required performance in noise, non-uniformity and dark signal levels and hence can not compete with high-end high-cost CCDs. The next most-demanding application would be optical navigation.

Recent developments indicate that this was a pessimistic view. Today CMOS imaging performs better than expected, and gets into domains where CCDs are not even feasible.

For instance the first-generation IMEC APS sensor developed in the ESA contract Attitude Sensor Concepts for Small Satellites (ASCoSS, Ref.2) led to a miniature star tracker breadboard with an accuracy and a Noise

Equivalent Angle both better than 1 arc minute (2σ) per $5m_v$ star in a $20^\circ \times 20^\circ$ field of view, at an update rate of 10Hz. The sensor performed with the same signal to noise ratio, for a given optics aperture, as a CCD. In addition, the sensor proved radiation-tolerant at the dose rates encountered during typical missions (Ref.3), and this without any rad-hardening design measures. IMEC and its imager spin-off company FillFactory are now cooperating in the development of the next-generation CMOS sensors for star and sun sensing.

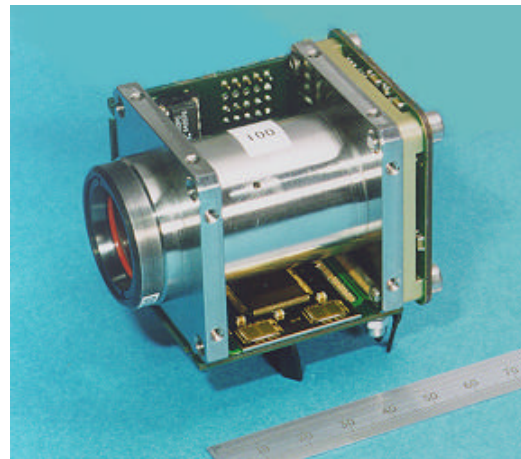


Figure 1: ASCoSS APS-based star tracker breadboard

In the field of spacecraft visual telemetry, experience has been amassed on two flights, with two more flights scheduled for the near future: FUGA15 sensors were demonstrated on Ariane V testflight A-502. These are continuous-readout APS imagers, with a logarithmically compressing opto-electric transfer which allows for a huge input dynamic range. As a drawback, this sensor architecture has high noise, and even more importantly, a high static non-uniformity that has to be removed by look-up-table correction even before attempting image processing and data compression.

Normal CCDs and APSs imagers (ideally) have low noise, low non-uniformity, and a linear transfer function. Such a sensor was tried in-flight too, alongside the trusty FUGA15, on the XMM mission. The sensor, named IRIS1, was developed at the end of 1997, as part of an ESA contract. Two lessons learned were, one, that it is fairly hard to predict illumination conditions in order to set the correct exposure time on a linear-transfer camera, and

two, that the contrast in a typical space telemetry scene (i.e. black sky, sun, earth, dark spacecraft, reflections off metallic parts, ...) demands for more than the 60-70dB dynamic range allowed by CCDs or APSs.

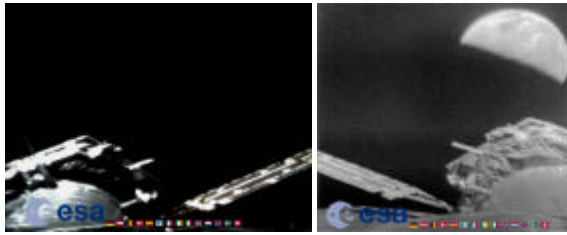


Figure 2: XMM mission visual telemetry, left IRIS1 picture, right FUGA15 picture. Observe limited contrast, exposure problems, and lower noise with IRIS1.

2. HIGH-DYNAMIC RANGE IMAGING

A method has been devised to allow a linear-transfer APS to accept an intra-scene contrast normally exceeding its dynamic range, and this in one single image exposure, i.e. without reverting to combining two or more separate images each made with a different exposure time.

To obtain this the pixel has been modified to collect photocharges at its highest sensitivity up to a certain threshold, after which the pixel's transfer reverts to the sensitivity commanded by the imager's electronic shutter. This yields a two-piece transfer curve with a compressing character. The knee in the curve can be set to a fixed position, or alternatively it can be controlled more dynamically with an external digital-to-analogue convertor.

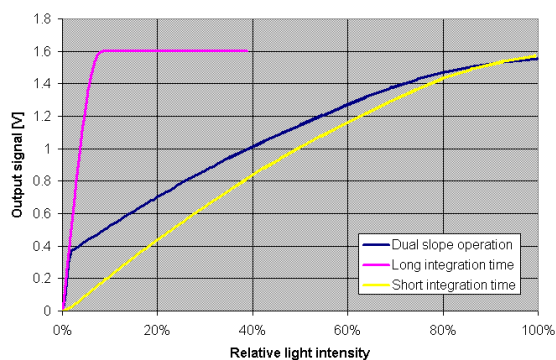


Figure 3: integrating APS transfer curves for long exposure time, short exposure time, and dual-slope combination of both.

3. A 3k x 2k HIGH-RESOLUTION SENSOR

In 1999 an APS imager was realised targeted at true-negative size 35mm digital studio-quality photography (Creo-Scitex Leaf C-MOST™ camera). This sensor not only has a for CMOS unprecedented resolution of 3000 by 2000 pixels, it also had to overcome the 19 mm x

19mm reticle size limit imposed by the silicon fabrication process.

The latter problem was side-stepped by using the stitching technology offered by the fab, Tower Semiconductor of Israel. Stitching, a technique inherited from the CCD-world, allows a chip to be built of several mask sets that each individually undergo their own exposure and processing steps. This way a chip larger than the reticle can be built from modules, each smaller than the reticle. To obtain a total die size of over 38 x 27 mm, six modules were used, including one 1k x 1k pixel array block, and upper/lower and side periphery blocks.

During pixel design noise and saturation levels were optimised for the dynamic range demanded by the particular application.

FillFactory high-resolution APS

Photosensitive area	24x36mm (35mm film negative format)
Number of pixels	3150 x 2100
Pixel size	11.4µm (.5µm process)
Number of analogue outputs	4
Sensitivity	> 9µV/e-
Fill factor	55%
Electronic shutter	Rolling curtain
Noise level	< 40e-
Saturation level	> 140000e-
Dynamic range	> 70dB
Double Sampling	On-chip
Non-uniformity	< 1%
Readout speed	250 ms
Colour	Optional
Power	< 250mW

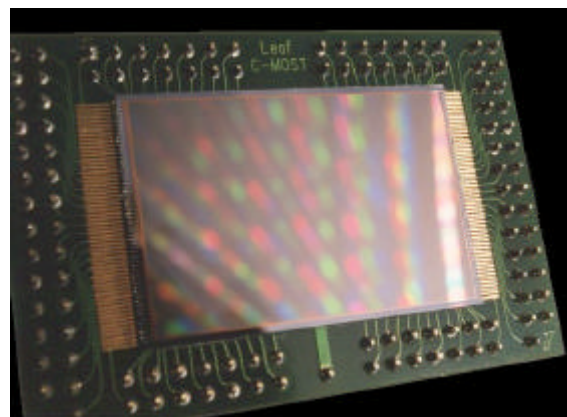


Figure 4: 35mm CMOS APS with chip-on-board packaging.

To safeguard the sensor's noise performance no logic or ADC has been included on the chip: external components are to be used. From a systems point of view this is still acceptable, as quality cameras tend not to be of minimal dimensions anyway. The power requirements are a

standard 5Vdc. Operation with elevated supply voltage is possible too, in which case the sensor's dynamic range increases.

4. A 1000pps HIGH-SPEED IMAGER AND CAMERA

High-speed imaging traditionally has been the domain of photochemical pellicule film cameras, a technology that can attain frame rates in the tens of thousands per second, at the expense of bulky equipment and even more bulky reels of film. The application of standard CCDs in this field is hindered by an imperfect charge transfer, leading to ghost images, especially in over-illuminated parts. The best high speed CCDs today are limited to 1000 frames/sec at a resolution of 512 by 384 pixels (e.g. Kodak EKTAPRO series). The very first generation of dedicated high-speed CMOS APS already exceeds CCD performance: the Photobit PB-1024 is a sensor with 1k x 1k pixels at 500 images/second, while the device presented here performs at 512 x 512 pixels and 1000 frames/second, with its technology still enabling a considerable growth in sensor format and resolution.

The latter has been designed by FillFactory for US company Vision Research, which commercialises it in their Phantom camera range. The sensor uses a six-transistor active pixel that avoids ghost imaging by means of its immediate conversion of photocharge to voltage. The pixel also implements a true synchronous shutter (i.e. snap shot shutter) that allows exposure times for the whole array to be instantaneous and as low as 10 microseconds. While CCDs implement synchronous shuttering by the interline architecture or the frame transfer architecture, this APS device has an analogue memory element located in each pixel. Sensitivity does not suffer thanks to FillFactory's patented near-100%-fillfactor technology which was pioneered in the Ibis-1 device in 1997 (Ref.1). The pixel's sensitivity, noise, and saturation levels were optimised for the highest possible sensitivity, to allow for the ultra-short exposure times demanded by the application.

FillFactory high-speed APS

Photosensitive area	8x8mm
Number of pixels	512 x 512
Pixel size	16µm (.5µm process)
Number of analogue outputs	16
Sensitivity	25µV/e-
Fill factor	50%
Electronic shutter	Synchronous, true snapshot
Dynamic range	> 58dB
Double Sampling	-
Readout speed (nominal)	1000 frames/second
Readout speed (windowed)	32000 frames/second
Colour	Optional
Power	600 mW

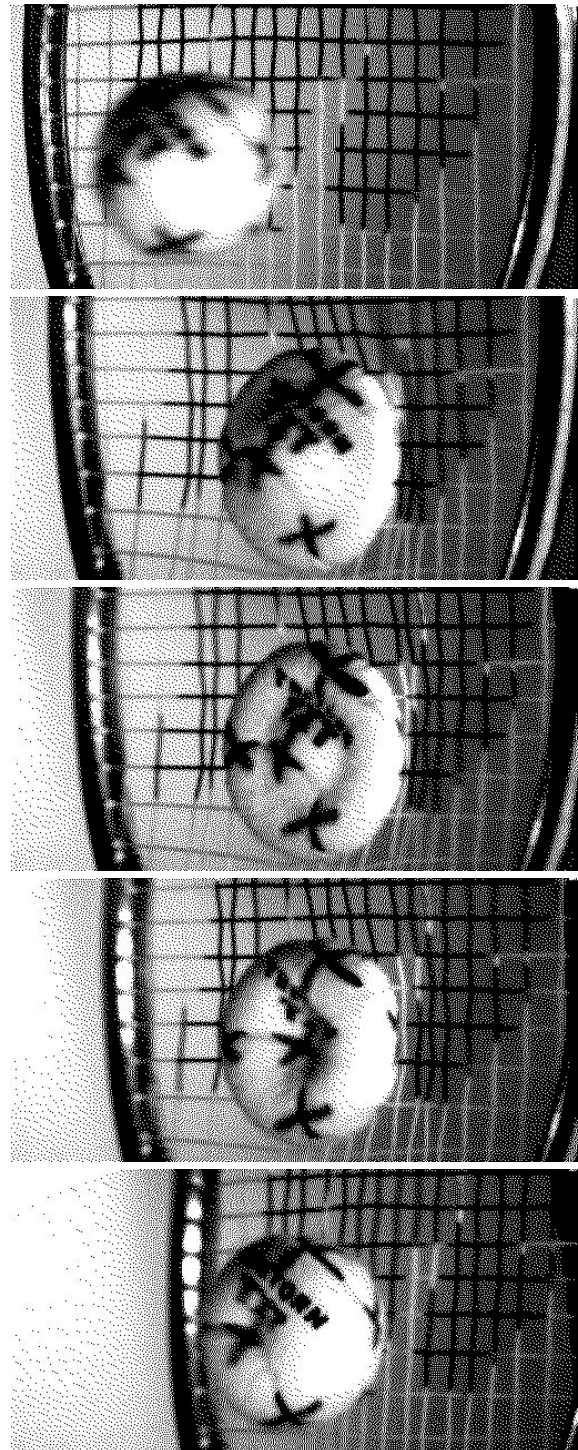


Figure 5: 2000 frames/s tennis ball sequence filmed with Phantom v4.0 camera (reduced to dithered black&white for reproduction)

Vision Research Phantom v4.0 camera

Frame storage	Up to 512 megabyte
Interfacing	Firewire, sync, video
Dimensions	8x10x25 cm
Mass	2250g
Build	Rugged, high-g
Power	28Vdc/1A

Typical ground-based applications are crash-tests and sports motion analysis. Space applications that could be envisaged are microgravity physics experiments (fluid dynamics, ...), robotics, and analysis of thruster plumes.

5. RECENT DEVELOPMENTS IN RADIATION HARDENING

Total dose irradiation tests on standard CMOS APS pixels show a significant loss of functionality after irradiation with γ rays to doses between 50 and 200 Gy(Si) [5-20 krad(Si)], depending on the technology, the layout of the pixel, and the dose rate (Ref.3). An increased reverse current of the silicon photodiodes and an enhanced leakage current of the reset transistor in the active pixel, through its parasitic field transistor, cause this failure. As a consequence, nMOS-based pixels show a large increase in dark current, while the integration of the actual photocurrent on the pixel capacitance is virtually obliterated by the leakage currents of the transistors, pinning the pixel's output voltage to a certain level (Ref.4).

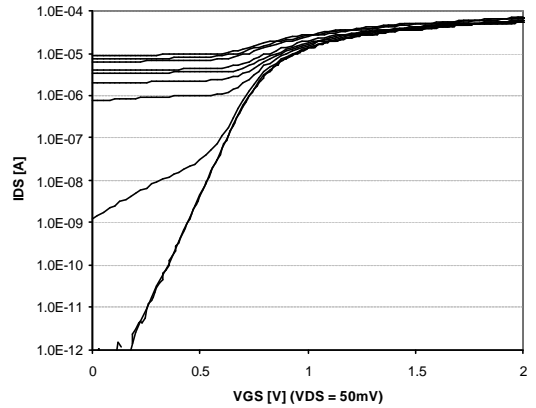
Alternatively, pMOS pixels do not suffer as obviously from radiation effects as they are not plagued by the parasitic field transistor. Yet, their application in imagers is still less attractive as these pixels have a considerably lower sensitivity than nMOS ones.

IMEC developed, partly funded by ESA, a new nMOS pixel architecture that preserves the electro-optical sensitivity of the type, while adding to it an increased tolerance towards γ -irradiation, showing only a gradual deterioration up to doses exceeding 20 megarad, 200kGy(Si). The major drawback of the technique is in its inherently larger pixel size, as indicated in the following table:

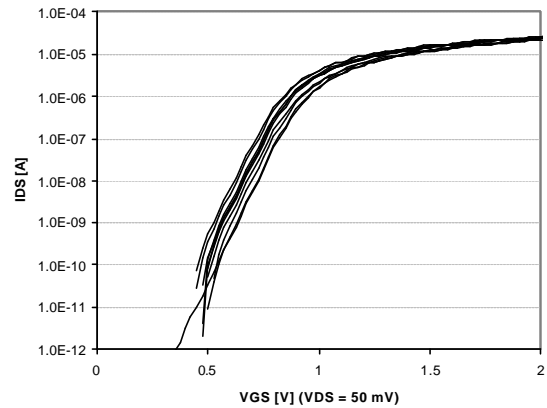
Process feature size (μm)	miminal nMOS pixel pitch (μm)	rad-hard nMOS pixel pitch (μm)
.7	14	20
.5	8	15
.35	5	8

Figure 6 (a) shows the input characteristics of a $5 \mu\text{m}/1 \mu\text{m}$ nMOS transistor in a $0.7 \mu\text{m}$ CMOS technology. A large increase in leakage current can be observed due to the parasitic field transistor parallel with the drawn transistor. Nevertheless, the results show that the thin gate oxides that are used in currently available CMOS technologies can withstand several kGy(Si) while the leakage can be avoided by appropriate design techniques (fig. 2 (b)). The voltage threshold shift, which results from the positive charge build-up in the gate oxide, does not disturb detrimentally the operation of the pixels. The thickness of the gate oxide still decreases for smaller feature technologies. Therefore, the shifts become smaller

and technologies become more tolerant with respect to total ionising dose.



(a)



(b)

Figure 6: (a) Input characteristics of a $10\text{nm}/1\text{nm}$ nMOS transistor processed in 0.7nm . A large increase in leakage current can be observed due to the parasitic field transistor. (b) Input characteristics of a $10\text{nm}/2.8\text{nm}$ 'enclosed' nMOS transistor processed in a 0.5nm technology. No leakage current increase can be observed.

Figure 7 gives the dark current measured at the output of a complete rad-hard pixel. Its pre-irradiation value is about 30 mV/s . If a pixel photodiode capacitance of 10 fF (from calculations and measurements on standard pixels) is assumed, this value corresponds to a dark current of 225 pA/cm^2 . The specific design of this pixel avoids leakage of the transistors and leads to a largely decreased dark current growth. The dark current values that are observed in this pixel after more than 200 kGy(Si) , are already obtained after less than 200 Gy(Si) in standard pixels. At low doses, the dark current increases linearly as seen in Figure 7. The increase is larger in case of a continuous bias of the reset pin.

However, in practice the reset line is pulsed a few times per second and the dark current increase is smaller. In this experiment, which lasted for several weeks, the ^{60}Co

irradiation (dose rate 350 Gy(Si)/h) was stopped for 562 hours after 33.8 kGy(Si). During this period, significant annealing was observed indicating that dark current degradation might be very low in the low dose rate space environment where long-term annealing may occur.

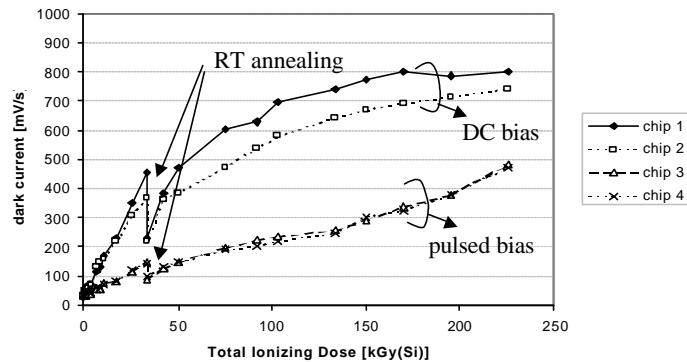


Figure 7: dark current after irradiation, rad-hard pixel in Alcatel Microelectronics .7 μ m technology.

Present on-going work is the application of the underlying hardening principles to imager peripheral circuits such as ADCs and correlated double sampling amplifiers. The technology will be used in a forthcoming new generation APS sensor for star tracking and other attitude sensing applications. A stripped-down version of the technology will be used in the IRIS3 camera-on-a-chip, which will feature a 1024x768 resolution and direct interfacing to SDRAM memory banks for image storage and to an image compression device.

Note that due to the larger dimensions of radiation-hard pixels the technology is not amenable to very high resolution imagers: with a .5 μ m process imagers up to 1000x1000 are feasible when the peripheral electronics are not hardened, and 800x800 with full hardening. With a .35 μ m process these figures improve to 2000x2000 and 1200x1200. All this of course without stitching. With stitching almost arbitrary sensor sizes become possible, essentially only limited by speed and yield.

7. CONCLUSIONS

The future looks bright for CMOS image sensors for space applications. Basic research into radiation hardness soon may yield devices performing well up to hundreds of kilorads and beyond, with the actual pixels breaking the megarad barrier.

For industrial applications, sensors have been demonstrated exceeding six megapixels in resolution with a high dynamic range, and others with full frame rates of 1000 images/second. The technologies used in these sensors can be applied to obtain even higher performances. It is to be expected that smaller-feature CMOS processes, i.e. .35 μ m and beyond, will help in

combining radiation-hardness and high-performance for space use.

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High-speed images courtesy of Vision Research Inc., Wayne, New Jersey, USA

Space images courtesy of ESA/ESTEC, Noordwijk, the Netherlands

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