SEFUW: SpacE FPGA Users Workshop, 1st Edition

Preliminary Agenda (To be updated at the end of the week)

Presentations and time slots might change (not all presentations are included)
Final titles as well as short Abstracts will be included

Tuesday 6th November	
09:15	**Welcome** by David Merodio Codinachs (ESA), David Dangla (CNES) Bernard Bancelin (Atmel)
Session 1	European FPGA industry
09:30	***ATMEL General presentation*** Atmel
10:00	**Mentor**
10:30	***ATMEL Current IDS status and results*** Atmel
11:00 Coffee Break	
11:30	***ATMEL Future enhancements*** Atmel
12:00	***Flexras***
12:30	***NanoXplore*** Olivier Lepape, NanoXplore
13:00 Lunch Break	
Session 2	Space industry experiences
14:00	***CNES: European FPGA products*** CNES, David Dangla
14:20	***Atmel FPGAs at Astrium***, Alfonso Gonzalo, EADS Astrium Crisa
14:50	"***Example of use of the ATF280 in the Simbio-Sys instrument (BepiColombo)***" Vincent Carlier , IAS- Orsay,
15:05	"**SVOM mission: ATF280F/AT697F data processing for real-time GRB detection and localization & ATF280E SpaceWire CEA IP recent developments**", Hervé Le Provost , CEA
15:30	"***ATF280 projects in Thales Alenia Space***" Xavier Chebanier, Thales Alenia Space
15:30 Coffee Break	
16:00	***IP implementations in FPGAs*** Mercier Maya, Maya Technologies
Session 3	Tools
16:25	"***External Routing for Atmel IDS tool***" ESA/Torino, Nikos Andrikos
16:45	"***FT-UNSHADES 2***" Miguel A. Aguirre, Universidad de Sevilla
17:05	"***CAD tools for SEU simulation, test pattern generation and untestability proofs of SEUs in SRAM-FPGA based systems***" Luca Cassano, University of Pisa
17:25	***General Discussion***
17:45 – 18:30	***Demos and workshops***

Wednesday 7th November	
08:50	Welcome by David Merodio Codinachs (ESA), David Dangla (CNES)
Session 1	Non-European FPGA industry
09:00	***Microsemi SoC products*** (Detailed topics to be included)
10:00	***Xilinx FPGA space products, part 1*** (Detailed topics to be included) Joe Fabula, Xilinx
11:00 Coffee Break	
11:30	***Xilinx FPGA space products, part 2*** (Detailed topics to be included) Joe Fabula, Xilinx
12:00	**Panel**: "Re-configurability for space"
13:00 Lunch Break	
Session 2	Space industry experiences
14:00	***Xilinx at EADS Astrium*** EADS Astrium, Rajan Bedi
14:30	"***Dynamically Reconfigurable Processing Module (DRPM), application on instruments and qualification of FPGA package***" Björn Fiethe , IDA-TU Braunschweig
14:50	"***DRPM architecture overview***" Mario Porrmann, University of Bielefeld
15:20	**Terma** (TBC)
15:50	***Microsemi at EADS Astrium*** Ottmar Ried , EADS Astrium
16:10 Coffee Break	
Session 3	Tools
16:30	"***Soft Errors in Partially and dynamically reconfigurable SRAM-based FPGAs***" Massimo Violante, Politecnico di Torino
17:00	"***Single Event Transient Effects on Microsemi ProASIC Flash-based FPGAs: analysis and possible solutions***" Luca Sterpone, Politecnico di Torino
17:30	**General discussion**
18:00-18:10	**Wrap up**

Note to all attendees: you are encouraged to propose topics to be addressed in the General Discussions parts. Please send an email to david.merodio.codinachs@esa.int with topics you would like to discuss. (Please include in the Subject of the email "SEFUW general discussion topics".