DRPM architecture overview

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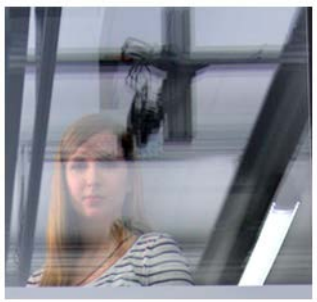
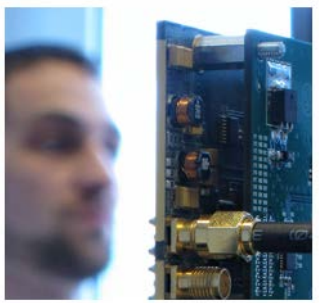
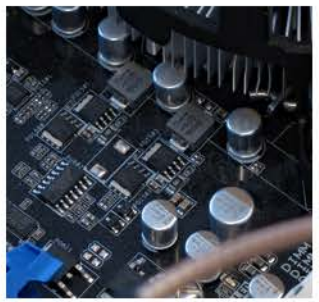
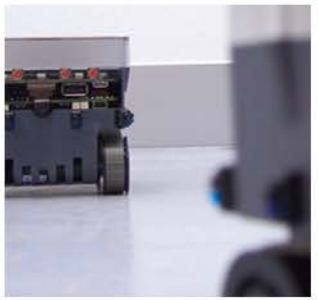
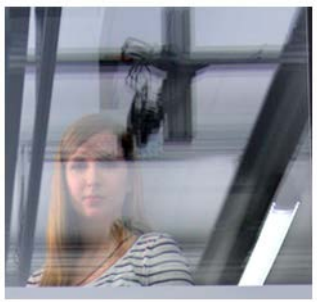
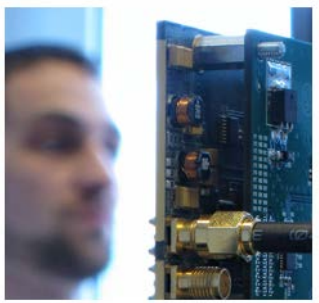
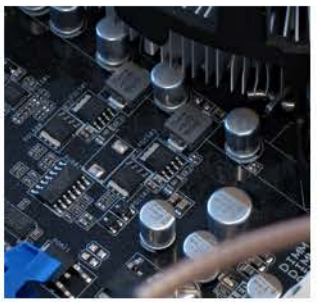
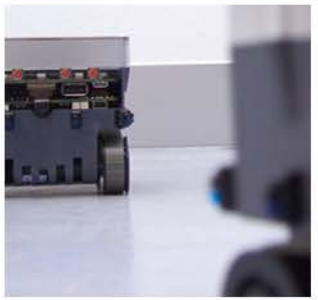
Project partners:

European Space Agency, ESTEC, Netherlands
Politecnico di Torino, Italy
Swiss Space Technology, Switzerland
TWT GmbH Science & Innovation, Neuhausen, Germany

DRPM architecture overview

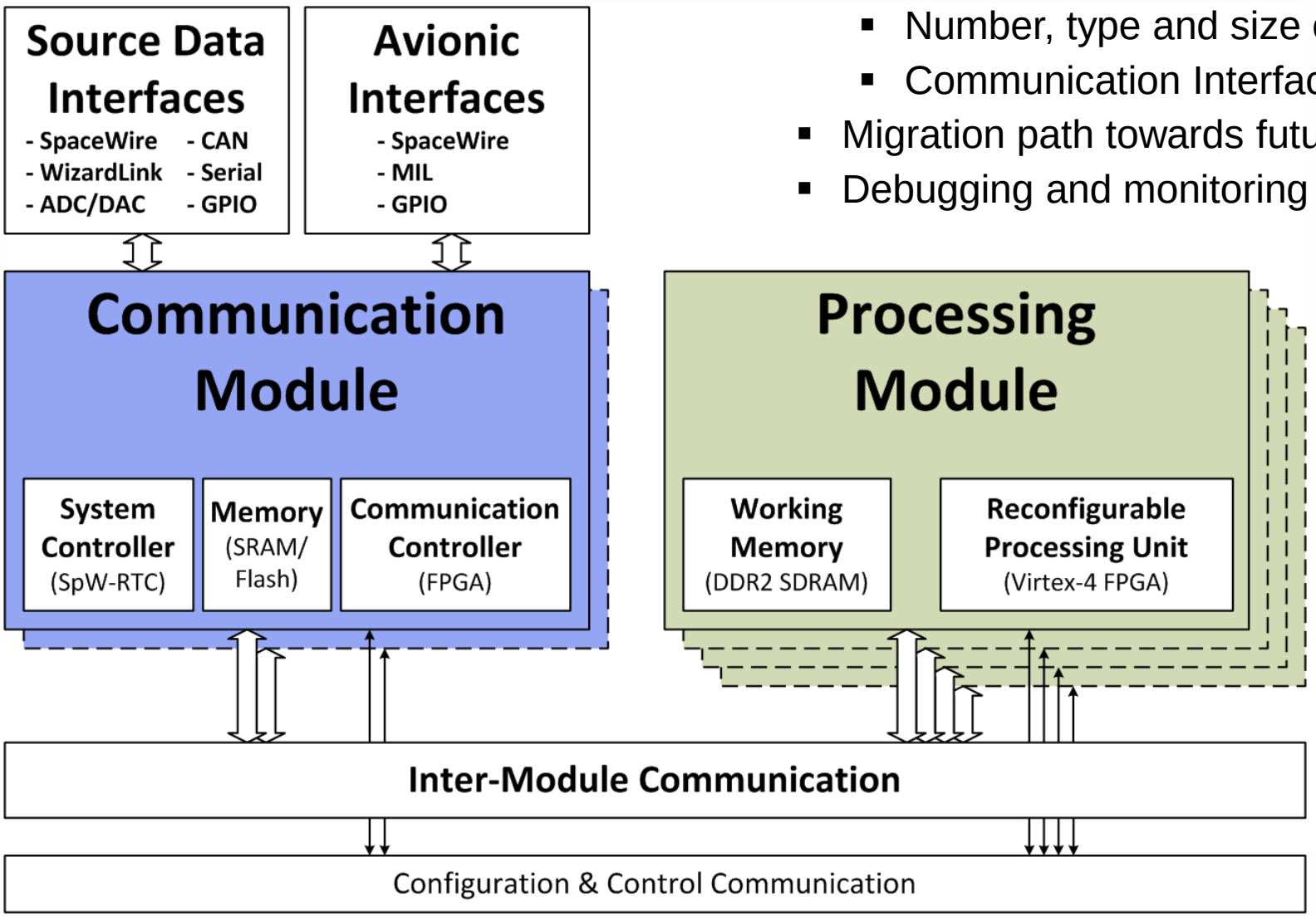
- System Architecture
- Run-Time Reconfiguration
- Communication Infrastructure

DRPM System Overview

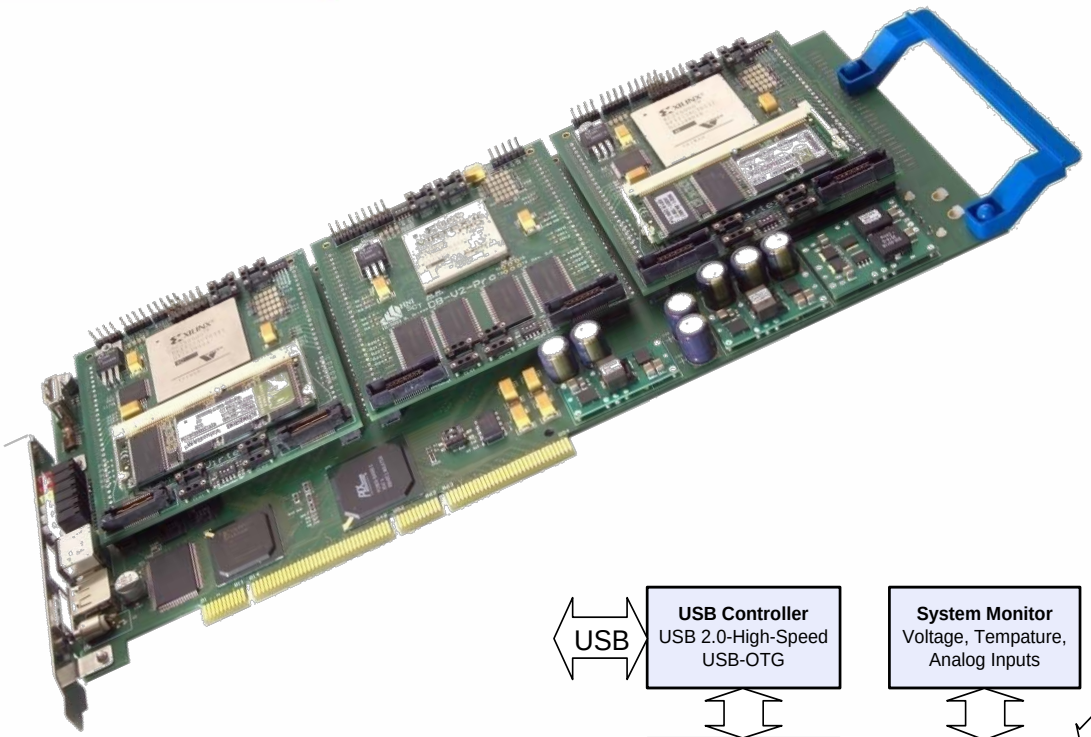
Design goals

- Scalability
  - Number, type and size of FPGAs
  - Communication Interfaces
- Migration path towards future flight versions
- Debugging and monitoring facilities



DRPM – Dynamically Reconfigurable Processing Module

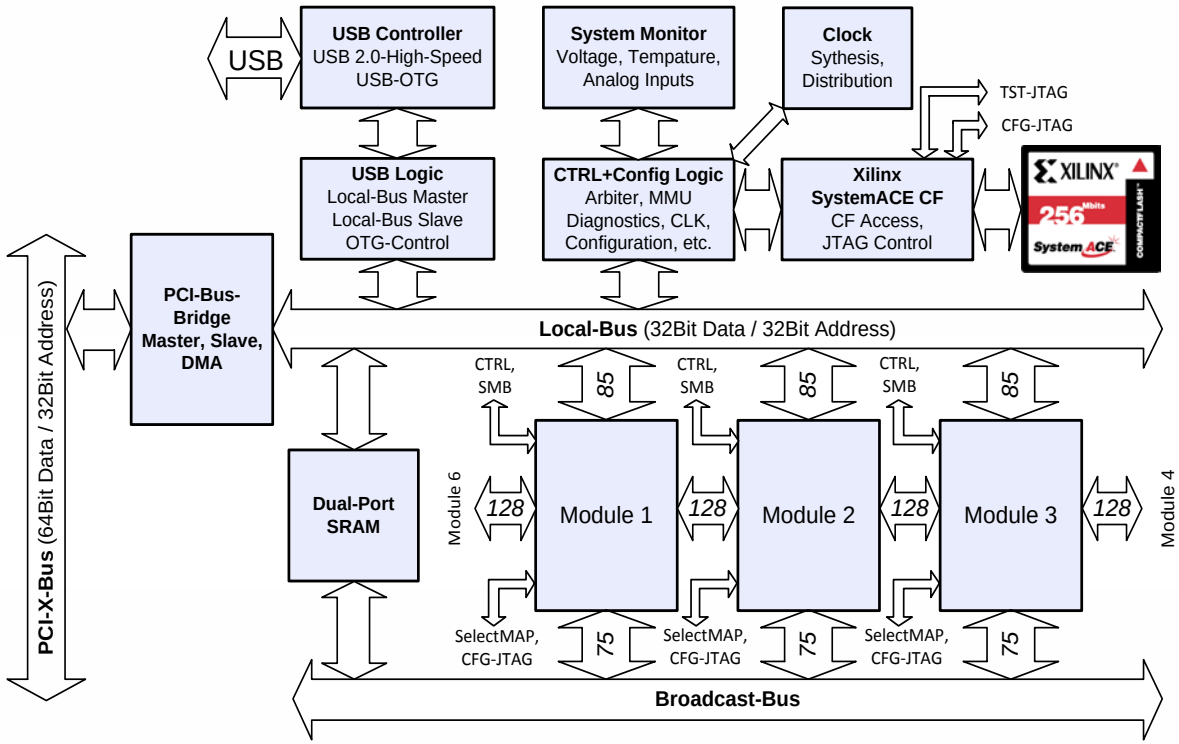
Platform for DRPM implementation



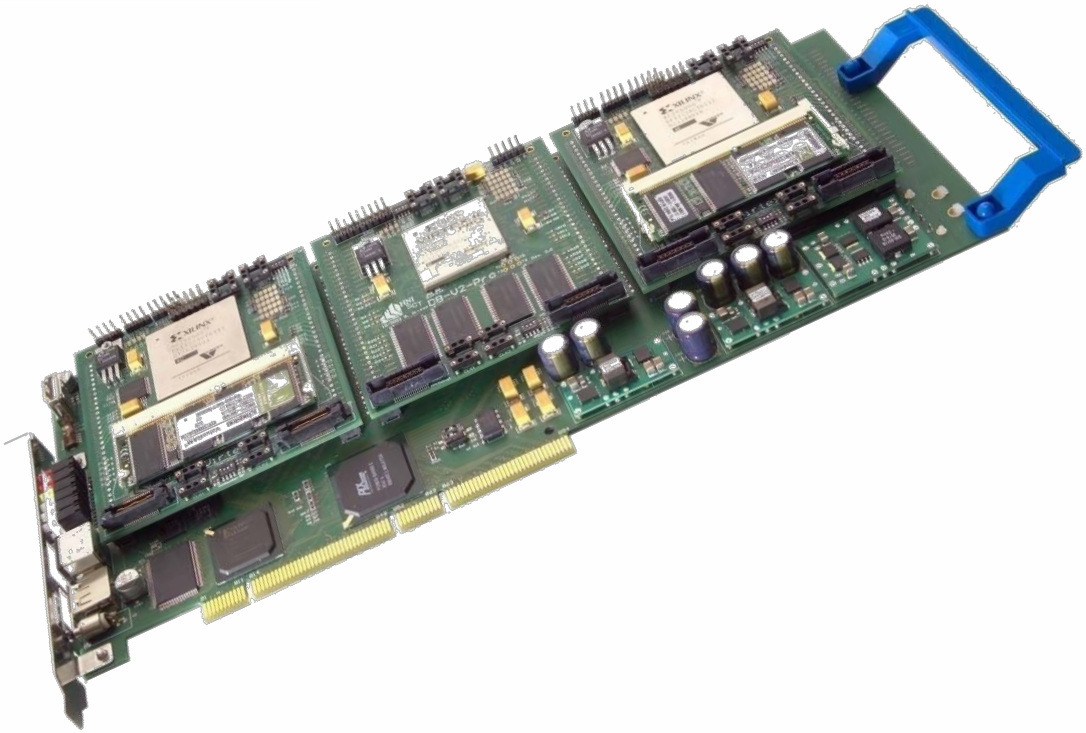
RAPTOR Prototyping Systems

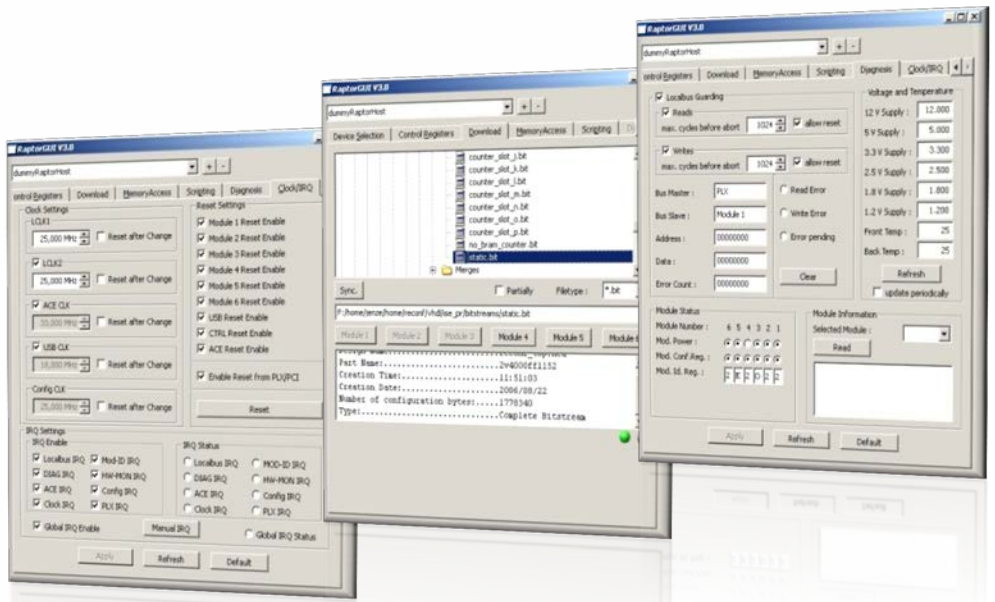
Prototypic Implementation of Microelectronic Circuits on FPGAs

- PCI-X / PCIe Mainboard
- Up to six modules
- High bandwidth between modules
- Partial dynamic reconfiguration



Platform for DRPM implementation





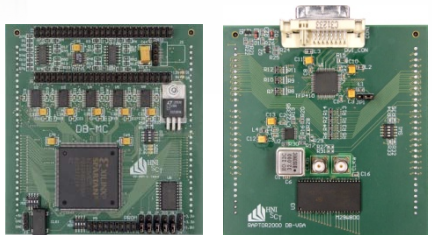
FPGA-Modules

- Xilinx FPGAs up to Virtex 5 (7-series in design)
- Embedded processors
- Up to 4 GB SDRAM

Communication

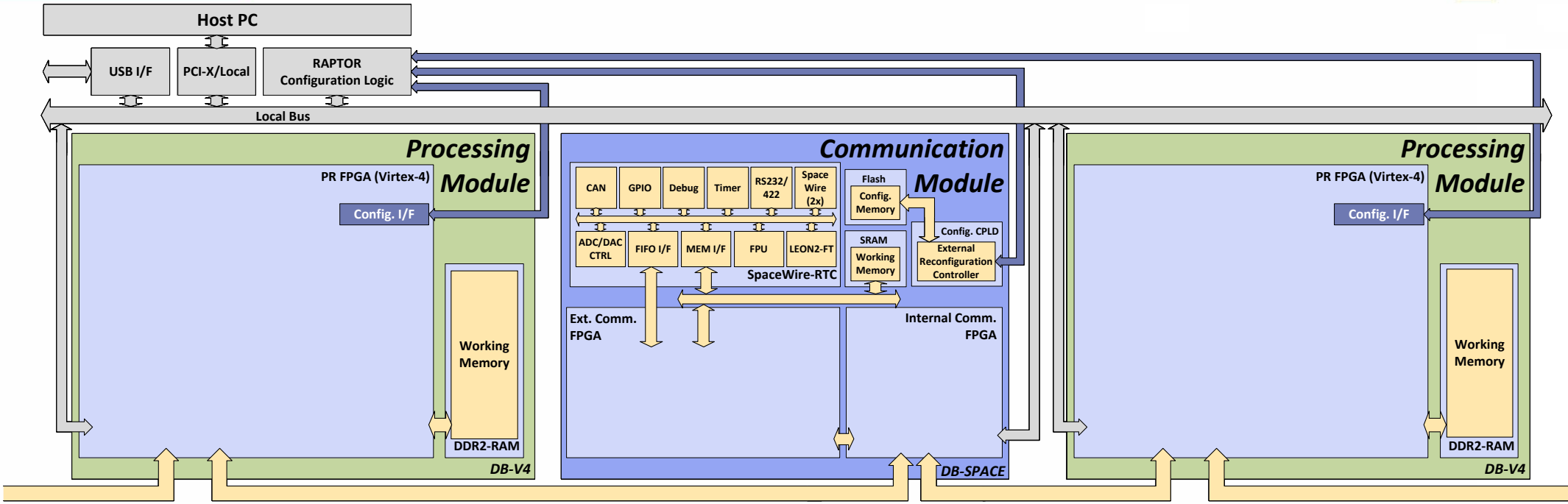
- Ethernet
- FireWire, USB
- CAN, LON, EIB, Interbus
- Serial, Parallel

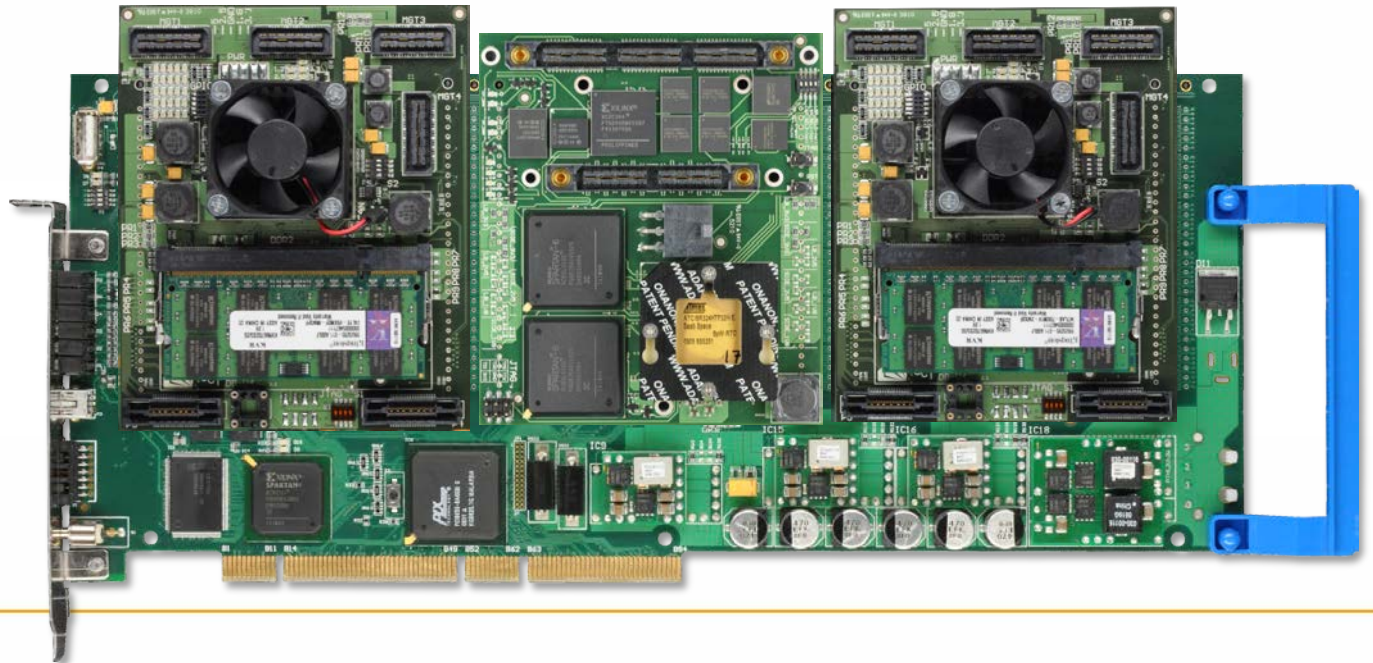
I/O-Modules



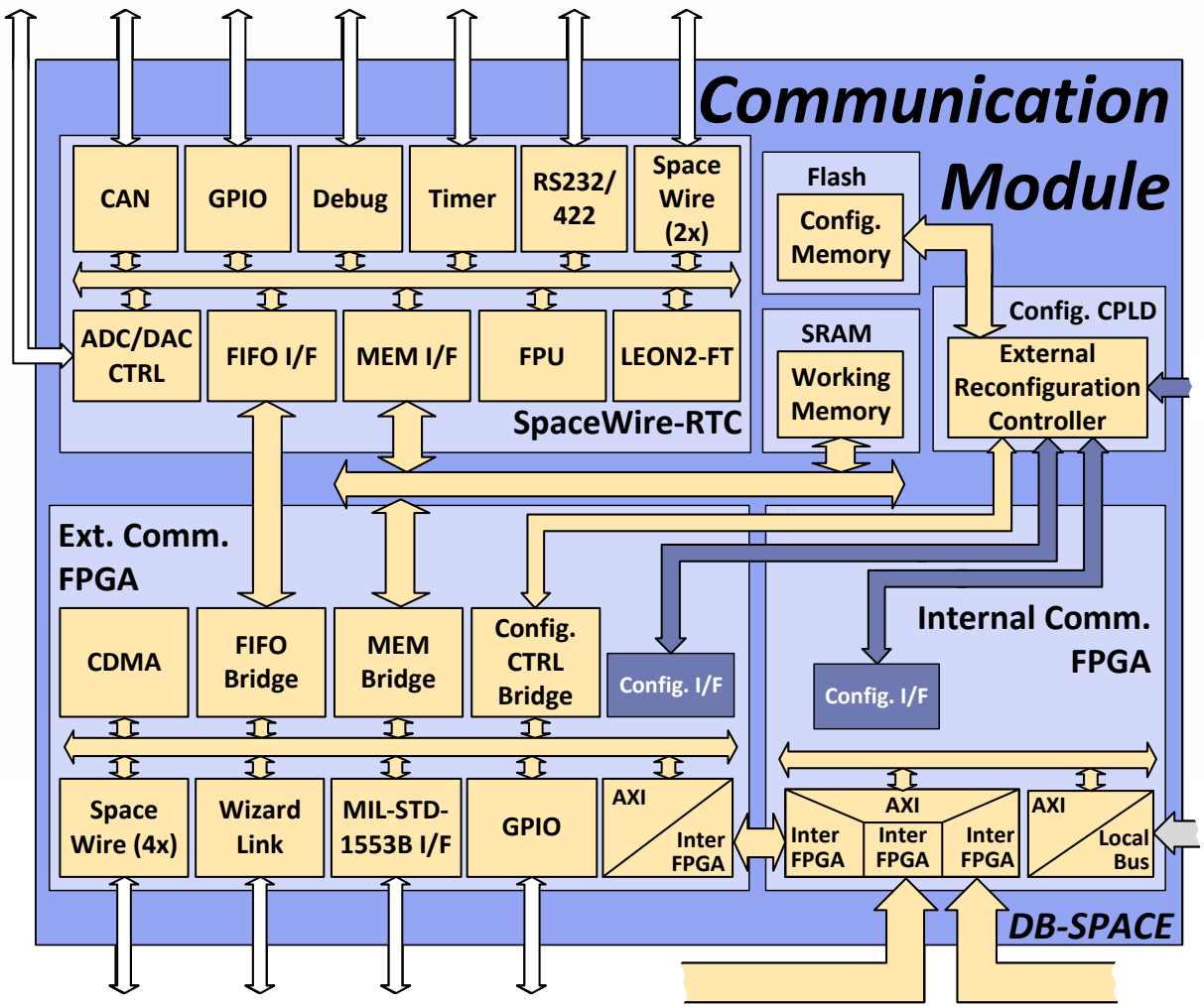
- Analog I/Os
- Digital I/Os
- SSI interfaces
- VGA interface

DRPM Overview



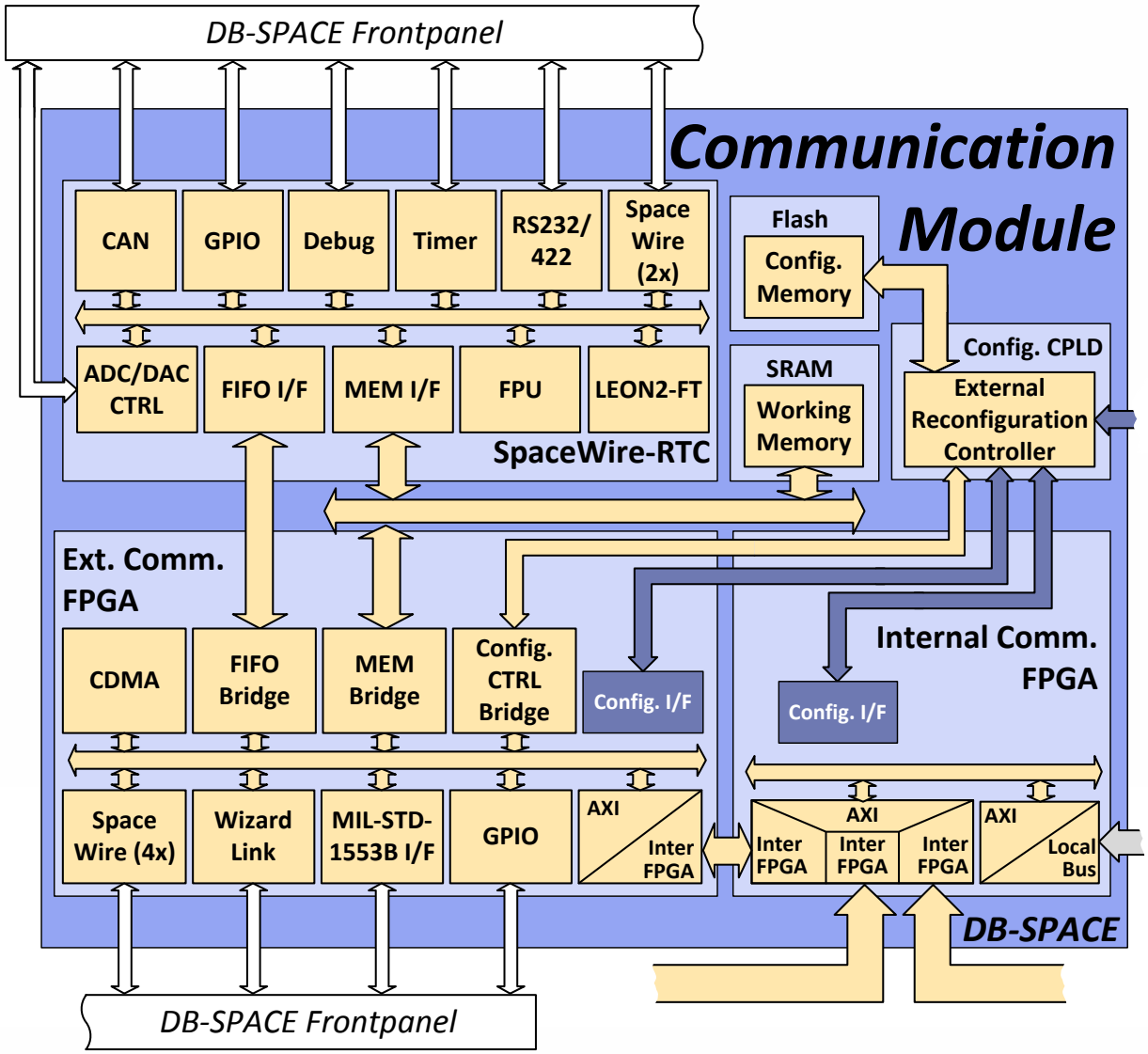


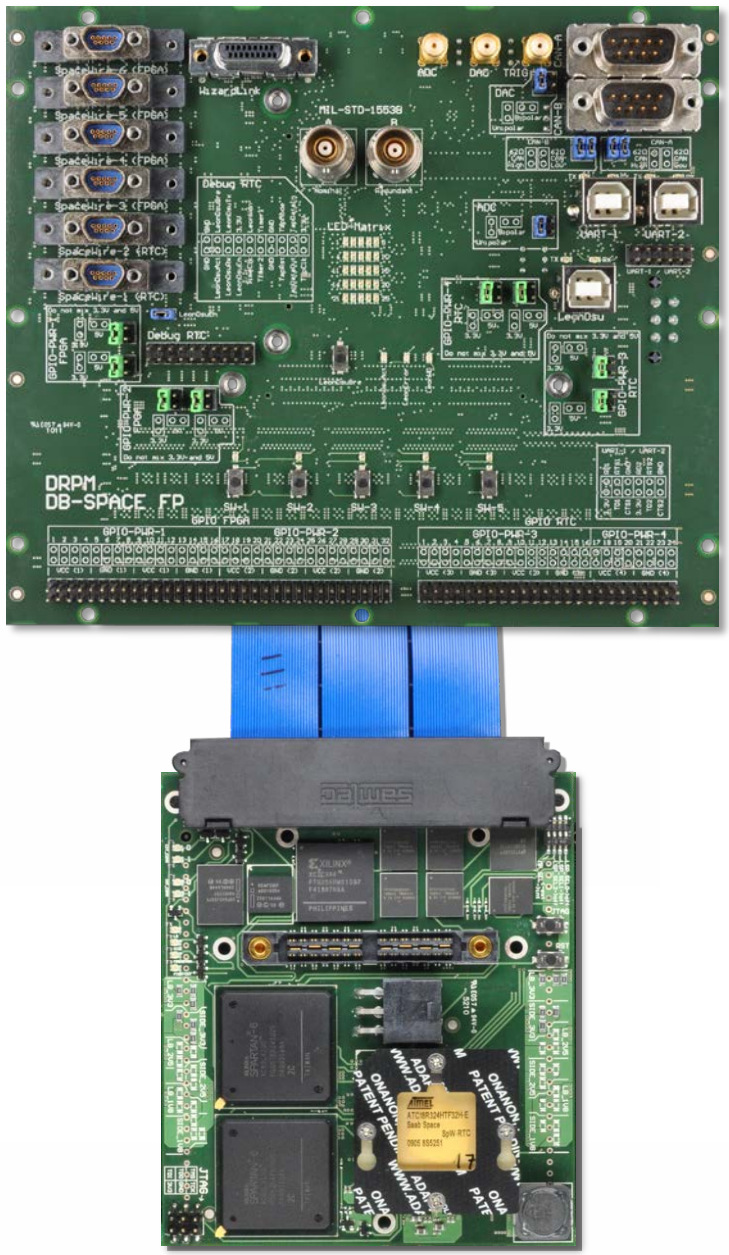
Communication Module *DB-SPACE*



- System Controller: SpaceWire RTC AT7913E
  - LEON2-FT CPU
  - 2 SpaceWire Interfaces
  - CAN, ADC/DAC, GPIO, …
- External Communication FPGA
  - 4 SpaceWire Links
  - WizardLink Interface (2.7 Gbit/s) used as PHY for SpaceFibre
  - MIL-STD-1553B
  - 32b GPIO
- Internal Communication FPGA
  - Flexible communication to other modules
  - Monitoring interface
- AMBA AXI4 communication between IP cores
- Ext. Reconfiguration Controller

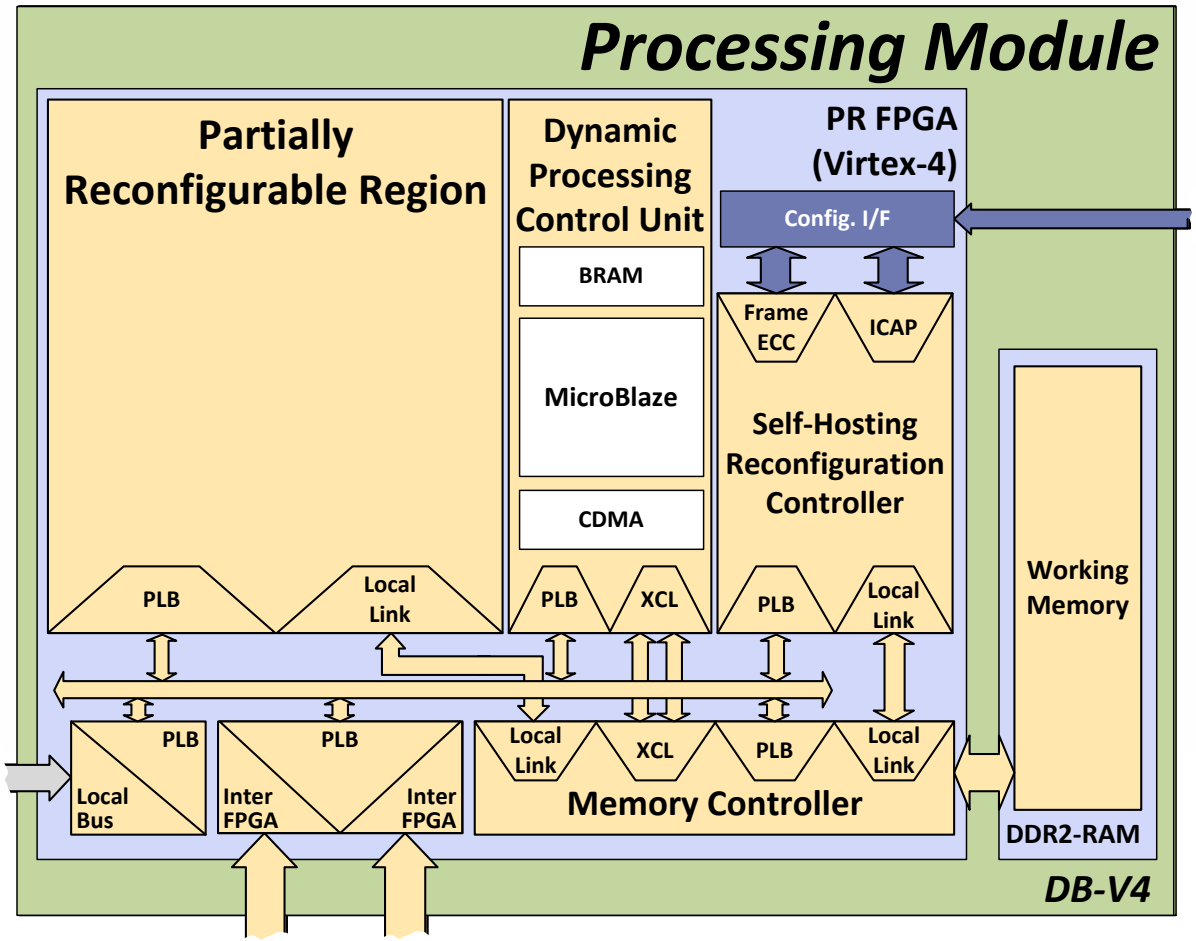
DB-SPACE Frontpanel





- Easy access to the interfaces of DB-SPACE

Processing Module *DB-V4*



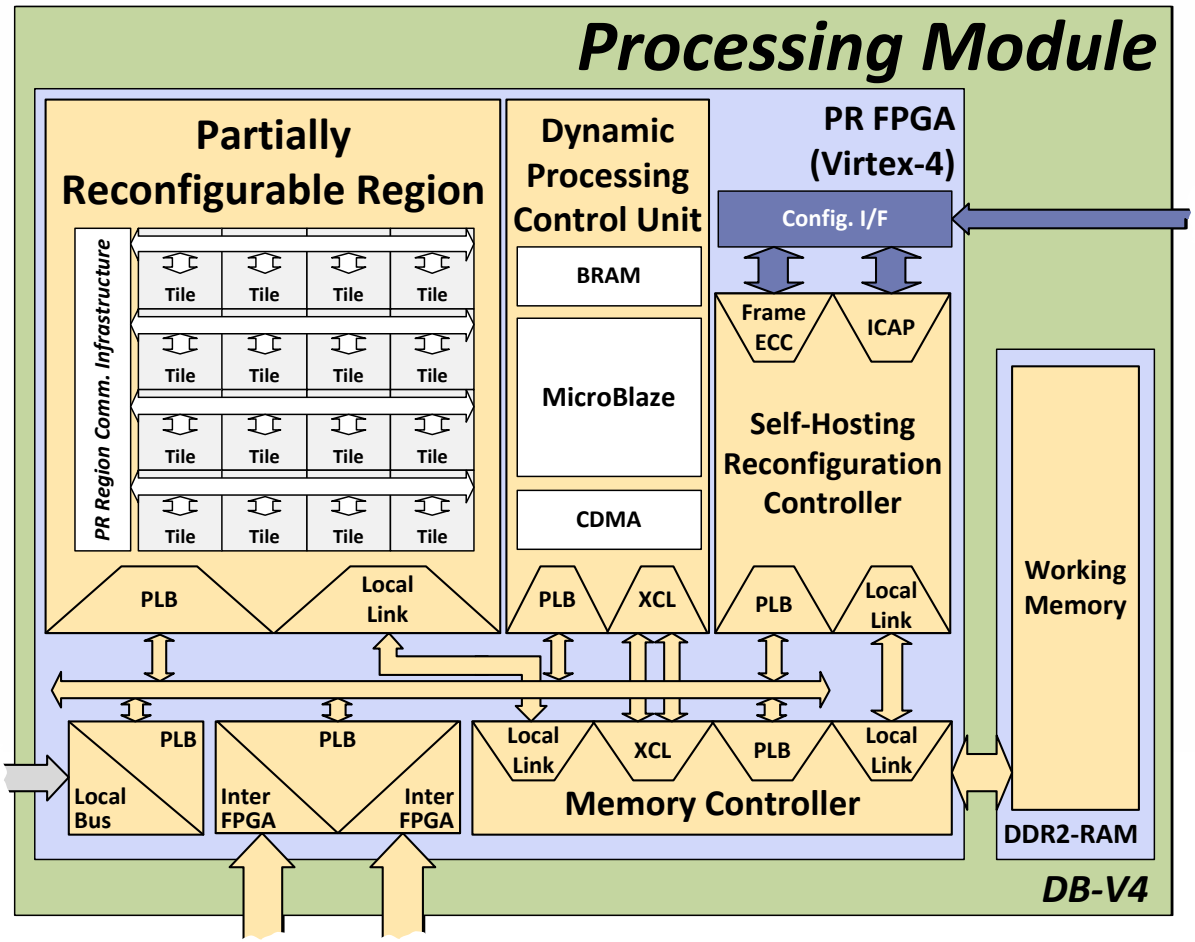
- 4 GByte DDR2 SDRAM
  - Working memory
  - Configuration Cache

FPGA Static Area

- Multi Port Memory Controller
  - 32b data, 7b ECC (BCH 32,7)
  - Integrated ECC statistics unit
  - Integrated fault injection
- Communication
  - PLB based module interconnect
  - Bridge to other modules
  - Monitoring and debug bridge
  - Local Link for streaming data
- Reconfiguration controller
- Dynamic Processing Control Unit

Partially Reconfigurable Region

Processing Module *DB-V4*

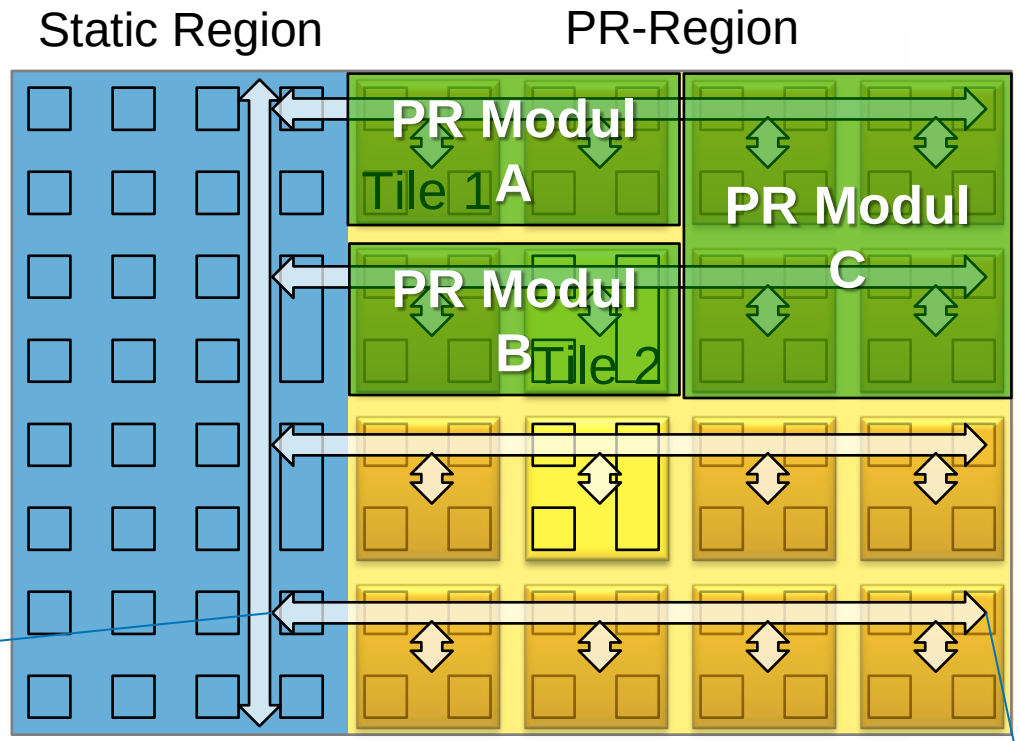


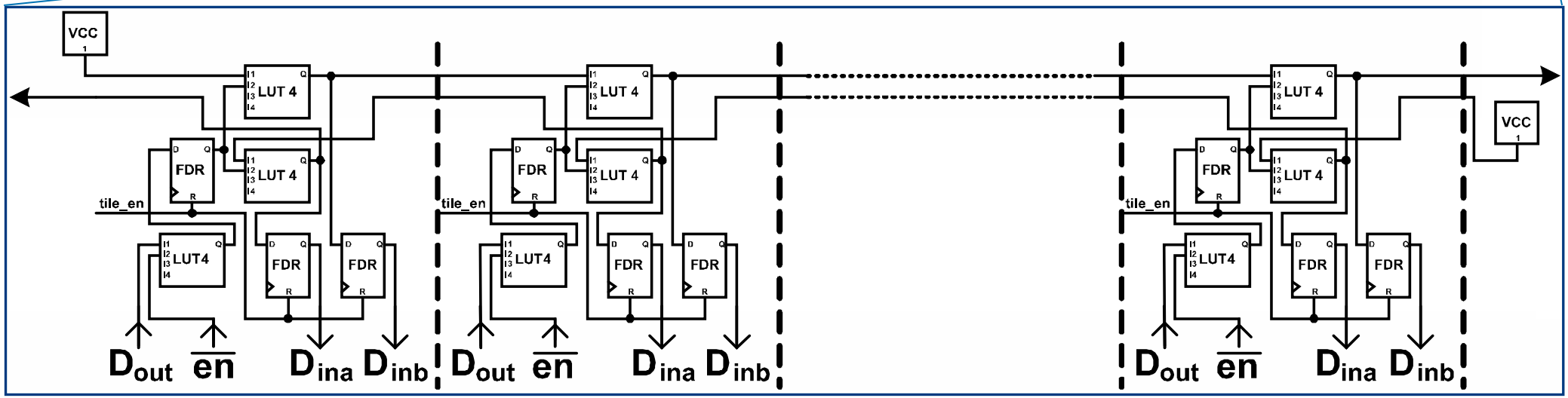
Partially Reconfigurable Region

- Tiled PR-region
  - Flexible module placement
  - PR-modules can be placed at any position within the partially reconfigurable region
- Homogeneous communication infrastructure
  - Integrated address decoder and PR tile management
  - Enables relocation of modules
  - Automatically generated using DHHarMa tool [FCCM 2011]

Processing Module *DB-V4*

- Communication macro must occupy the same resources in every tile
- Homogeneity allows placement of modules at any position with the same type of tiles
- Automatic generation of communication infrastructure based on VHDL specification
- Dedicated placer and router for homogeneous macros up to Xilinx Virtex-7

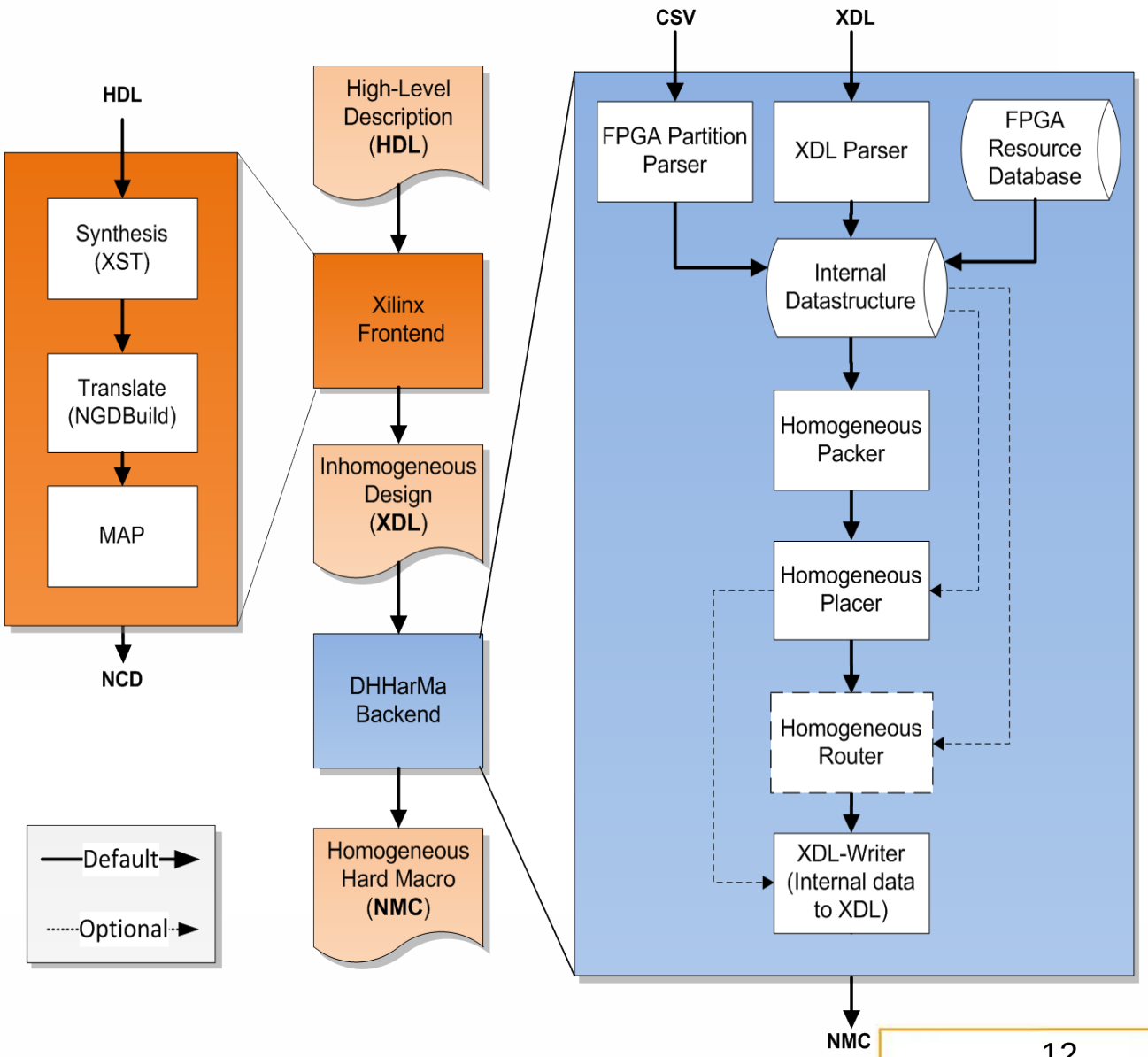




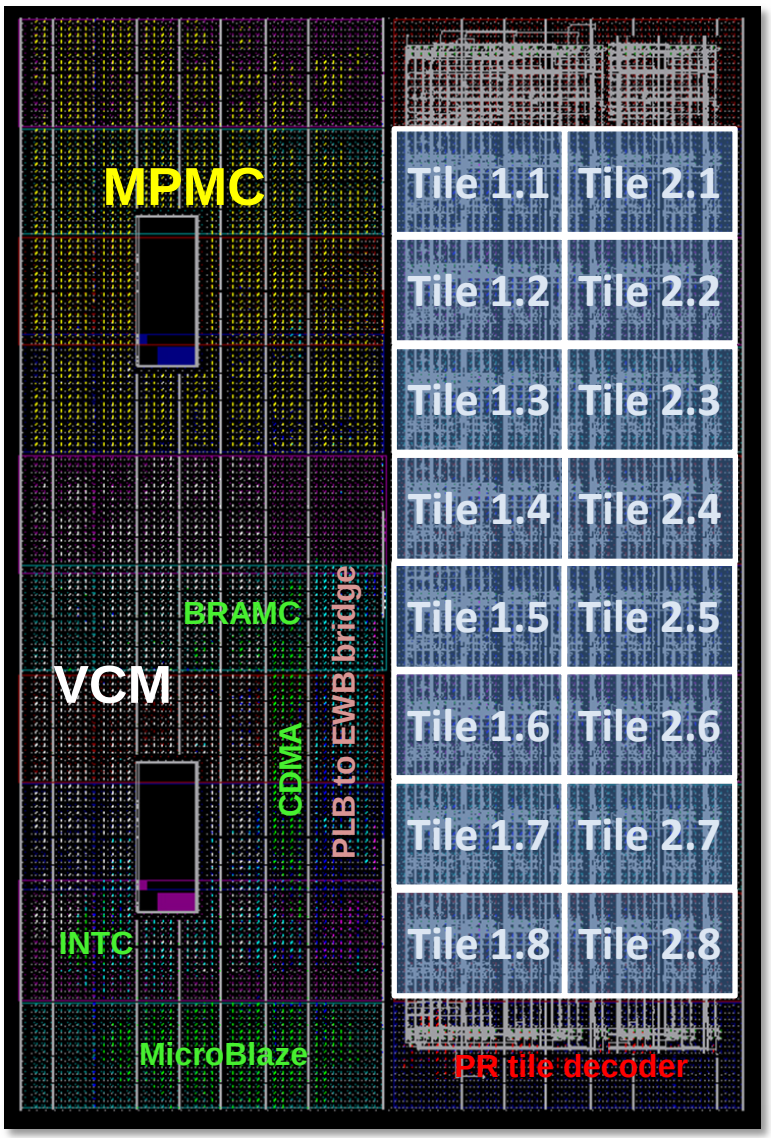
Processing Module *DB-V4*

DHHarMa toolflow overview

- Starting from HDL description
- Based on XDL, using Xilinx tools as Frontend
- Automatic creation of homogeneous structures
- Allows easy modifications
- Allows easy migration to other FPGA(Families)



Processing Module *DB-V4*



Xilinx Virtex-4 FX100

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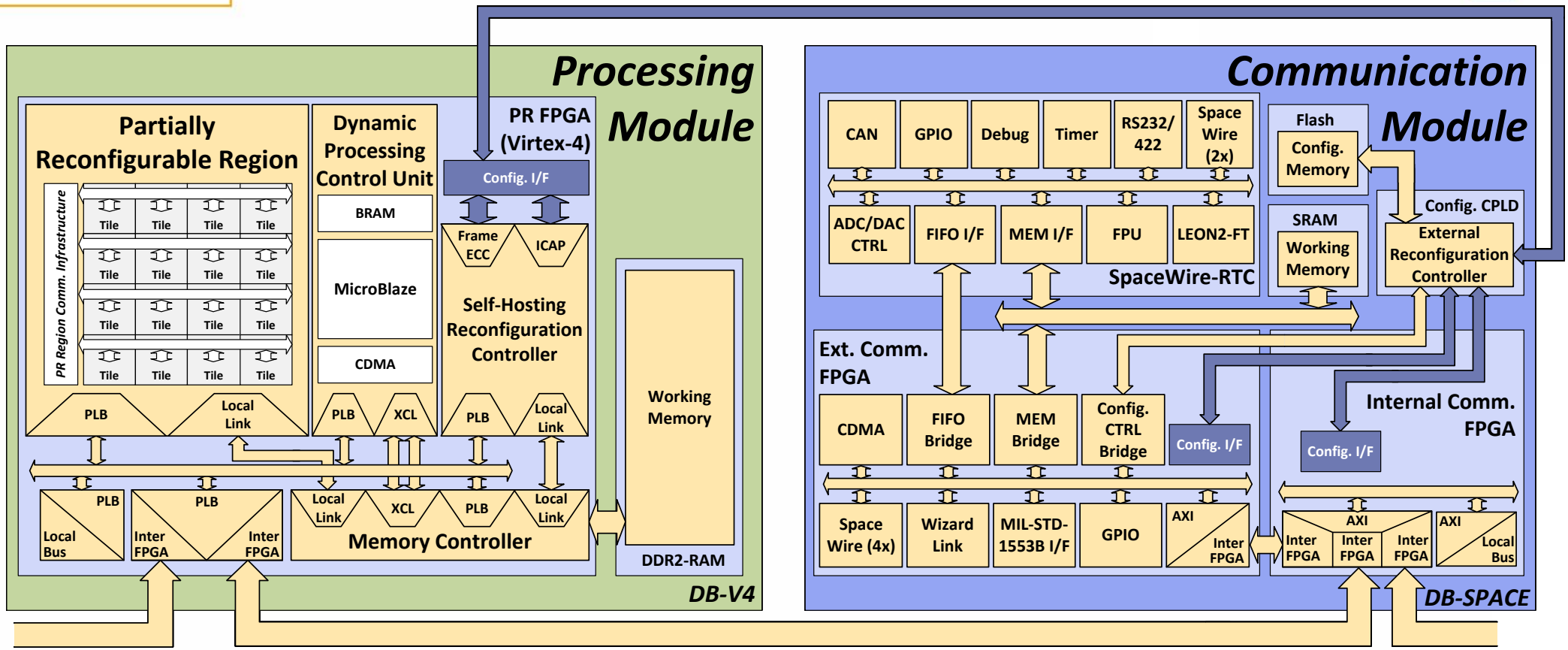
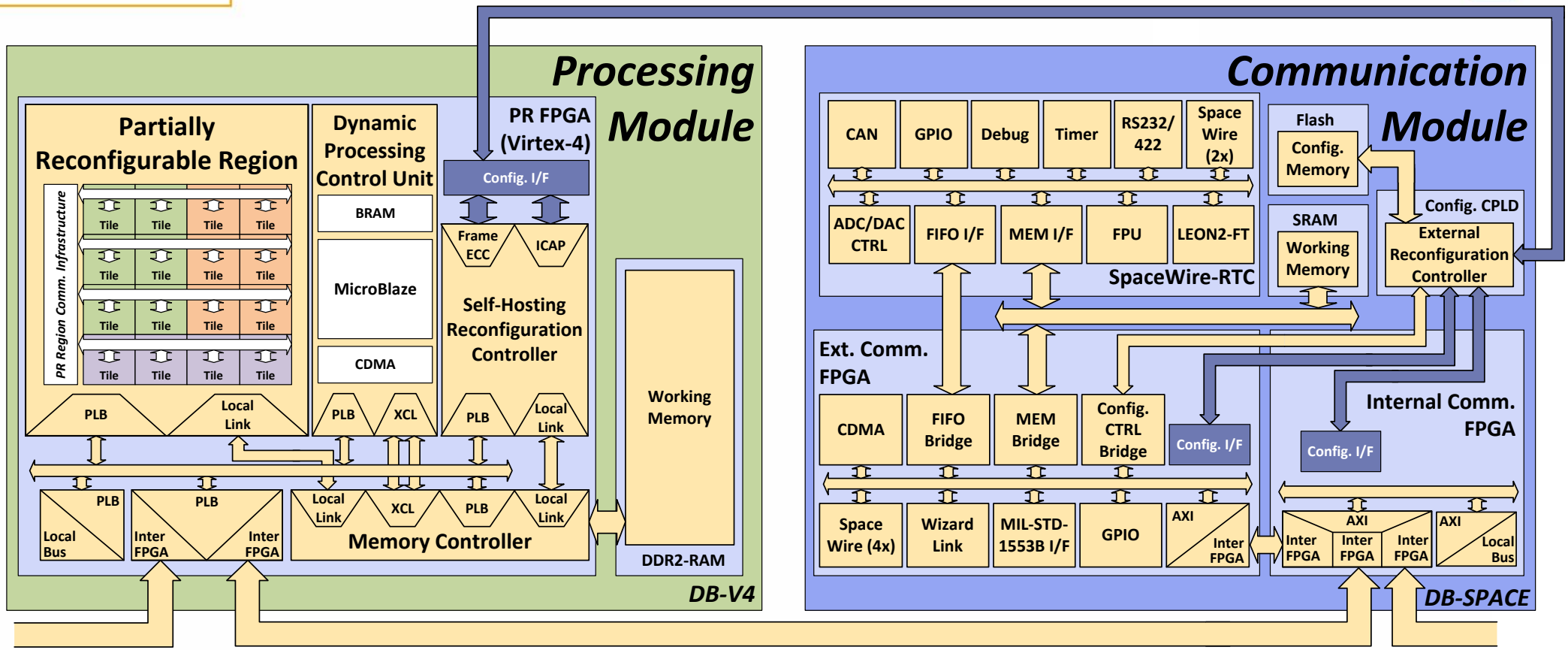
External Reconfiguration Controller



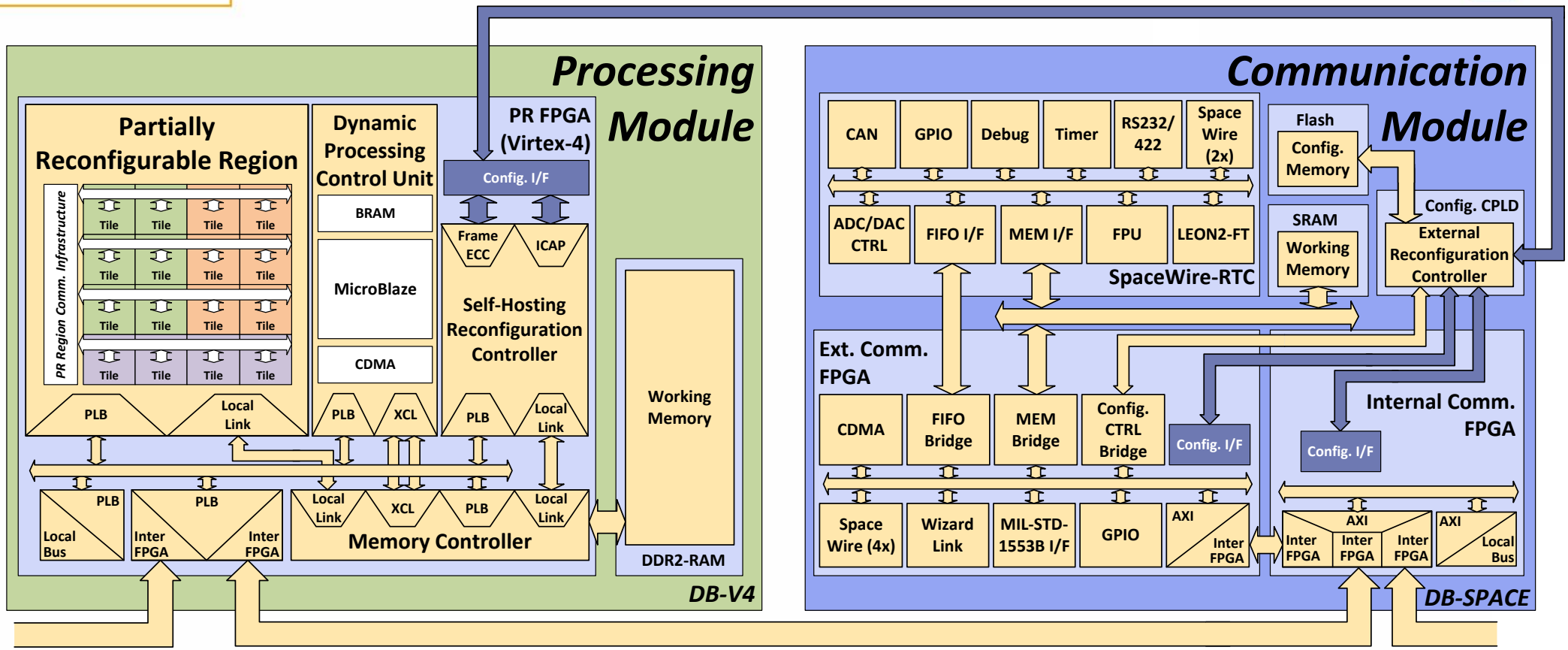
- Initial startup configuration of Communication Module and Processing Modules
  - 128 Mbyte flash memory stores golden copies of all configuration data
- Partial run-time reconfiguration of Processing Modules
  - Accessible via any configured interface, e.g., SpaceWire, MIL-STD-1553B
  - SelectMap reconfiguration with 50 MByte/s
  - Supports blind scrubbing

Self-hosting Reconfiguration



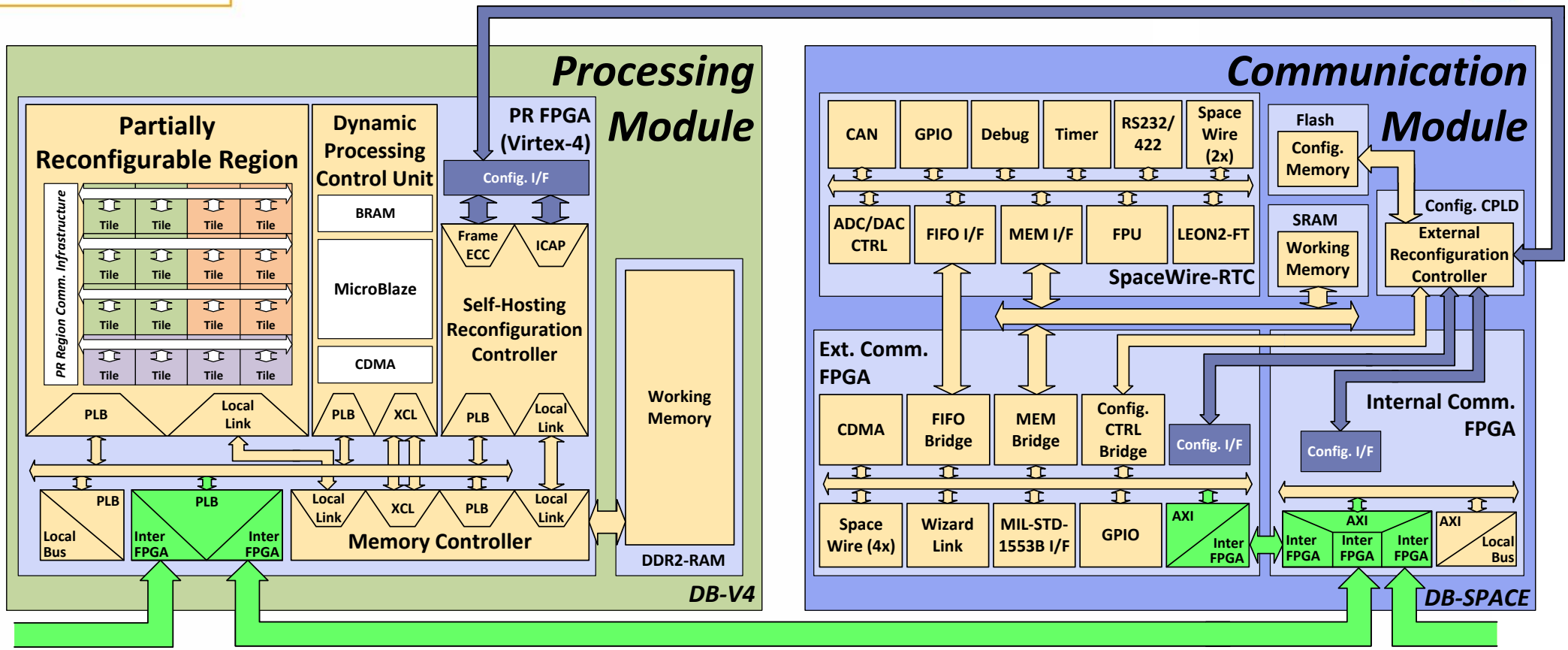
- Partial run-time reconfiguration
  - Controller implemented in the static part of the FPGA
  - DDR2-SDRAM stores configuration data
  - Dynamic Processing Control Unit
    - Maintains the free resources, determines feasible position for new modules
  - Self-hosting Reconfiguration Controller
    - Performs bitstream relocation, transfers bitstream to ICAP

Self-hosting Reconfiguration



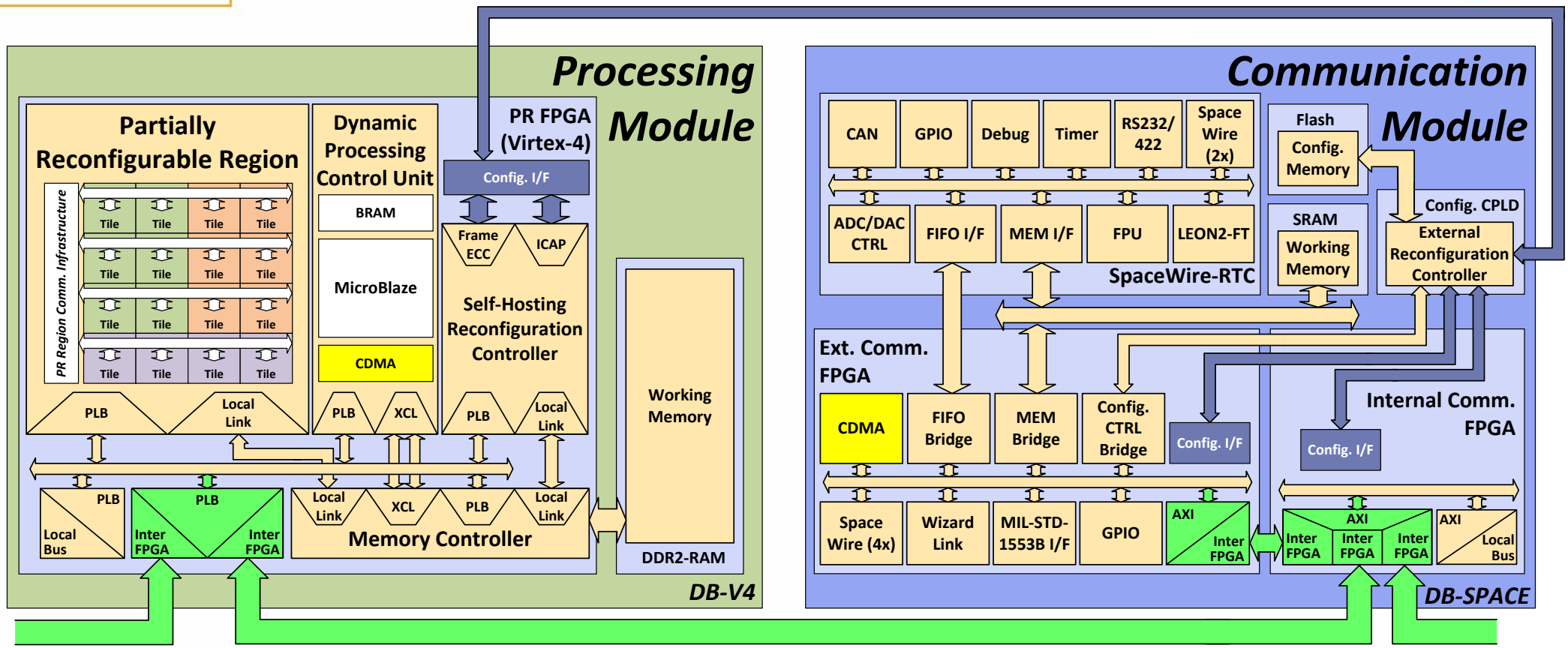
- Partial run-time reconfiguration
  - Reconfiguration is triggered internally or via external interfaces
  - 400 MByte/s reconfiguration bandwidth
  - Readback scrubbing using intrinsic EDAC support of the FPGA
  - Individual scrubbing rates for different FPGA regions
  - Fault injection utilizing partial reconfiguration
  - Monitoring and statistics functions

Communication Infrastructure



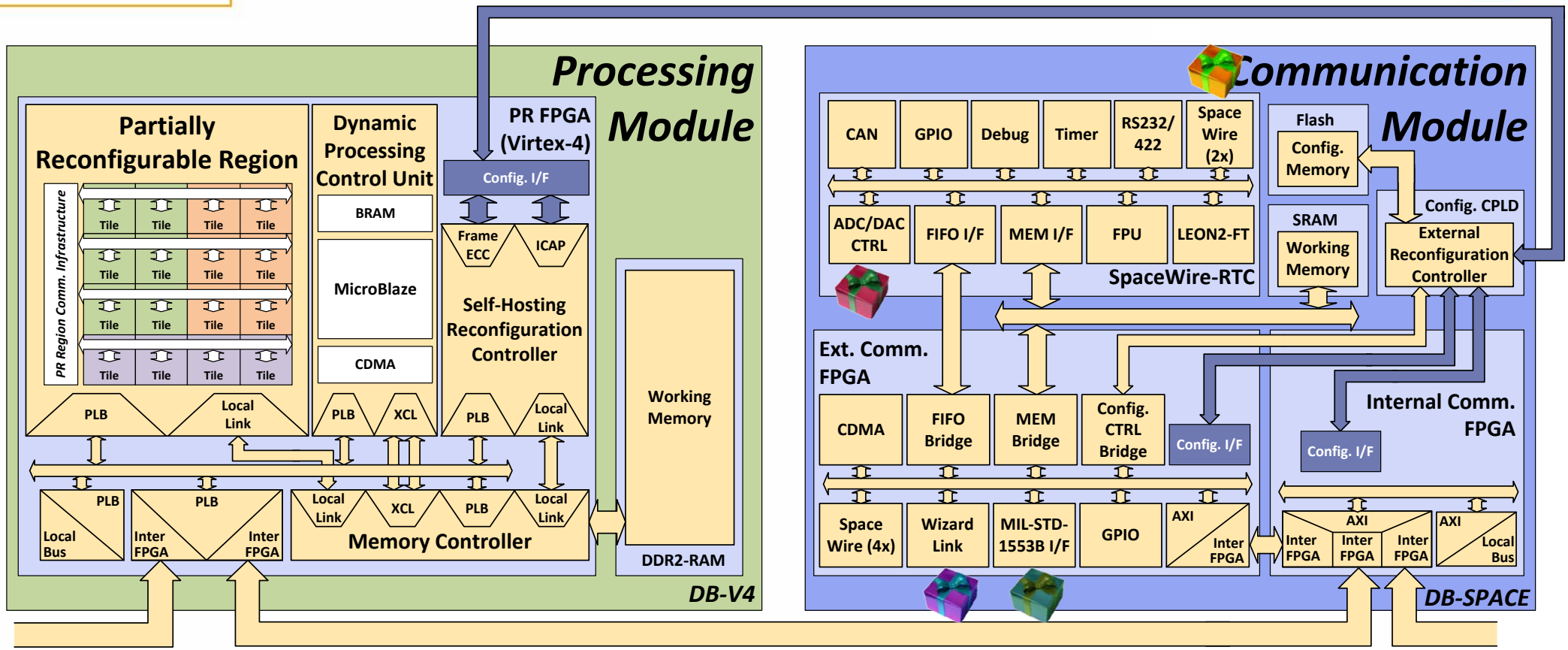
- Inter-FPGA interface for communication between FPGAs
  - Abstracts from physical interface between FPGAs
  - Master/Slave interface to AXI/PLB bus
  - Routing capability for up to four ports (IP core configured at design-time)
  - Integrated packetizer and flow control

Communication Infrastructure



- Inter-FPGA interface for communication between FPGAs
  - DMA unit enables burst transfers
  - RRMU (Resource and Reconfiguration Management Unit) schedules parallel data transmission and controls the involved DMA units

Communication Infrastructure



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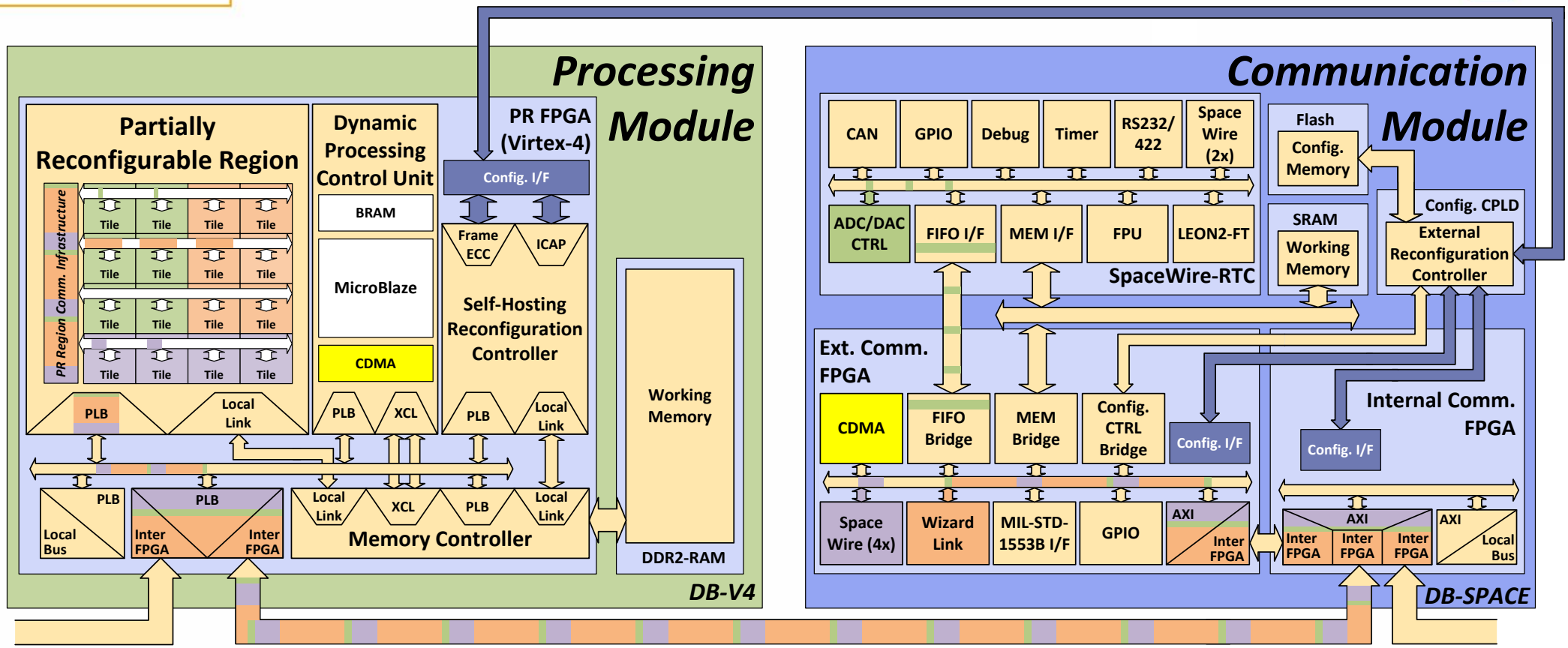

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  - DMA unit enables burst transfers
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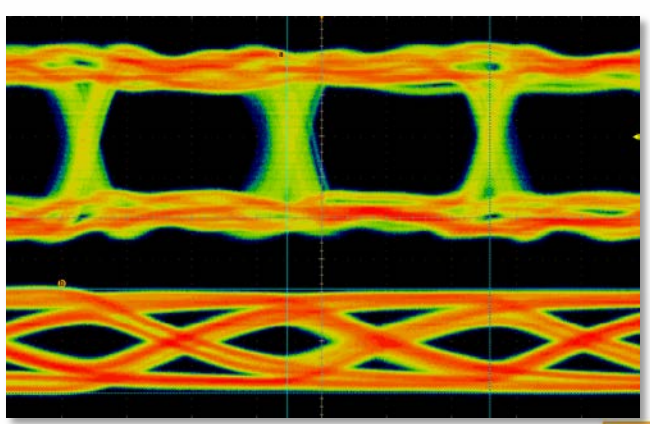
Communication Infrastructure

	Signaling Rate	Effective Bandwidth
SpaceWire-RTC	200 Mbit/s (FD)	160 Mbit/s (FD)
SpaceWire-FPGA	200 Mbit/s (FD)	160 Mbit/s (FD)
WizardLink	2700 Mbit/s (FD)	2100 Mbit/s (FD)
MIL-STD-1553B	1 Mbit/s (HD)	0.7 Mbit/s (HD)
Inter-FPGA	3200 Mbit/s (FD)	3100 Mbit/s (FD)
AMBA AXI4	3200 Mbit/s	3100 Mbit/s
PLB	6400 Mbit/s	6200 Mbit/s

WizardLink IP Core

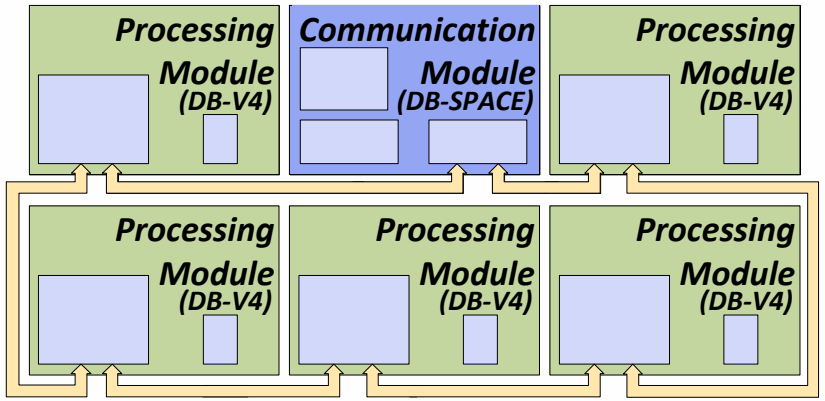
- Integrated scatter gather DMA functionality
- 2.7 Gbit/s (2.1 Gbit/s effective)
- 3m PCIe cable (4.5m chip to chip)
- Next step: Integration of SpaceFibre protocol



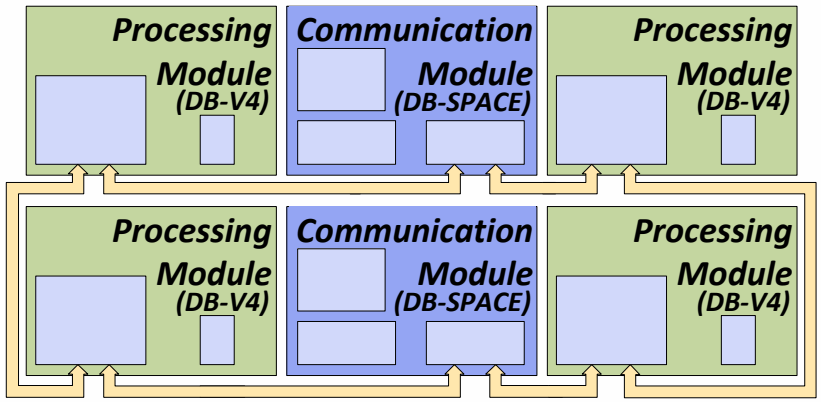
Transmitter

Receiver

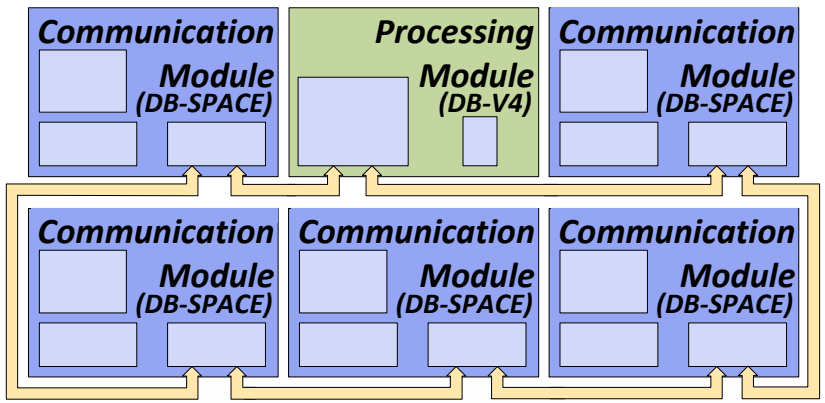
Scalability - Examples



- 6x SpaceWire
- 1x WizardLink, MIL, CAN, ADC/DAC
- 54x GPIO
- 20 GByte DDR2, 1 Gbit Flash
- 5 Xilinx Virtex-4 FX100 FPGAs

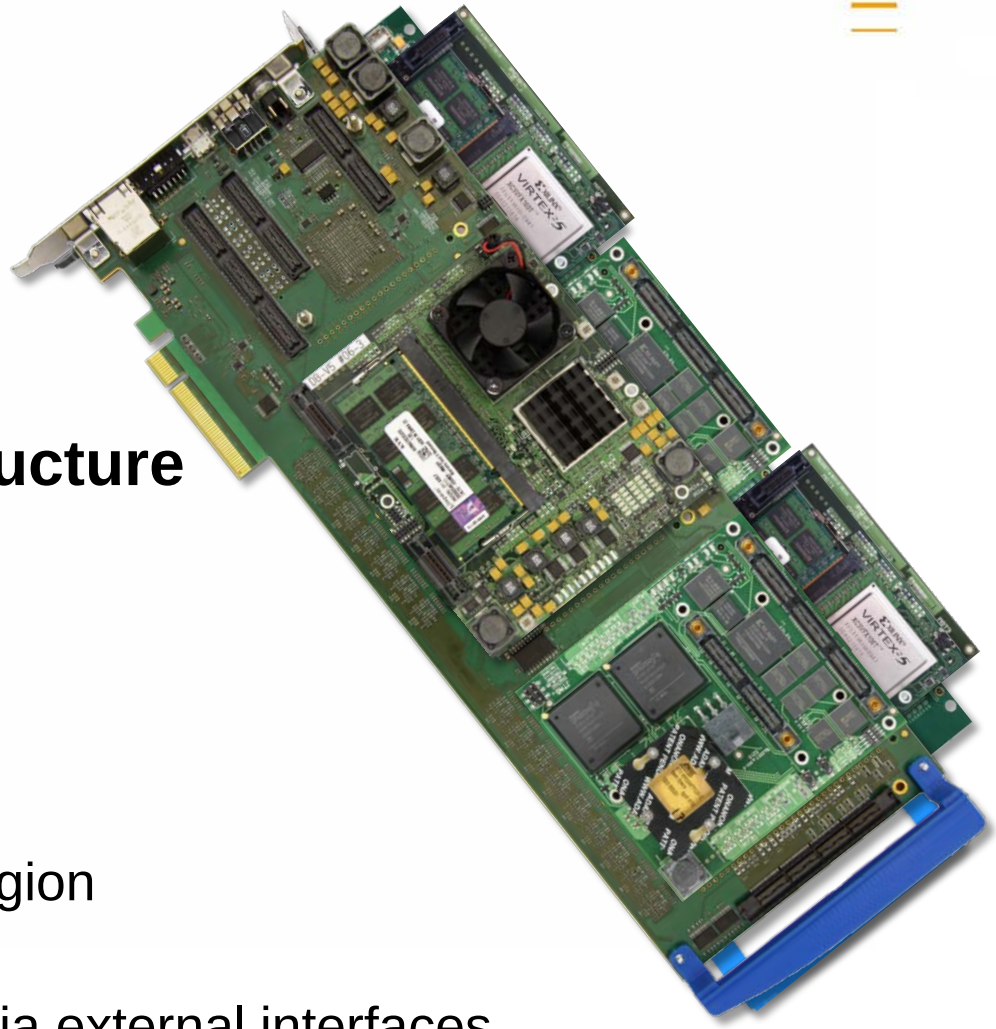


- 12x SpaceWire
- 2x WizardLink, MIL, CAN, ADC/DAC
- 108x GPIO
- 16 GByte DDR2, 2 Gbit Flash
- 4 Xilinx Virtex-4 FX100 FPGAs



- 30x SpaceWire
- 5x WizardLink, MIL, CAN, ADC/DAC
- 270x GPIO
- 4 GByte DDR2, 5 Gbit Flash
- 1 Xilinx Virtex-4 FX100 FPGA

Conclusion



- **Scalable system architecture**
  - Number of FPGAs and Interfaces
  - New FPGAs (Xilinx Virtex-5 FX100T)
  - New host interfaces (PCIe)
- **Powerful communication infrastructure**
  - Reconfigurable at design time
  - AXI/PLB inside FPGAs
  - IP-core for Inter-FPGA communication
- **Partial run-time reconfiguration**
  - Homogeneous communication in PR region
  - 400 MByte/s reconfiguration bandwidth
  - Self-reconfiguration or reconfiguration via external interfaces
  - Adaptive scrubbing with fast scrub rates
- **EDK based design flow**
  - Easy IP-core reuse

Thank you
for your attention!

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