

# Xilinx @ Astrium October 2012

Adam P Taylor CEng FIET

All the space you need



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# Introduction

## Main Experience on the Ukube project

**The main objective of this proposal is to demonstrate the feasibility of Astrium Patent 20090316898:**

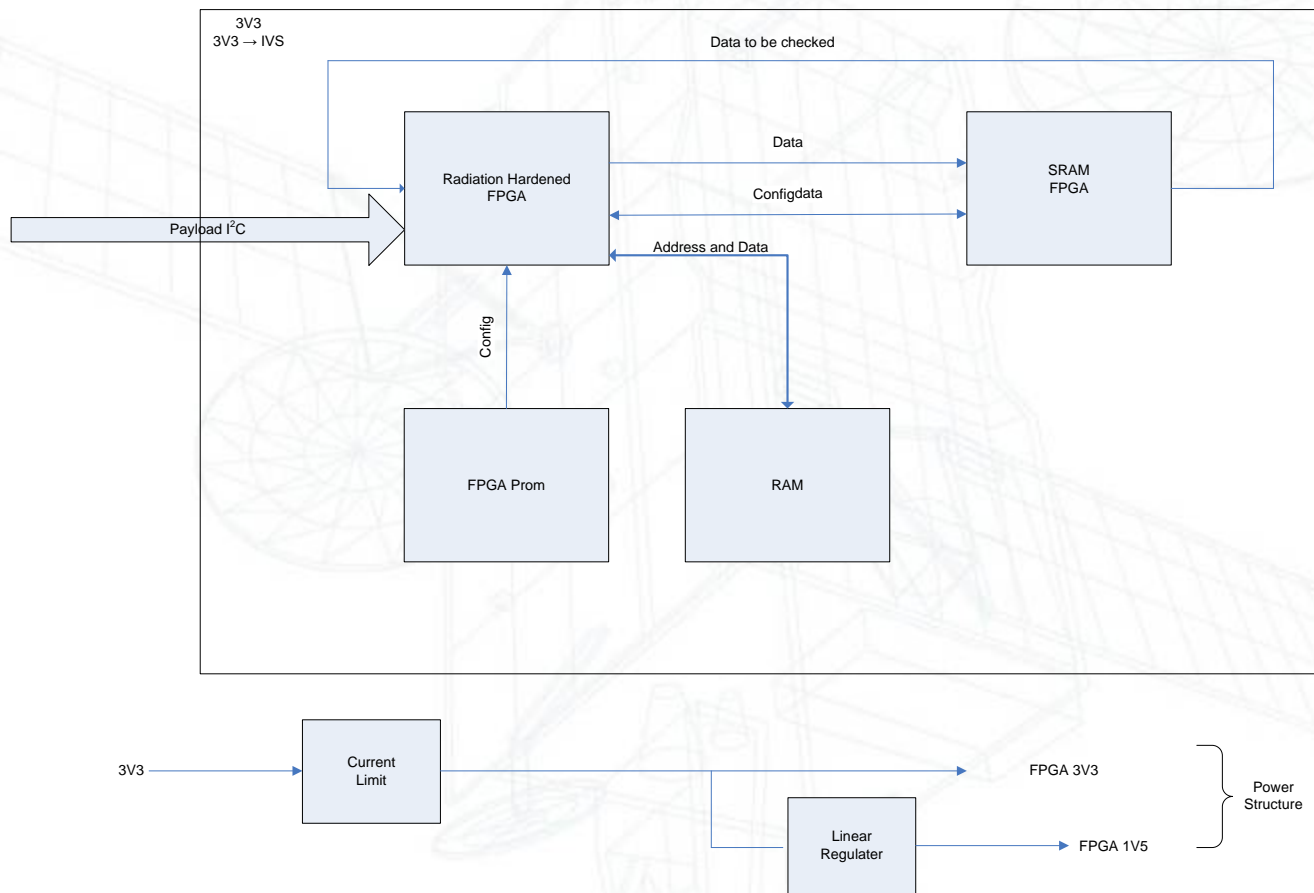
- Random Number Generation in Orbit (Inventors: Dr Omar Eman, Peter Bennie and James Stuart Glanfield)

**Secondary objective to gather statistics on the radiation performance of an SRAM based FPGA**

**Contract Duration: 9 months**

**Launch Date March 2013**

# Architecture

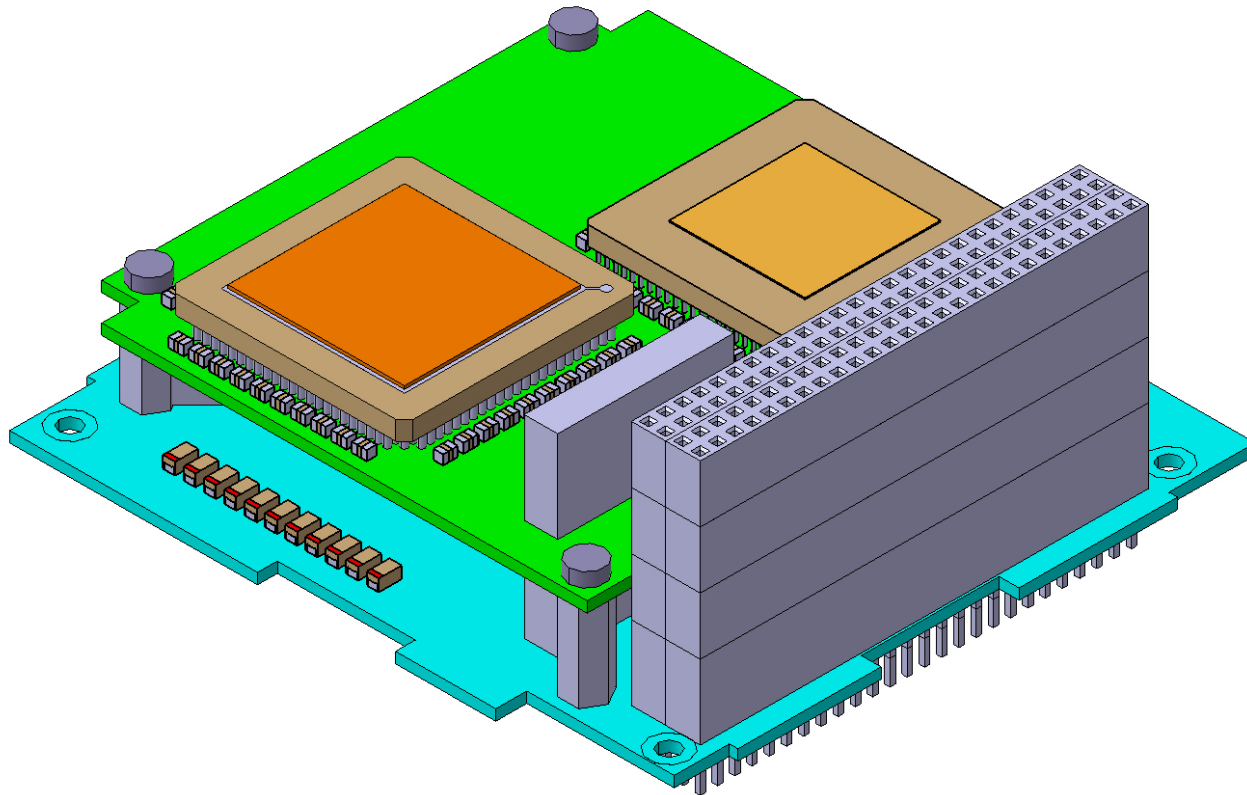


# Interfaces

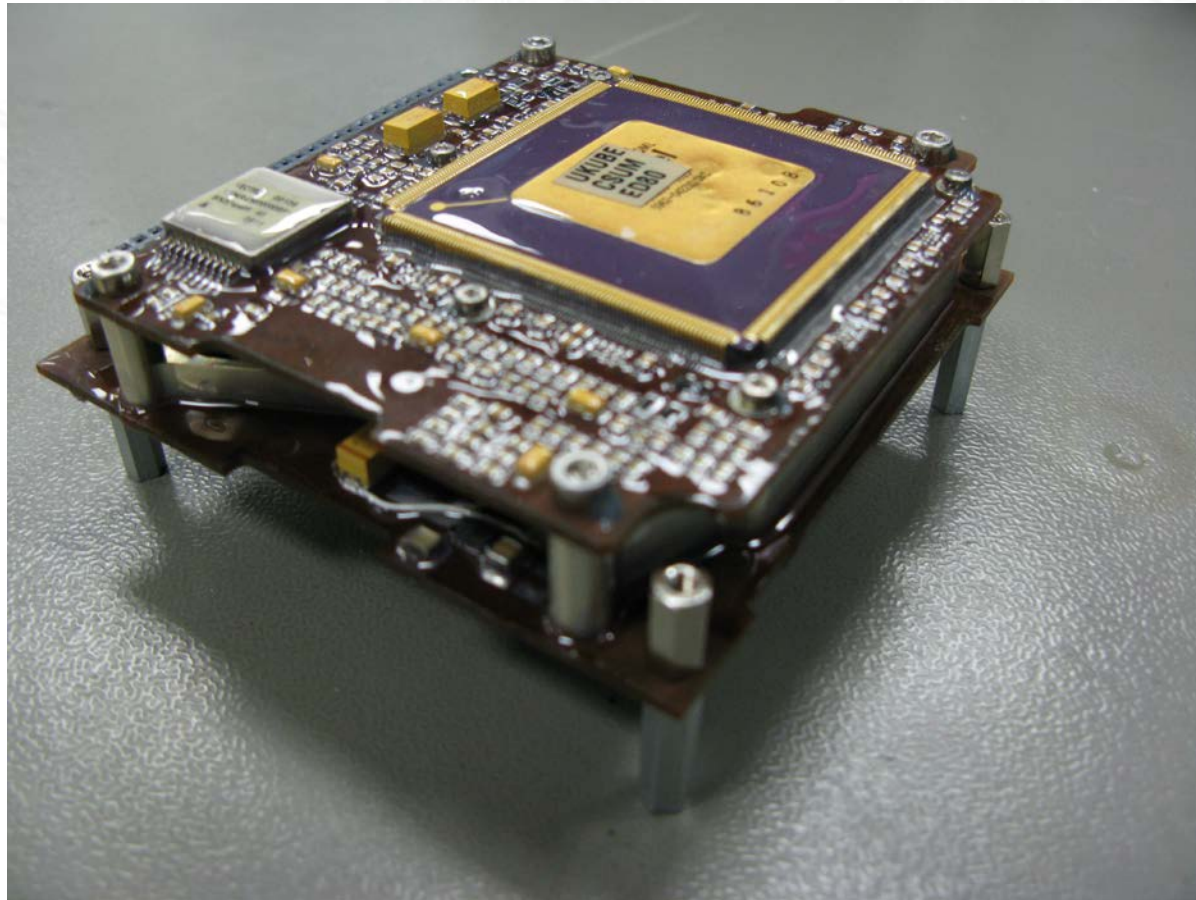
**Very Simple Interface Requirements**  
**I2C bus for control and telemetry gathering**  
**3v3 12v,5v, Supplied from payload**



# 3D Cad Model



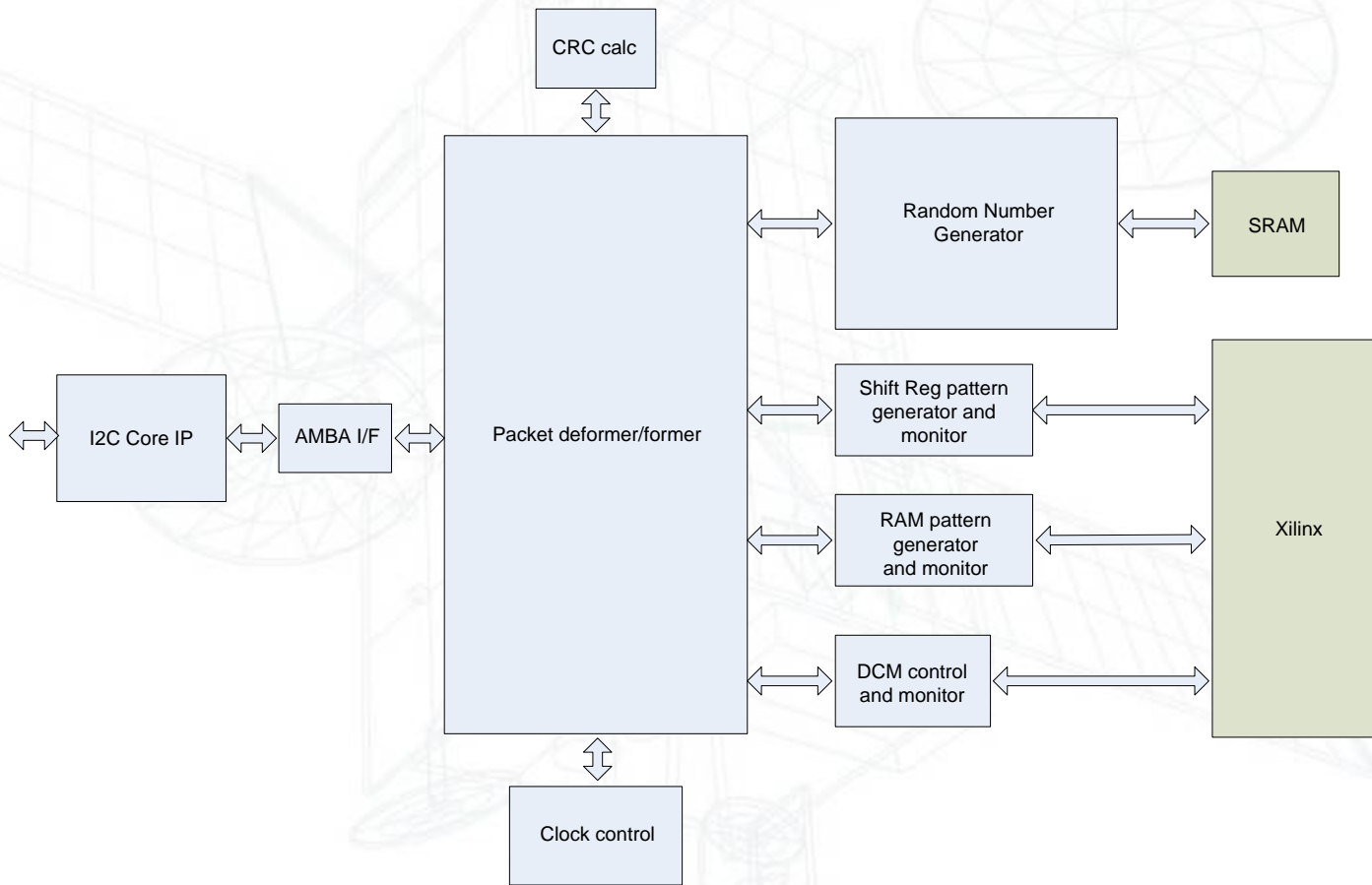
# Reality



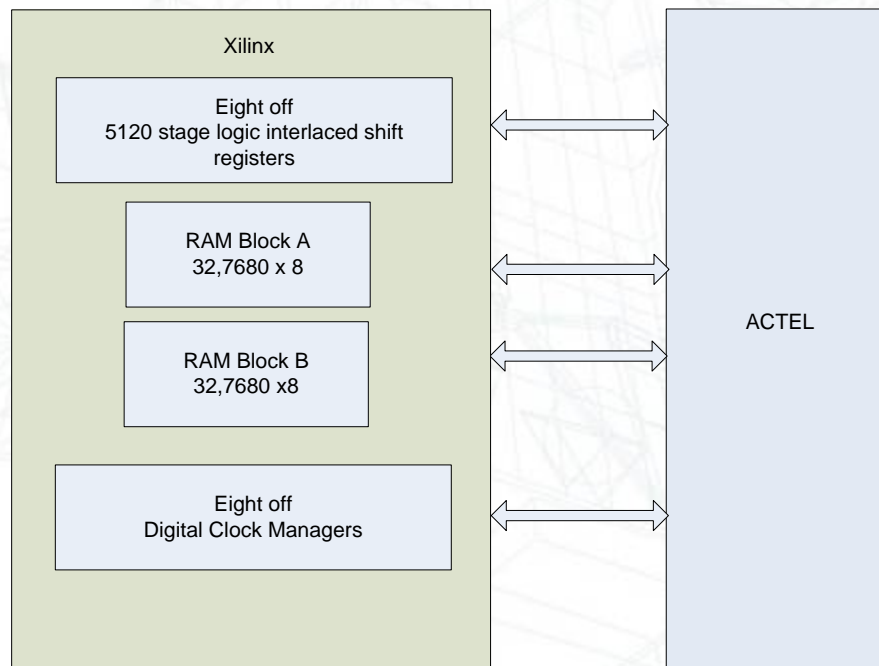
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# Actel FPGA Architecture



# Xilinx FPGA Design - Characteristics





# Challenges of Janus

**Financial and Timescale, much faster and cheaper development than we are used to.**

- Sponsorship from **Invotec** to support mission

**Obtaining the Flight FPGAs in the available budget and desired time scales.**

- Sponsorship from **Xilinx** to support mission

**Power management for the Xilinx FPGA.**

**Ensuring Reliable configuration.**

- Ended up with dual Flash Configuration Proms in hot redundant configuration.

# Benefits Janus Brings

**Ukuba platforms several benefits.**

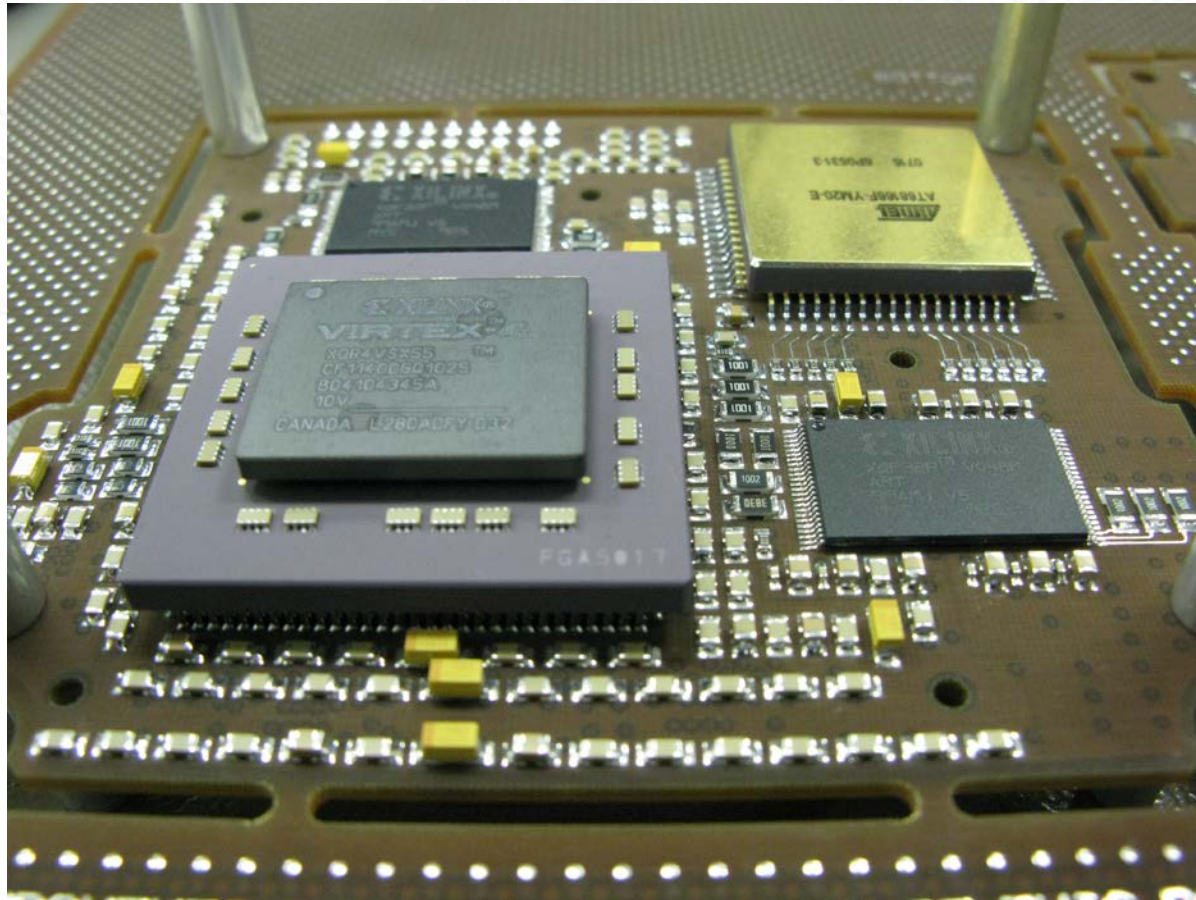
**Demonstration of a patent which could be key for future Secure missions.**

**Heritage for large Xilinx FPGAs and correlation of Xilinx performance against modelling.**

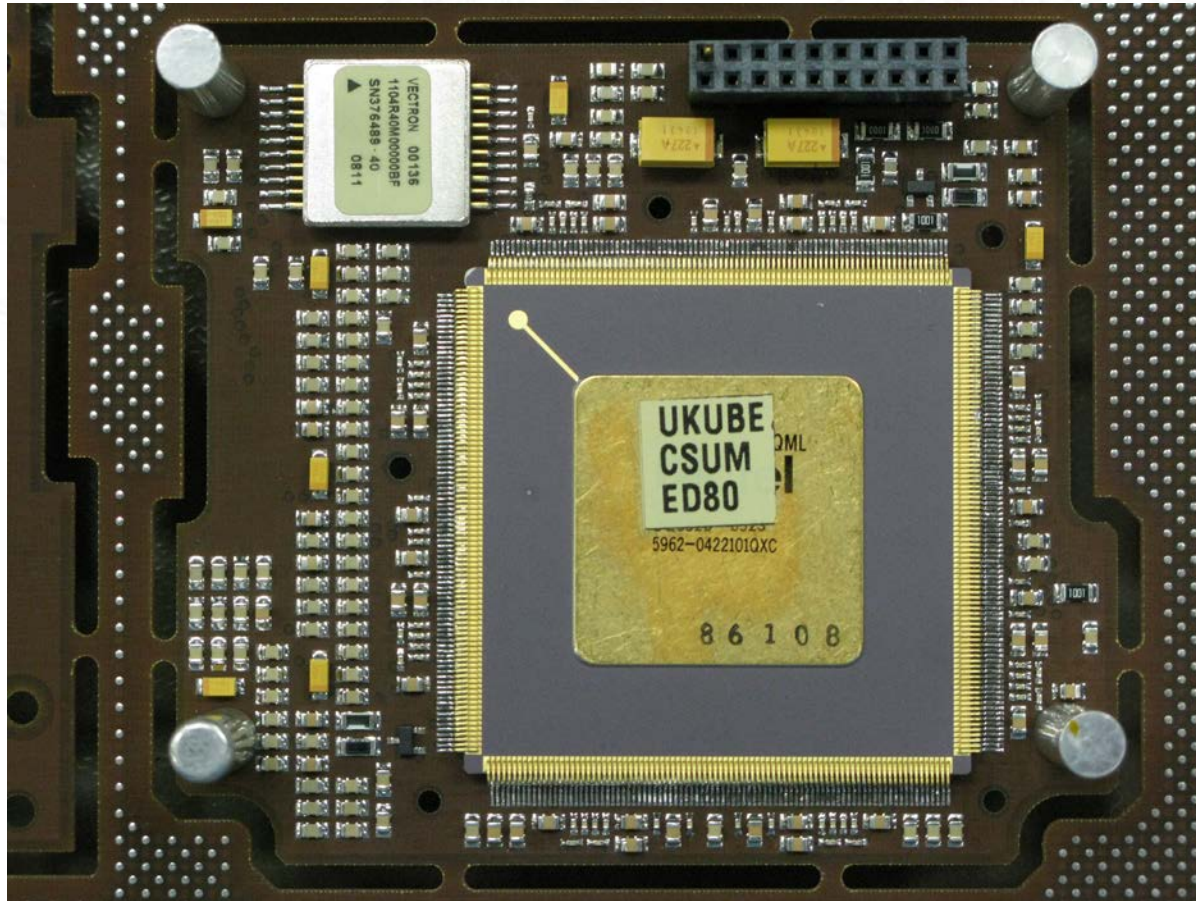
**Experience of smaller nano-satellite requirements and engineering.**

**Benchmarking.**

# Images



# Images



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# Conclusion

**Xilinx as the largest FPGA company has a wide user base and as such issues with tools etc are normally addressed quickly.**

**There is also a wide range of web support available.**

**Power required by the device certainly the Virtex 5 is considerable.**

**Interested to see what effect if any the synthesis power switch has on the V5QV power?**

