FPGAs for Space Applications
Ken O’Neill
Director of Marketing, Space Products
Microsemi SOC Group
Agenda

- RTSX-SU
- RTAX-S
- Life Test Data for Programming Software
- RTAX-DSP
- RT ProASIC 3
- IP for Space Applications
- Next Generation Space-Flight FPGAs
- New Product Concepts
- Space Forum
SEU-Enhanced Flip-Flops

- Foundation for RTSX-SU, RTAX-S/SL and RTAX-DSP FPGAs

**Standard Flip-flop**

- D → Q
- CLKB → CLK

**SEU-Enhanced Flip-flop**

- D → Q
- CLKB → CLK

**Microsemi Advantage**
- 100% gate availability - no gate loss to TMR implementation
- Upsets due to single ion strike voted out by the unaffected latches
- Voting the feedback paths prevents the flip flop from changing state
- Transparent to user, no special skill or knowledge needed

**Voter Gate**
- Two correct inputs outvote single incorrect input
- Self-corrects asynchronously
## Screening Flows for Space-Flight FPGAs

### Screening Process

<table>
<thead>
<tr>
<th>Mil-Std 883 Class B</th>
<th>Extended Flow</th>
<th>QML-V / EV Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Sort</td>
<td>Wafer Sort</td>
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<tr>
<td>Package Assembly (B flow)</td>
<td>Package Assembly (E flow)</td>
<td>Package Assembly (EV flow)</td>
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<tr>
<td>Bond Pull (Extended Pull Test)</td>
<td>Bond Pull (Extended Pull Test)</td>
<td>Bond Pull (Extended Pull Test)</td>
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<td>Internal Visual (Cond. B)</td>
<td>Internal Visual (Cond. A)</td>
<td>Internal Visual (Cond. A)</td>
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<td>Pre-Cap Source Inspection (Cond. A)</td>
<td>Pre-Cap Source Inspection (Cond. A)</td>
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<td>Temperature Cycling (10 Cycles)</td>
<td>Temperature Cycling (10 Cycles)</td>
<td>Temperature Cycling (50 Cycles)</td>
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<tr>
<td>Seal (Fine/Gross Leak Test)</td>
<td>Seal (Fine/Gross Leak Test)</td>
<td>Seal (Fine/Gross Leak Test)</td>
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<tr>
<td>X-Ray</td>
<td>X-Ray</td>
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<td>Binning Circuit</td>
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<td>Comm Temp Test</td>
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<tr>
<td>Pre Read and Record +25C (R&amp;R)</td>
<td>Pre Read and Record Tri-Temp (R&amp;R)</td>
<td>Pre Read and Record Tri-Temp (R&amp;R)</td>
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<tr>
<td>Dynamic Burn-in (160 Hrs @125C)</td>
<td>Dynamic Burn-in (240 Hrs @125C)</td>
<td>Dynamic Burn-in (240 Hrs @125C)</td>
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<tr>
<td>Post-BI-Test +25C</td>
<td>Post-BI-Test +25C with R&amp;R</td>
<td>Post-BI-Test Tri-Temp with R&amp;R</td>
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<tr>
<td>Static Burn-in (144 Hrs @125C)</td>
<td>Static Burn-in (144 Hrs @125C)</td>
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<td>Post-BI Test +25C</td>
<td>Post-BI Test +25C with R&amp;R</td>
<td>Post-BI Test +25C with R&amp;R</td>
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<td>Final Test +125C with R&amp;R</td>
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<td>Seal (Fine/Gross Leak Test)</td>
<td>Seal (Fine/Gross Leak Test)</td>
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<td>Speed Grade Test (RTAX only)</td>
<td>Speed Grade Test (RTAX only)</td>
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<td>100% QA Electrical +25C</td>
<td>100% QA Electrical +25C</td>
<td>100% QA Electrical +25C</td>
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<td>Visual Inspection</td>
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### Lot Acceptance Tests

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<tr>
<th>Generic Group B</th>
<th>Lot Specific Group B with RGA</th>
<th>Lot Specific Group B with RGA</th>
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<tr>
<td>Generic Group C</td>
<td>Generic Group C</td>
<td>Wafer Lot Specific Group C (2000 Hrs HTOL)</td>
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<td>Generic Radiation Total Dose Report</td>
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<td></td>
<td></td>
<td>Lot Specific DPA (per Date Code)</td>
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</table>

RTSX-SU Family

- **RTSX-SU Features**
  - Designed specifically for Space Applications
  - Up to 2,012 SEU Hardened Flip-Flops eliminate user-designed TMR
  - Single Event Latch-up Immune
  - Supports Hot-Swapping and Cold Sparing
  - Configurable I/O support multiple 5.0V and 3.3V I/O standards
  - Pin Compatible with commercial SX-A devices for easy prototyping
  - Antifuse secure programmable technology

- **QML Certified Devices**
  - QML Class Q available today
    - Mil Std 883 Class B
    - Microsemi Extended flow
  - “EV” flow available today
    - All process steps of QML-V
    - 300°C bake with sample destructive pull at wire-bond set-up (bimetalic wire bonding)
    - 40-week lead time applies (2000 Hr Group C)

<table>
<thead>
<tr>
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<th>RTSX32SU</th>
<th>RTSX72SU</th>
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<tr>
<td>Dedicated Registers</td>
<td>1,080</td>
<td>2,012</td>
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<tr>
<td>Maximum I/Os</td>
<td>227</td>
<td>360</td>
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<td>Packages</td>
<td>CQFP-84</td>
<td>CQFP-208</td>
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<td>CQFP-208</td>
<td>CQFP-256</td>
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<td>CQFP-256</td>
<td>CCLG-256</td>
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<td>Manufacturing Flows</td>
<td>883B</td>
<td>E-Flow</td>
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<td></td>
<td>EV-Flow</td>
<td>EV-Flow</td>
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Latest Packaging for RTSX-SU

- **84-pin Ceramic Quad Flat Pack**
  - A54SX32A-CQ84, RTSX32SU-CQ84
  - Smaller footprint than 208-CQFP
    - 273 vs 853 mm², 68% saving
  - Lower mass than 208-CQFP
    - 2.2g vs 8.8g, 75% saving

- **256-pin Ceramic Chip-Carrier Land Grid array (CCLG)**
  - Integrate programmed and tested FPGAs into Multi-Chip Modules (MCMs)
  - Small package size (17mm x 17mm) fits inside MCM
  - Hermetically sealed, offered with RTSX32SU
  - Uses standard Actel programming hardware

Bond pads on top surface bond FPGA to other components inside MCM

Land grid array underside for testing and programming. Mount on MCM substrate using thermally conductive, electrically non-conductive adhesive
## Success in Space – RTSX-SU

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<thead>
<tr>
<th>Project</th>
<th>Launch Date</th>
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<tr>
<td>Mars Reconnaissance Orbiter</td>
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<tr>
<td>GPS 2R-M (8 Satellites)</td>
<td>Sept 2005 to Aug 2009</td>
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<tr>
<td>SAR-Lupe 1, 2, 3, 4 and 5</td>
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<td>TerraSar X</td>
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<td>Operational Responsive Space - 1</td>
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<td>Mars Science Lab</td>
<td>Nov 2011</td>
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RTAX-S/SL
Designed for Space
Radiation-tolerant FPGA alternative to RH ASICs
- Ten times larger than previous largest space FPGA
  - Up to 4M system gates – approximately 500,000 ASIC gates
- Designed for space — Single Event Upset (SEU) enhancements
- 0.15µm, 7-layer metal CMOS with Antifuse, manufactured at UMC
- Embedded block RAM
- Multiple Flexible I/O standards
- Live at Power-up (LAPU)
- Single chip
- Low power consumption
## RTAX-S/SL FPGA Family

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<td>10,752</td>
<td>20,160</td>
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<td><strong>I/O Registers</strong></td>
<td>744</td>
<td>1,548</td>
<td>2,052</td>
<td>2,520</td>
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<td><strong>Total Modules</strong></td>
<td>4,224</td>
<td>18,144</td>
<td>32,256</td>
<td>60,480</td>
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<td><strong>RAM Blocks</strong></td>
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<td>36</td>
<td>64</td>
<td>120</td>
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<td><strong>Total RAM Bits</strong></td>
<td>54K</td>
<td>162K</td>
<td>288K</td>
<td>540K</td>
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<tr>
<td><strong>Max User IO’s</strong></td>
<td>248</td>
<td>516</td>
<td>684</td>
<td>840</td>
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<td><strong>Packages</strong></td>
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<tr>
<td>CQFP</td>
<td>208, 352</td>
<td>352</td>
<td>256, 352</td>
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<td>CCGA/LGA</td>
<td>624</td>
<td>624</td>
<td>624, 1152</td>
<td>1272</td>
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<td><strong>Status</strong></td>
<td>QML Class Q and QML Class V Qualified Silicon Now Shipping</td>
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</table>

- Typical lead times:
  - 18 weeks B-flow, 50 units, CQFP or LGA packaging
  - 24 weeks E-flow, 50 units, CQFP or LGA packaging
  - 40 weeks QML Class V, 20 units, CQFP or LGA packaging (includes 2000 Hr Group C life test)
  - CCGA takes 8 to 10 weeks longer to process for B-flow and E-flow
  - Preparation of export documentation may add additional lead time
RTAX-SL Low Power Family

- Reduced stand-by current
- New part numbers
  - SMDs have been updated with new part numbers
  - Power calculator available for all families
- Stand-by current spec
  - Reduced by 70% to 80% relative to standard RTAX-S (worst case conditions)
    - For example RTAX2000SL spec is 150mA at 125°C
  - Dynamic current spec is unchanged
  - Device timing is unchanged
- Schedule
  - Open for orders NOW
    - Usual lead times will apply
RTAX-S/SL Radiation Data

- **Single-event Latch-up (SEL)**
  - Testing performed up to LET 117 MeV-cm²/mg (125°C)
  - No SEL observed; No control logic upset observed

- **R-Cell Single-event Upset (SEU)**
  - LET_{TH} in excess of 37 MeV-cm²/mg
  - Cross-section < 1E⁻⁹ cm²
  - SEU per R-Cell < 4E⁻¹¹ Errors/bit-day (worst case GEO)

- **Memory SEU**
  - SEU < 1E⁻¹⁰ upsets/bit-day (worst case GEO)
    - EDAC operational, background scrubbing at 2MHz

- **Single-event Transient (SET)**
  - High frequency testing analysis reported at Space Forum www.actel.com/asf

- **Total Ionizing Dose (TID)**
  - Results indicate suitability for vast majority of space missions
    - Stays within parametric limits beyond 200Krads (si)
    - No functional failure up to 300Krads (si)
  - TID performed on each production wafer lot

Complete Development Solutions

**Microsemi RTAX-S Prototyping Solutions**

- Reprogrammable Solution Using APA/A3P with ALDEC Adapter
- Sockets and Adapter Sockets for using Commercial Devices
- Prototype Using Commercial AX Product in Ceramic Package
- RTAX-S Proto Units – Mil Temp Tested, No 883B Processing
- RTAX-S Production Units – QML Class Q or Class V

**Typical Design Phases**

- Phase 1: Concept Validation
- Phase 2: Demonstration Hardware
- Phase 3: Test Hardware using flight boards
- Phase 4: Final Flight Hardware

RTAX-S/SL Qualification, Reliability and Flight Heritage
RTAX-S/SL Reliability and Qualification Status

- QML Class V qualification granted November 2011
  - RTAX4000S/SL qualified
  - No plans to discontinue QML-Q (B-flow, E-flow) now that QML-V is available

- Aerospace Corporation (AX2000, I-temp)
  - Identical antifuses, processing, programming to RTAX2000S
  - Longest runners > 38,000 hours HTOL
  - > 26 Million device hours accumulated!
  - One time-zero SRAM failure
    - Would have been detected by 883B screening
  - Testing complete, no antifuse anomalies observed

- NASA GSFC (RTAX-S)
  - Testing completed, no anomalies observed

- Microsemi (RTAX-S)
  - Multiple life tests up to 6,000 hours
  - No antifuse failures observed
  - Overall product FIT rate calculated < 10 FIT (60% confidence level, EA = 0.7eV)

<table>
<thead>
<tr>
<th>Type</th>
<th>Devices</th>
<th>Dev. Hrs</th>
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<tbody>
<tr>
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<td>277</td>
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<td>10,894,309</td>
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<td>AX2000</td>
<td>LTOL</td>
<td>272</td>
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<td>AX2000</td>
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<tr>
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<td>246,000</td>
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<tr>
<td>RTAX250S</td>
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<td>RTAX2000S</td>
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<td>RTAX2000S</td>
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<td><strong>984,000</strong></td>
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RTAX-S Now in Space!

**Cosmo-SkyMed**
1, 2, 3 and 4
First Launch
June 2007
- RTAX2000S-CQ352

**Mars Phoenix**
Launched
August 2007
- RTAX1000S-CQ352

**Chandrayaan-1**
Launched
October 2008
- RTAX2000S-CQ352

**SDS-1**
Launched
January 2009
- RTAX2000S-CQ352

**GOSAT (IBUKI)**
Launched
January 2009
- RTAX2000S-CQ352

**WINDS (KIZUNA)**
Launched
February 2009
- RTAX2000S-CQ352

**Sicral-1B**
Launched
April 2009
- RTAX2000S-CQ352

**LRO & LCROSS**
Launched
June 2009
- RTAX2000S-CG624 (BAE)
- RTAX2000S-CQ352
- RTAX250S-CQ208

RTAX-S Now in Space!

**IRIS**
Launched November 2009

- RTAX1000S-CGS624 ($6\Sigma$)
- RTAX2000S-CGS624 ($6\Sigma$)

**Cryosat 2**
Launched April 2010

- RTAX2000S-CQ256

**Advanced EHF**
August 2010

- RTAX2000S-CQ352

**QZSS Michibiki**
Launches September 2010

- RTAX2000S-CQ352

**CHIRP**
Launched Sept 2011

- RTAX4000S-CQ352
- RTAX2000S-CG1152
- RTAX1000S-CQ352
- RTAX250S-CQ208

**Mars Science Lab “Curiosity”**
Launched November 2011

- RTAX2000S-CG624 ($6\Sigma$)

**MUOS**
Launched February 2012

- RTAX2000S-CG624 (BAE)

**Radiation Belt Storm Probes (RBSP)**
Launched August 2012

- RTAX1000S-CQ352
- RTAX2000S-CQ352

Planning to Fly RTAX-S

- Sentinel 2: CG624
- KompSat 3: CG624
- ExoMars: CQ208 CQ256
- GOES-R: CQ208 CQ352 CG624 - BAE
- Radarsat Constellation Mission: CQ352
- Magneto-spheric MultiScale: CQ208 CQ352 CG624 - 6Σ
- Galileo: CQ352
- Bepi Colombo: CQ208 CQ256 CQ352
- Gaia: CG624 - 6Σ CG1152 - 6Σ
- James Webb Space Telescope: CQ352
- GPS-III: CQ208 CQ256 CQ352 CG624 - 6Σ
- Iridium Next: CQ208 CQ352

Life Test History of Programming Software
Overall Accumulation of Life Test Data

- Test data accumulated over many RT FPGA products
  - Customer life tests performed by Microsemi
  - Enhanced Lot Acceptance Testing (ELA)
  - Product Qualification testing
- Microsemi recommends using the most recent software version

### 12 Most Recent Releases

<table>
<thead>
<tr>
<th>Silicon Sculptor Software Version</th>
<th>Device-Hours</th>
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<tbody>
<tr>
<td>V5.22.0</td>
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<tr>
<td>V5.18.1</td>
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<td>V5.18.0</td>
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<td>V5.14.1</td>
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<td>V5.12.1</td>
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<td>V5.12.0</td>
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<td>V5.10.1</td>
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<td>V5.8.1</td>
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<td>V5.6.0</td>
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<td>V5.4.1</td>
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<td>V5.2.0</td>
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<td>V4.80.0</td>
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### Top 12 by Device-Hours

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## Prog Software Life Test by Product – RTSX-SU

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<td>V5.2.0</td>
<td>16,800</td>
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<td>33,600</td>
</tr>
<tr>
<td>V5.18.1</td>
<td>2,856</td>
</tr>
<tr>
<td>V5.2.0</td>
<td>64,800</td>
</tr>
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<td>V5.22.0</td>
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<tr>
<td>V5.4.1</td>
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<tr>
<td>Grand Total</td>
<td>199,656</td>
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</table>
## Prog Software Life Test by Product – RTAX-S

<table>
<thead>
<tr>
<th>Device</th>
<th>Device-Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTAX250S</td>
<td>205,400</td>
</tr>
<tr>
<td>V3.89</td>
<td>24,800</td>
</tr>
<tr>
<td>V3.93</td>
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<td>V4.64.0</td>
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<tr>
<td>V4.70.1</td>
<td>5,000</td>
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<td>V4.80.0</td>
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<td>V5.12.0</td>
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<table>
<thead>
<tr>
<th>Device</th>
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<td>129,640</td>
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<tr>
<td>V3.93</td>
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<tr>
<td>V4.64.0</td>
<td>16,800</td>
</tr>
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<td>V4.70.0</td>
<td>129,640</td>
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<tr>
<td>V4.80.0</td>
<td>32,000</td>
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<tr>
<td>V4.80.0</td>
<td>32,000</td>
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<tr>
<td>V4.80.0</td>
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<td>V4.80.0</td>
<td>32,000</td>
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<td><strong>Grand Total</strong></td>
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<table>
<thead>
<tr>
<th>Device</th>
<th>Device-Hours</th>
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</thead>
<tbody>
<tr>
<td>RTAX2000S</td>
<td>974,712</td>
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<tr>
<td>V4.64.0</td>
<td>16,800</td>
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<tr>
<td>V4.70.0</td>
<td>129,640</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td><strong>Grand Total</strong></td>
<td><strong>974,712</strong></td>
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<table>
<thead>
<tr>
<th>Device</th>
<th>Device-Hours</th>
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</thead>
<tbody>
<tr>
<td>RTAX4000S</td>
<td>637,072</td>
</tr>
<tr>
<td>V4.64.0</td>
<td>16,800</td>
</tr>
<tr>
<td>V4.70.0</td>
<td>129,640</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
</tr>
<tr>
<td>V4.80.0</td>
<td>32,000</td>
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<tr>
<td><strong>Grand Total</strong></td>
<td><strong>637,072</strong></td>
</tr>
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Power Matters

Introducing RTAX-DSP

Industry’s Most Reliable Space FPGAs Add Sophisticated DSP Capabilities
RTAX-DSP –
Fast DSP Without Sacrificing Reliability

- High performance DSP
  - RTAX-DSP Mathblocks run 18bit x 18bit multiply-accumulate at 125MHz over full military temperature range (-55°C to 125°C)

- True radiation tolerance
  - Configuration is not upset or changed by heavy ion radiation
  - DSP blocks protected against heavy ion radiation effects

- Lower power
  - Fewer parts to get the job done means lower power consumption

- Proven reliability
  - RTAX-DSP uses same 0.15µm UMC process, same antifuse programming technology, same basic architecture as RTAX-S/SL
  - Reliability characteristics expected to be identical

- No cost or schedule risk
  - No ASIC tooling charge (or repeat charge, if design changes are made)
RTAX-DSP Architecture Overview

Builds upon established RTAX-S/SL architecture
RTAX-DSP Mathblocks

- Important in FIR, IIR digital filters and FFT
### RTAX-S/SL and RTAX-DSP Families

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>System Gates</td>
<td>250K</td>
<td>1M</td>
<td>2M</td>
<td>2M</td>
<td>4M</td>
<td>4M</td>
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<tr>
<td>Dedicated Registers</td>
<td>1,408</td>
<td>6,048</td>
<td>10,752</td>
<td>9,856</td>
<td>20,160</td>
<td>18,480</td>
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<td>54K</td>
<td>162K</td>
<td>288K</td>
<td>288K</td>
<td>540K</td>
<td>540K</td>
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<td>Max User IO’s</td>
<td>248</td>
<td>516</td>
<td>684</td>
<td>684</td>
<td>840</td>
<td>840</td>
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<tr>
<td>DSP Mathblocks</td>
<td></td>
<td></td>
<td></td>
<td>64</td>
<td></td>
<td>120</td>
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<tr>
<td>Packages</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>CQFP</td>
<td>208, 352</td>
<td>352</td>
<td>256, 352</td>
<td>352</td>
<td>352</td>
<td>352</td>
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<tr>
<td>CCGA/LGA</td>
<td>624</td>
<td>624</td>
<td>624, 1152</td>
<td>1272</td>
<td>1272</td>
<td>1272</td>
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<td>Prototype Units</td>
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<td>NOW (CQ352)</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW (CQ352)</td>
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<tr>
<td>Qualification Status</td>
<td>Qualified &amp; Shipping</td>
<td>Qualified &amp; Shipping</td>
<td>QUALIFIED! Mil Std 883 Class B</td>
<td>Qualified &amp; Shipping</td>
<td>QUALIFIED! Mil Std 883 Class B</td>
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</tr>
<tr>
<td>Flight Units</td>
<td>NOW</td>
<td>NOW (CQ352)</td>
<td>Lead Time Applies</td>
<td>NOW</td>
<td>Lead Time Applies</td>
<td></td>
</tr>
</tbody>
</table>

- QML class Q and class V qualification planned for 2012
- 25% price reduction on RTAX-DSP effective November 2011!
RTAX-DSP Radiation Hardening

- **Register Cells**
  - Enhanced Single Event Transient (SET) protection in FPGA flip-flops
  - Triple-module redundancy for Single Event Upset (SEU) immunity

- **Mathblocks**
  - SET protection in Mathblock combinatorial logic
  - SEU protection in Mathblock sequential logic
RTAX-DSP Hardening By Design

R-Cell SET Mitigation

- **Hardened**
  - R-cell output buffer is triplicated on RTAX-DSP

- Improves SET performance by up to 16X

Mathblock SET Mitigation

- **Guard-Gate**
  - AND gate if signals agree
  - Latch if they disagree
  - Transients less than delay are filtered out

- Error rate better than 5E-9 Errors / DSP bit / day

Radiation Summary

- Enhanced R-cell provides approx. 16X more SET protection
  - RTAX-S @120 MHz: 1.9 events / RTAX2000S /100 years
  - RTAX-D @120 MHz : 0.12 events / RTAX2000D /100 years

- SET for Mitigated DSP blocks

  For a DSP-Bit (SEE/DSP-Bit/Day)
  GEO; 100mil; Z=2; no Funneling

<table>
<thead>
<tr>
<th>SET for DSP blocks</th>
<th>Multiply</th>
<th>ADD/ACC</th>
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</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>120 MHz</td>
<td>120 MHz</td>
</tr>
<tr>
<td>Solar Min</td>
<td>5.03E-09</td>
<td>1.15E-08</td>
</tr>
<tr>
<td>Worst Day</td>
<td>4.17E-06</td>
<td>1.27E-05</td>
</tr>
</tbody>
</table>

- All reports for RTAX-DSP can be found in published papers at SEE2010, NSREC 2010 conferences
  http://www.actel.com/documents/RTAXDSP_SEE_WP.pdf
IP and Tools

- **Smart Gen Mathblock configurator**
  - User interface allowing precise configuration of Mathblock
  - Mathblock macro IP cores available now
    - Multiply, Multiply and Add / Subtract, Multiply and Accumulate

- **RTAX-DSP Microsemi IP**
  - SmartDesign RTL generator using on-chip math blocks
  - CoreFIR 6.0 for RTAX-DSP available now
  - CoreFFT 4.0 Radix-2 Fast Fourier Transform available now
  - Additional DSP cores to follow

<table>
<thead>
<tr>
<th>IP Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fully enumerated FIR filter</td>
</tr>
<tr>
<td>Radix-2 FFT</td>
</tr>
<tr>
<td>Folded FIR filter</td>
</tr>
<tr>
<td>Interpolation polyphase FIR filter</td>
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http://www.actel.com/products/ip/default.aspx
Introducing RT ProASIC3: Flash FPGAs for Space

Reprogrammable RT ProASIC®3 Devices
Simplify Design of Space Systems
Reprogrammable FPGAs for Space

- Easy prototyping and hardware timing validation
  - Prototyping architecture and flight architecture are the same
- In-system reprogrammable on prototyping board
  - Does not jeopardize integrity of expensive prototyping board
- Reprogrammable in integrated flight hardware
  - Program with integration test patterns, then reprogram with flight design

Advantages of Flash FPGAs over SRAM FPGAs

- Both Flash- and SRAM-based FPGAs are reprogrammable
- Flash FPGAs retain their configuration in heavy ion radiation
- SRAM FPGAs lose their configuration in heavy ion radiation
  - Require mitigation – expensive, excessive power and board space
RT ProASIC3 Device Architecture

- Built using VersaTiles
- Up to 75,264 VersaTiles
  - Each VersaTile Can Be
    - 3-input Combinatorial Gate
    - Latch
    - D-Flip-flop with Enable
  - Register-intensive Applications Handled Easily
- All Input Signals Can Be Inverted
  - Easier Technology Mapping and Netlist Optimizations

Any 3-Input Combinatorial Function

D Flip-Flop With Enable and Set or Reset

Set or Reset
RT ProASIC3 Highlights

- Flexible Power Supply Voltage
  - $V_{CCA}$ nominal from 1.2V to 1.5V
  - Lower $V_{CCA}$ for power saving
  - Higher $V_{CCA}$ for higher performance

- Flash*Freeze Ultra Low-Power Mode
  - Flash*Freeze entry / exit in < 1µsec
  - Static power < 0.55mW
    (RT3PE600L, 25°C)
  - Preserves register states

- Qualification and Screening
  - Mil Std 883 Class B qualification completed
  - B-flow and E-flow available NOW
  - EV-flow coming soon
  - QML class Q qualification is planned for 2013
RT ProASIC3 Summary

- Prototype with low-cost commercial ProASIC3 devices today
  - Identical silicon, identical timing
    - Plastic FG484 and FG896 match Ceramic CG484 and CG896 footprint
    - RT-PROTO versions are available NOW

<table>
<thead>
<tr>
<th></th>
<th>RT3PE600L</th>
<th>RT3PE3000L</th>
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</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>600K</td>
<td>3M</td>
</tr>
<tr>
<td>Tiles</td>
<td>13,824</td>
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<td>Total RAM bits</td>
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<td>504K</td>
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<tr>
<td>Flash (ROM) bits</td>
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<tr>
<td>PLLs</td>
<td>6</td>
<td>6</td>
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<tr>
<td>Globals</td>
<td>18</td>
<td>18</td>
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<tr>
<td>Maximum IO</td>
<td>270</td>
<td>620</td>
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<tr>
<td>Packages (Availability)</td>
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<td>CQFP</td>
<td>256 (NOW)</td>
<td>256 (NOW)</td>
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<td>CCGA/LGA</td>
<td>484 (NOW)</td>
<td>484 (NOW)</td>
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<tr>
<td></td>
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<td>896 (NOW)</td>
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<tr>
<td>STATUS</td>
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<td>Mil Std 883 Class B Qualification Complete</td>
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</table>

Reliability Summary

- Qualification was completed per MIL-STD-883 Class B
- RT3PE3000L-CG896 used as qualifying vehicle
  - 79 units finished 3000+ hours of HTOL
- ESD Results – HBM
  - 2000V on all pins except PLL (500V)
  - Class 1B achieved
- Extensive reliability data set collected for 0.13um Flash process from UMC
  - Overall product FIT rate calculated $< 9 \text{ FIT}$ (60% confidence level, $EA = 0.7 \text{ eV}$)
Projected SEL onset LET at 68 MeV-cm$^2$/mg
  • Non-destructive SEL events have been observed at LET 80 MeV-cm$^2$/mg
No Flash cell configuration upset > 96 MeV-cm$^2$/mg LET
Single Event Upsets and Single Event Transients
  • Flip Flops do not upset with TMR mitigation
    – Synopsys Synplify and Mentor Precision RT synthesis have TMR options
  • Memory upsets – use EDAC or redundancy for memory protection
    – Onset LET$_{TH}$ ~ 0.5 MeV-cm$^2$/mg
  • Other SEEs, requiring manual instantiation of mitigation
    – Clock upsets, Logic transients, I/O bank transients

Well suited to Low Earth Orbit (LEO)
## RT ProASIC3 SEE Summary

<table>
<thead>
<tr>
<th></th>
<th>SEL (Events / FPGA-day)</th>
<th>FF SEU (No TMR, Errors / bit-day)</th>
<th>FF SEU (TMR, Errors / bit-day)</th>
<th>Logic Cell SET (Errors / bit-day)</th>
<th>I/O SET (Errors / bit-day)</th>
<th>I/O Bank SET (Errors / bit-day)</th>
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<tr>
<td><strong>Op Frequency</strong></td>
<td>Any</td>
<td>50 MHz</td>
<td>50 MHz</td>
<td>Max</td>
<td>50 MHz</td>
<td>50 MHz</td>
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<tr>
<td><strong>LEO</strong></td>
<td>1.9E-12 (RT3PE600L)</td>
<td>9.6E-9</td>
<td>SEU Immune</td>
<td>2.9E-10</td>
<td>7.4E-10</td>
<td>3.5E-8</td>
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<tr>
<td></td>
<td>2.7E-10 (RT3PE3000L)</td>
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<tr>
<td><strong>GEO Solar Max</strong></td>
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<td>4.82E-8</td>
<td>SEU Immune</td>
<td>1.79E-9</td>
<td>4.55E-9</td>
<td>1.77E-7</td>
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<tr>
<td><strong>GEO Solar Min</strong></td>
<td></td>
<td>2.65E-7</td>
<td>SEU Immune</td>
<td>1.45E-8</td>
<td>3.29E-8</td>
<td>1.02E-6</td>
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<tr>
<td><strong>GEO Worst Week</strong></td>
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<td>5.73E-5</td>
<td>SEU Immune</td>
<td>4.22E-6</td>
<td>8.09E-6</td>
<td>2.31E-4</td>
</tr>
<tr>
<td><strong>GEO Worst Day</strong></td>
<td></td>
<td>2.08E-4</td>
<td>SEU Immune</td>
<td>1.44E-5</td>
<td>2.76E-5</td>
<td>8.27E-4</td>
</tr>
</tbody>
</table>

**LEO:** 1000Km, 41° Inclination  
**GEO:** 100mil; Z=2; No Funneling

RT ProASIC3 Total Ionizing Dose (TID)

- Production TID test on RT3PE3000L-CG484 flight units
  - Testing at lower dose rates (500 and 5k rad / minute), per TM 1019
    - More representative of space than prior testing (~ 40 Krad / min and higher)
    - For comparison, dose rate in GEO space is around 10 mrad / min
  - Testing with $V_{\text{PUMP}}$ pin grounded (recommended)
  - Devices functional after 30 Krad
  - Propagation delay degradation 10% at 25 Krad to 30 Krad
  - DC parameters remain within datasheet specification at 50 Krad
    - Power Supply Current, Input threshold, Output drive and Transition Time

- Experimental low dose-rate TID test
  - Propagation delay degradation 10% at ~40 Krad, 15% at ~55 Krad
Low Dose Rate TID Tests

- Testing at ~ 1 rad / minute
- Propagation delay degradation (two wafer lots tested):
  - 10% at ~ 35 Krad, 15% at ~ 50 Krad, 30% at > 75 Krad
RT ProASIC3 Now in Space

International Space Station

RT3PE3000L-CG484
Planning to Fly RT ProASIC3

- Orbcomm Generation 2
- Interface Region Infrared Spectrograph
- Lunar Atmosphere Dust Environment Explorer
- Resurs P
- Glonass
IP for Space Applications
IP for Space Applications

- **Gaisler Leon3-FT**
  - 32-bit, SEE immune, 25 DMIPs at 25 MHz in RTAX-S/SL
  - Building flight and design-in heritage
    - **In Flight:** SIR-2 (Norway) on Chandrayaan-1 (India), Prisma (Sweden), Tacsat-4 (USA), RBSP (USA)
    - **Planning to fly:** Bepi Colombo (ESA), MMS (USA), Orbcomm (USA)

- **Gaisler Spacewire**
  - 100Mb/sec or higher in RTAX-S across T and V range

- **Microsemi Mil-Std 1553B**
  - Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT)
  - Can be supplied as netlist or as RTL, includes full test bench
  - Certified per RT validation test plan Mil-Hdbk-1553 Appendix A

- **Microsemi CorePCIF**
  - 33MHz and 66MHz; Target, Master, Target + Master configurations

- **Microsemi CoreFIR**
  - Fully enumerated, Folded, and Interpolation Polyphase versions
  - Utilize Mathblocks when targeted to RTAX-DSP

- **Microsemi Core FFT**
  - Radix-2
  - Utilizes Mathblocks when targeted to RTAX-DSP
Flight Heritage – IP Cores

EFA Typhoon
First Production Aircraft 2002
PCI

STEREO
Launched 2006
PCI

SWIFT / MIDE X
Launched 2004
PCI

Advanced EHF
Launched August 2010
PCI

SOFIE (Instrument) / AIM
Launched 2007
Mil Std 1553

James Webb
Space Telescope
Launch Expected 2018
Mil Std 1553

Next-Generation Space-Flight FPGAs
Roadmap for Space-Flight FPGAs

- **Rad Tolerant Flash**
- **RTAX-DSP**
- **RT ProASIC3**
- **RTAX-SL**
- **RTAX-S**
- **Class V Qualification**
- **Next Generation Space FPGA**

Next Generation Space-Flight FPGA

- Designed for high-bandwidth data processing in payload applications
  - Abundant high-performance programmable logic fabric
  - Embedded high speed multiply-accumulate blocks
  - Ample on-board memory with fast access time, two block sizes
  - High performance I/Os – SERDES, LVDS, DDR2, …

- Based on 65nm Flash low power process
  - Naturally resistant to configuration upsets
  - Non-volatile configuration so live at power-up
  - No external boot memory required
  - Low static power

- Radiation enhanced for space
  - Total ionizing dose
  - Single event effects
  - Latch-up immunity
# RT4P Family Resources

<table>
<thead>
<tr>
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<th>RT4P-6M</th>
<th>RT4P-12M</th>
<th>RT4P-16M</th>
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</thead>
<tbody>
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<td>LUT4 + TMR/SET FF</td>
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<td>120,000</td>
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<tr>
<td>User IO (non-SERDES)</td>
<td>436</td>
<td>616</td>
<td>644</td>
</tr>
<tr>
<td>RAM18K Blocks</td>
<td>116</td>
<td>206</td>
<td>290</td>
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<tr>
<td>uRAM1K Blocks</td>
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<td>210</td>
<td>294</td>
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<td>RAM Mbits</td>
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<td>18x18 Multiply-Accumulate Blocks</td>
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<td>588</td>
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<tr>
<td>SERDES blocks (x4 lanes)</td>
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<td>DDR2/3 SDRAM Controller</td>
<td>2x32</td>
<td>2x32</td>
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<td>Globals</td>
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<td>PLLs (Rad Tolerant)</td>
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<tr>
<td>UPROM Kbits</td>
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<td>303</td>
<td>342</td>
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</tbody>
</table>

**Packages**

- **CG1152**: ✓
- **CG1600**: ✓ ✓ ✓

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- **Package plan is currently in discussion – Strong probability of HERMETIC CCGAs!**
- **RT4P-16M is NOT in plan-of-record but can be added if demand justifies it**
Radiation Specifications

- **Total Dose**
  - > 100KRad TID

- **Single Event Effects**
  - *No configuration failures* (to be tested to > 110 MeV-cm²/mg)
  - No single event latch-up (to be tested to > 110 MeV-cm²/mg)
  - Mitigation for single event upsets
    - Flip-flops with TMR and asynchronous self-correction (LET_{TH} > 37 MeV-cm²/mg)
      - Flip-flops in the logic fabric
      - Flip-flops in embedded features – Mathblocks etc
    - On-chip SRAM (RAM18K and uRAM1K)
      - Built-in ECC
      - 1E-10 errors/bit-day, GEO solar min
  - Mitigation of single event transients
    - Logic cells hardened with SET filter
    - Target 1E-8 errors/bit-day, GEO solar min
Flexible Chip Architecture (RT4P12M)

- Hardened IP (PCI-Express)
- Mathblock
- Block RAM (18Kb)
- μRAM (1Kb)
- Logic
- PLL
- SERDES
- uPROM
- SDRAM DDRx Controller
- Power Matters
Family Floorplans

RT4P6M

First Device in Development

RT4P12M

RT4P16M

**RT4P Logic Module**

- Dedicated Flip-flop to enable efficient TMR hardening
  - With enable, asynchronous set/reset, and synchronous set/reset
- Fast carry chain to complement Mathblock performance
  - Arithmetic functions (add/subtract)
  - Target 300+MHz for 32-bit functions
- Industry standard LUT4 for efficient synthesis
- High utilization
  - LUT4 and flip-flop in same module can be used independently
  - Hierarchical routing architecture enables >95% module utilization
- 18 x 18 multiplier with advanced accumulate
  - New 3-input adder function: \((C + D) \pm (A \times B)\)
- 300 MHz performance
  - Optional TMR registers on all inputs and outputs (including the C input)
- SEE/SEU protected
RT4P Memory Blocks

- **Radiation Tolerant**
  - Resistant to multi-bit upset
  - Built-in EDAC (DBD/SBC)

- **RAM18K**
  - Dual-port (x18) or Two-port Options (x36)
  - High performance (> 300MHz) synchronous operation
  - Example usage
    - Large FFT memory

- **uRAM1K**
  - 18-bit Three Port Memory
    - Synchronous Write Port
    - Two Asynchronous or Synchronous Read Ports
  - Example usage
    - Folded FIR filters and FFT twiddle factors
uPROM Non-volatile Memory

- Non-volatile memory based on FPGA configuration cell
  - Configuration upset immune
  - TID >= 100KRad
- 250Kbits to 450Kbits storage for DSP coefficients
- Initialize RAMs and registers from uPROM
  - Power-on initialization
  - Modification of coefficients during normal operation
  - RAM scrubbing
- Read performance of 25MHz x 32-bits
General Purpose IO

- Single ended standards
  - LVCMOS from 1.2V to 3.3V
  - LVTTL
  - PCI

- Voltage reference standards (600+ Mbps)
  - SSTL2
  - SSTL18 and SSTL15 (with termination) for DDR2/DDR3 SDRAM memories
  - HSTL18 and HSTL15 (with termination) for SRAM memories

- True LVDS with termination (600+ Mbps)
3.125Gbps SERDES

PMA Based on PCIe Gen 2 PHY
RT Performance = 1 – 3.125Gbps
Up to eight x4 units
SERDES Ganging Options

RefClkA
RX0/TX0
Rx1/TX1
RX2/TX2
RX3/TX3
RefClkB

PLL
PLL
PLL
PLL

Lane 0
Lane 1
Lane 2
Lane 3

x1
x1
x1
x1

x2
x2
x2
x2

X4 (Requires RefClkB = RefClkB)
DDRx Controller

- Built-in DDR Controller
- 8/16/32-bit External Data Bus
- High Performance
  - Operation speed to 666Mbps (333MHz Clock)
  - Support for DDR2 and DDR3
- ECC Options
  - X16 and X32 widths
Performance Summary

- General purpose logic
  - 250MHz system performance
  - >300MHz DSP support performance (adders, delays, etc.)

- Mathblock
  - 300MHz pipelined performance

- RAM18K and uRAM1K
  - > 300MHz

- IO
  - > 600Mbps LVDS and DDRx SDRAM data
  - SERDES to 3.125Gbps

- Overall
  - 250MHz general system performance
  - 300MHz signal processing performance
RT4P Product Availability

- Non-RT *SmartFusion2* devices for emulation and development
  - Not footprint compatible with RTG4, no SEU hardening, timing differences
  - Initial device: M2S050
  - Software general availability: **NOW**
  - Commercial device availability: Early 2013

- RT devices for space flight applications
  - Initial device: RT4P12M
  - Early SW access: Early 2014
  - Sample RT4P12M silicon: Early 2015
  - 883B flight units: 2015
  - QML qualification: 2016
New Product Concepts
Space System Manager

- Working on customizable Space System Manager
- Concept
  - Space systems need voltage, current and temperature telemetry
  - Space systems need digital control of motors, actuators and pyrotechnics
- Microsemi AMSG-HiRel has expertise in the analog / mixed signal aspects
- Microsemi SOC has expertise in the digital aspects
- Next steps – road-test concept with key customers, develop business case
Space Forum

- Detailed discussions on
  - Microsemi space products – discrete, linear, power, RF, ASIC, FPGA
  - Space product roadmap
  - Design tips and tricks
  - Qualification and reliability updates
  - Radiation testing results and mitigation strategies
  - Package development and roadmap
  - Development and verification tools

- Available for download at www.actel.com/asf

- Next events
  - USA – Dec 4, 2012, Los Angeles, CA
  - Europe – Spring 2013, Noordwijk, NL