



High Performance Partitioning

www.flexras.com
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- **CAD tools for FPGA-based Systems**
 - Wasga Compiler
 - Wasga Debug
 - Wasga Architect
- **IP**
 - High speed robust inter-chip communication IPs
 - IP for DUT debug
- **Service**
 - FPGA prototyping and verification
 - FPGA design
 - DO-254

Wasga Compiler

Timing-driven placement:

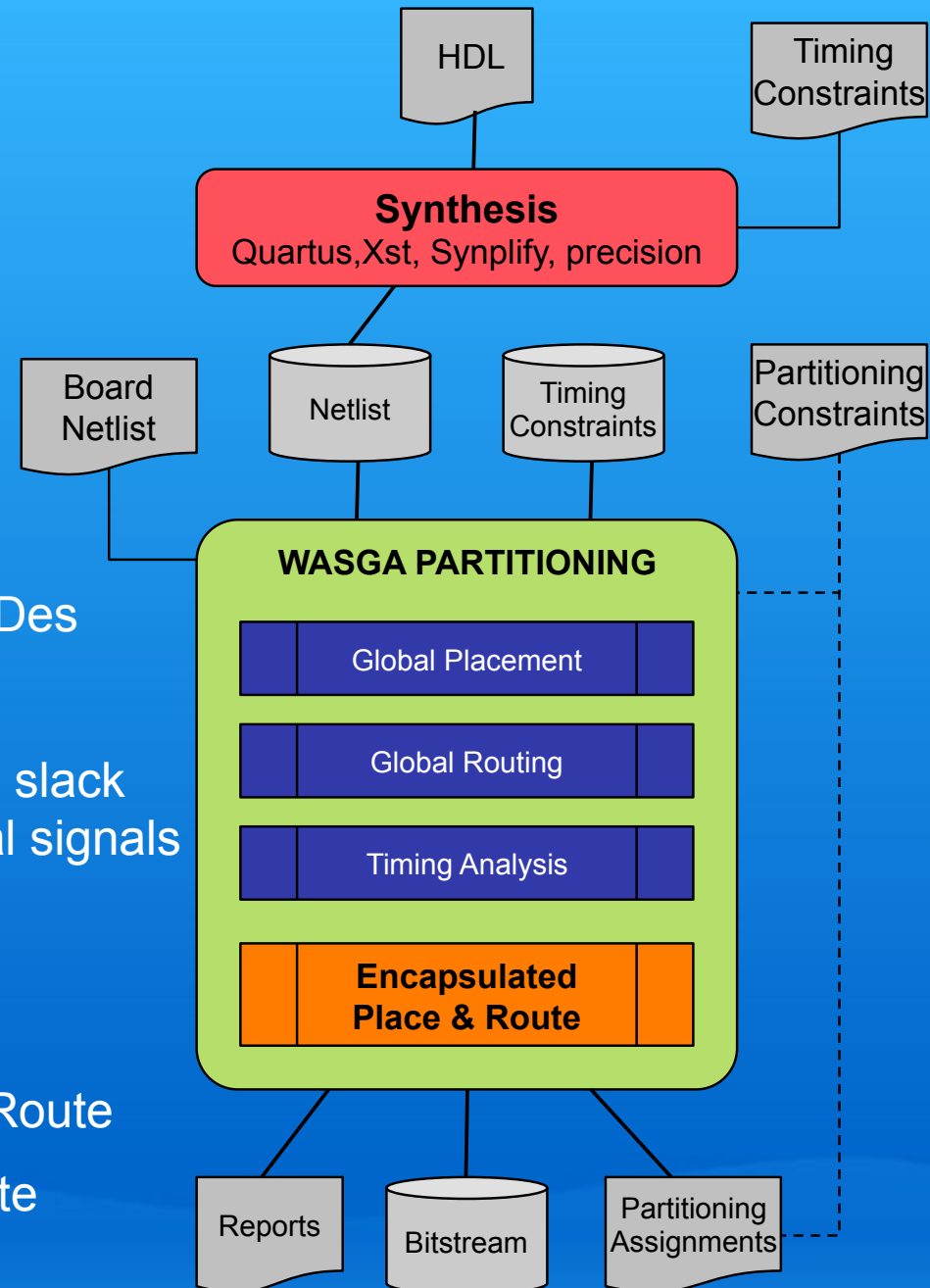
- clusters critical paths in FPGA
- optimizes critical paths crossing FPGA
- Manages clock domains

Timing-driven routing:

- Source-synchronous LVDS DDR and SerDes
- Critical signals are not multiplexed
- Pin multiplexing even optimized based on slack and automatically inserted on least critical signals

Timing Analysis:

- STA, critical paths before FPGAs Place&Route
- Accurate STA after all FPGAs Place&Route



Wasga Ease-of-Use

The screenshot displays the Wasga software interface with the following components:

- Board Statistics Panel:**
 - Board Schematic Preview:** Shows a schematic with six FPGA blocks labeled fpga_a through fpga_f. fpga_b and fpga_e are highlighted with blue borders.
 - FPGA Information:**
 - FPGA Name: fpga_b
 - FPGA Type: NONE
 - Resource lut: ovf=0 / max=27648 / used=25333 / available=69120
 - Resource ram: ovf=0 / max=4051 / used=38 / available=10128
 - Resource reg: ovf=0 / max=27648 / used=17283 / available=69120
 - Resource dsp: ovf=0 / max=25 / used=0 / available=64
 - Resource ramlut: ovf=0 / max=7168 / used=512 / available=17920
- Global Placement / Global Routing Panel:**
 - Global Placement Table:**

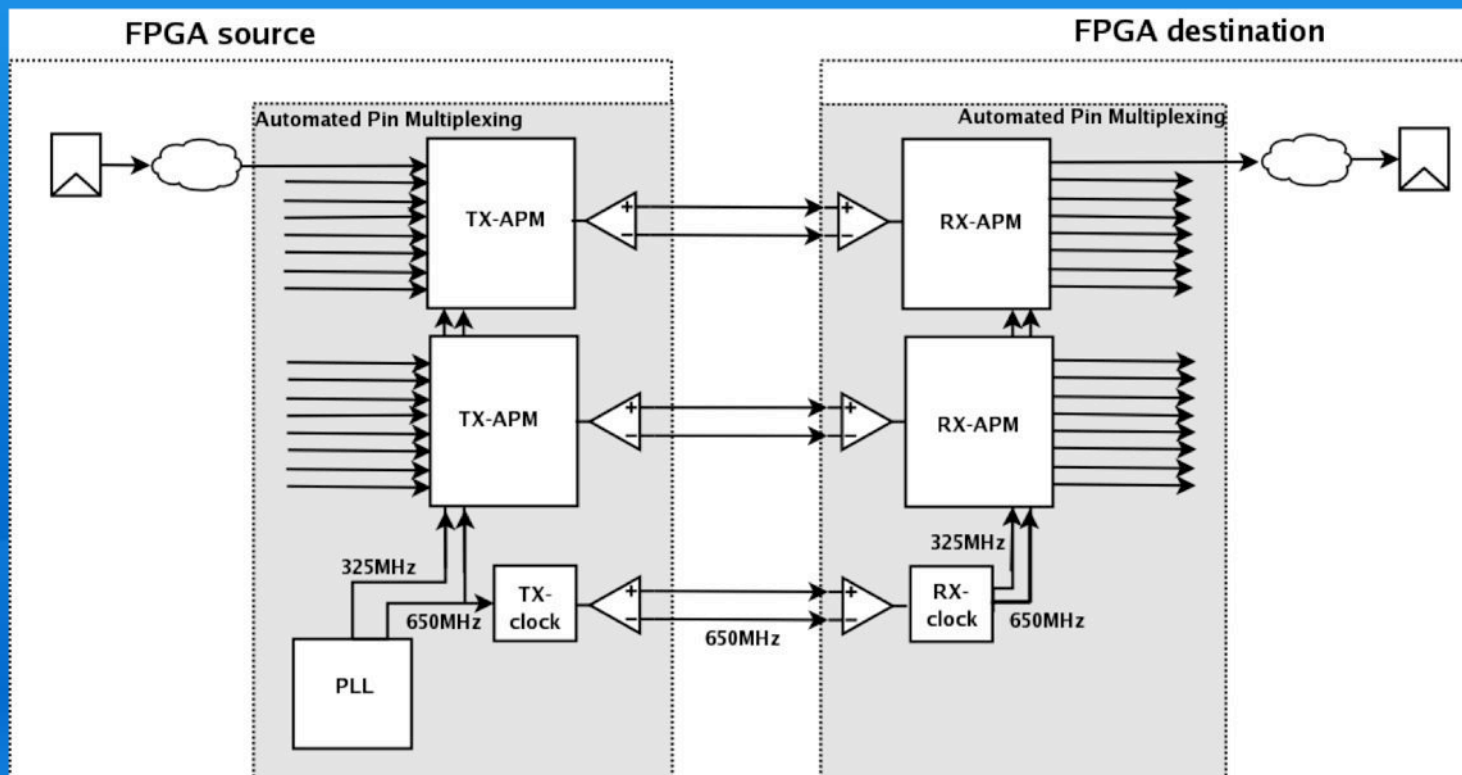
fpga_a	0	72
fpga_b	72	0
fpga_e	70	212
Interface	1	5
TOTAL	143	289
 - Global Routing Table:**

From \ To	fpga_a	fpga_b	fpga_e
fpga_a	0	72	(0)
fpga_b	72	0	(80)
fpga_e	(80)	0	70
Interface	(80)	(160)	212
TOTAL	143	289	
- Project Configuration Panel:**
 - Copy Scripts to Working Directory:** ☐
 - Clock Assignment File(s):** /home/mrabet/DEV/WASGA/benchs/testbenchs/mb4_
 - Pin Assignment File(s):** /home/mrabet/DEV/WASGA/benchs/testbenchs/mb4_
- Pin Assignments Wizard Dialog:**
 - Design Port Name:** xps_uartlite_0_RX_pin, xps_uartlite_0_TX_pin
 - FPGA Pin Name:** FPGA_B_RS232_RX, FPGA_B_RS232_TX
 - Buttons:** clear, Add Pin Assignment, < Back, Next >, Cancel

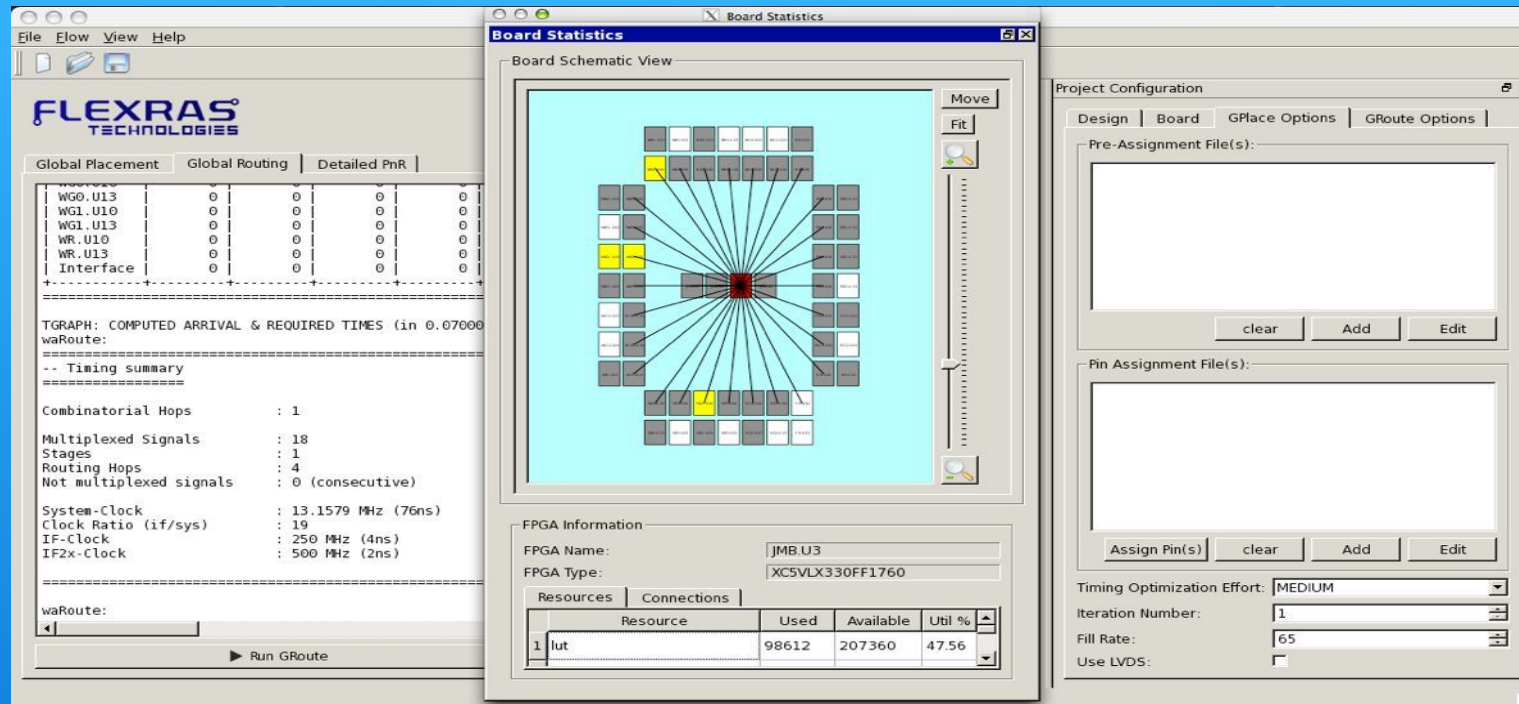
Automatic Pin Multiplexing (APM)

High Speed Tx/Rx IP modules

- Source synchronous system Lvds/Serdes
- Configurable multiplexing ratio
- Training counter to automatically configure input delay
- Checksum to verify correctness of communication data



Wasga Results



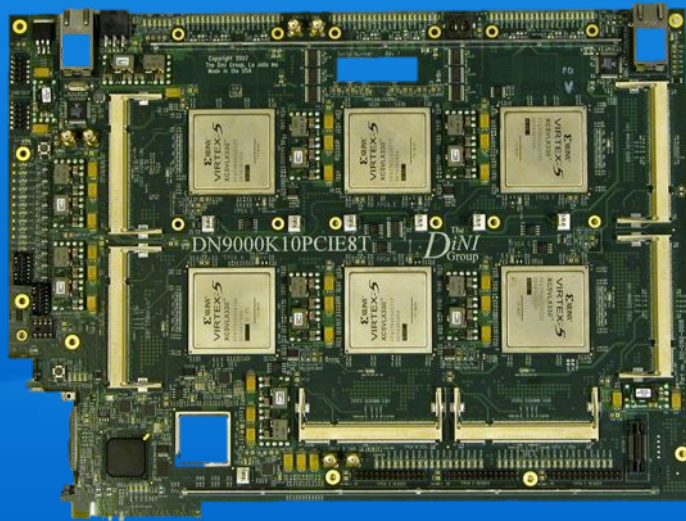
Hierarchical : 64 FPGA in multi-boards, LVDS
 Heterogeneous : Both Virtex-5 and Virtex-6

	FPGAs Used	FPGA Utilization	Partitioning Runtime	Memory Usage	Multiplexing ratio	System Clock Frequency
Design 1	45	47 %	70 min	12 GB	104	7 MHz
Design 2	12	60 %	15 min	5 GB	16	32 MHz

High Performance – High Capacity – Fast Runtime

Wasga Partitioning is Proven

- Wasga Partitioning OEM by world leading FPGA emulation vendor
 - In production since 2010
 - Used daily throughout the world
 - Routinely handles designs up to 1 billion gates
- Benchmarks and silicon validation
 - Using DINI DN9000K10PCI with 6 Xilinx XC5VLX110s
 - Using DINI DNV6F6PCIe with 6 Xilinx XC6VLX365T



Partners

Atmel

- Wasga is compatible with Atmel FPGA
- Access to the latest FPGA technology



Xilinx

- Alliance Program Member
- Access to the latest FPGA technology
- Wasga supports all Xilinx FPGA
- Wasga interface with ISE and Vivado Xilinx software



Dini Group

- Access to the latest boards technology
- Wasga supports all Dini boards
- Same distributor in Europe: EuropeLaunch

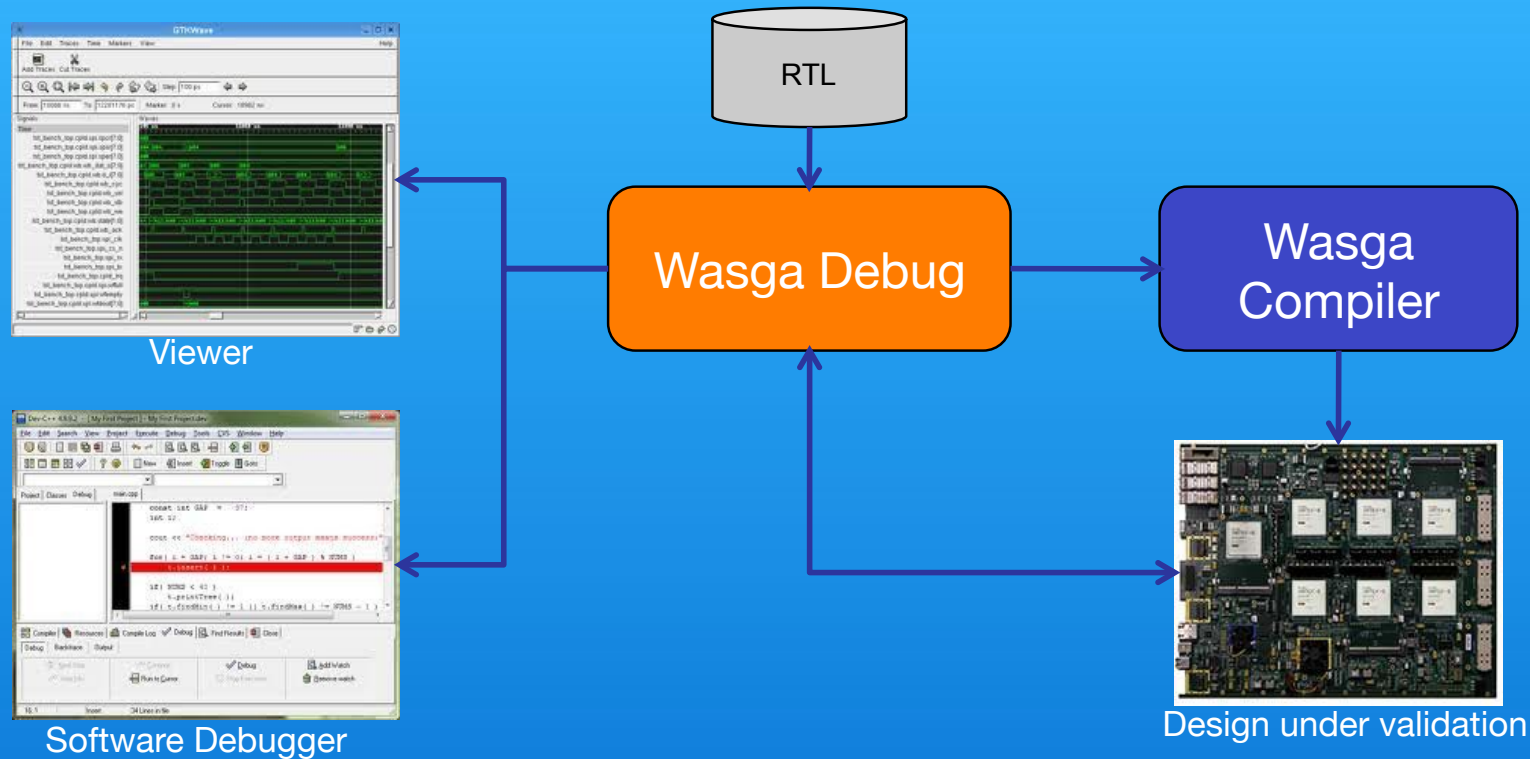


Reflex-Ces

- Partner in PPR european project
- Develop jointly prototyping board with 3 Virtex-7



Wasga Debug



Debug environment for hardware/software validation:

- Fast and easy capture probe insertion in FPGAs
- GUI interface to select signals in the RTL or Netlist
- Compact signals capture architecture
- Manages many FPGAs
- Minimizes recompilation
- Simulator-style view

Wasga Architect

- Board synthesis tool
 - Generates custom FPGA board from RTL
 - Simplify multi-FPGA custom board design
 - Partition SoC design
 - Define the number of FPGA
 - Define traces between FPGAs
 - Estimate board performances
- Inputs
 - RTL
 - Timing constraints
 - FPGA vendor & family
- Outputs
 - Board netlist
 - Board floorplan

