



Workshop FPGA ESA November 5th, 2012

Design flow precision - IDS



AGENDA

- Precision
- Precision constraints from IDS
- Improved customer design
- Target for timing improvement in IDS
- Application notes

PRECISION

New production release : **Precision Synthesis OEM 2012b**

Main Behavior by default :

- GCLKBUF and RSBUF automatically inserted
- max fanout : 100
- Replicate as max fanout strategy (setup_design -max_fanout_strategy =none)
- Flatten netlist
- No register in the pads

New variable : Setup_design -atmel_map_option { option(s) }

5 Options : lpm, no_lpm, single_output_macros, dual_output_macros and no_flatten_hierarchy

By default : lpm and single_output_macros

More efficient option : dual_output_macros (FGEN2(T), FGEN2R(T), FGEN1R(T), MGEN, and MGENR(T))

Old variables : warning message

PRECISION (suite)

Optimization :

- Minimum timing constraint :
create_clock to define all the clocks in the design
- More efficient atmel_map_option : dual_output_macros
- Retiming option is now available
- lower max fanout value :
 - General max value : setup_design -max_fanout=30,
 - Max value for a net : set_attribute -net ce20 -name max_fanout -value 2
- I/O pads with register : only if there are timing constraints at the design interface

set_attribute -design RTL -name INFF/OUTFF/TRIFF -value true -port name
To implement IBUFR you have to forbid OBUFR insertion

Precision constraints from IDS

- 8 GCK and 4 FCK :
 - External clocks and now derived clocks can use GCK
 - Only 2 from 4 FCK usable (one per column)
- Only one global reset available (RSBUF) : The global can be used now by external or derived reset

Set_attribute -design RTL -name PRESERVE_SIGNAL -value true -net <name net> or
set_attribute -design rtl -name MAX_FANOUT -value <needed value> -net {nreset_out}

- No unconnected Dout pins for the RAM
- IO pad with register :
 - Clock Skew between the core and the periphery
 - For each pad type, one global clock per die side
- Memories as black boxes is mandatory

Optimisations summary

	Timing optimisation	Place&route Optimisation
Dual_output_macros	x	x
Retiming	x	
General max fanout		x
Local max fanout	x	x
I/O pads with register	x	
Memory as black box		X

Example of Improved customer design

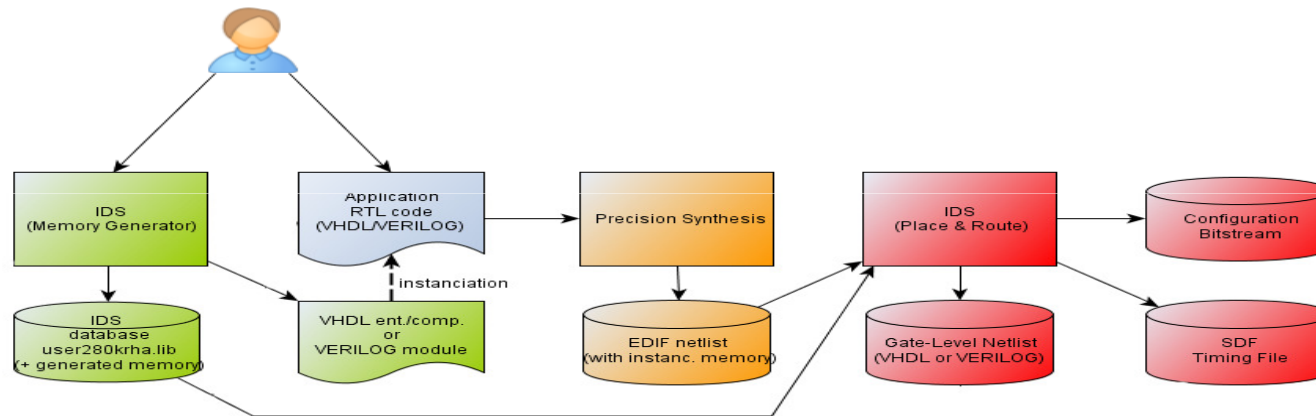
- ACDC3 : frequency target 20MHz
 - TAS information (november 2009)
Actel RTSX72SU : 31 Mhz (used ressources 69%)
Atmel ATF280F : 12 Mhz (used ressources 27%)
 - Last Atmel P&R (IDS 9.1.3a, precision 2012b)
Atmel ATF280F : 18 Mhz (+50%), (used ressources 17 %)
- After timing improvement in IDS : expected, 25 MHz

Target for timing improvement in IDS

- Customer design:
 - Max frequency from IDS (typ) : 29 MHz
 - Max frequency measured on board : 40 MHz
- Atmel design:
 - Max frequency from IDS (typ) : 25 MHz
 - Max frequency measured on board : 40 MHz

Application notes

- Available under AEDOS
- Memory generation in IDS in AT40K FPGA family (ref : 41020-AERO-10/12)



- Design Flow ATF280F (ref : 41021A-AERO-10/12 : Description from synthesis to final checks (simulation, formal proof))

THANK YOU !



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