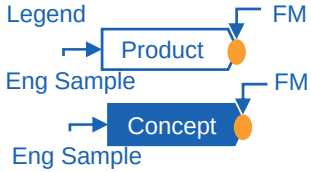
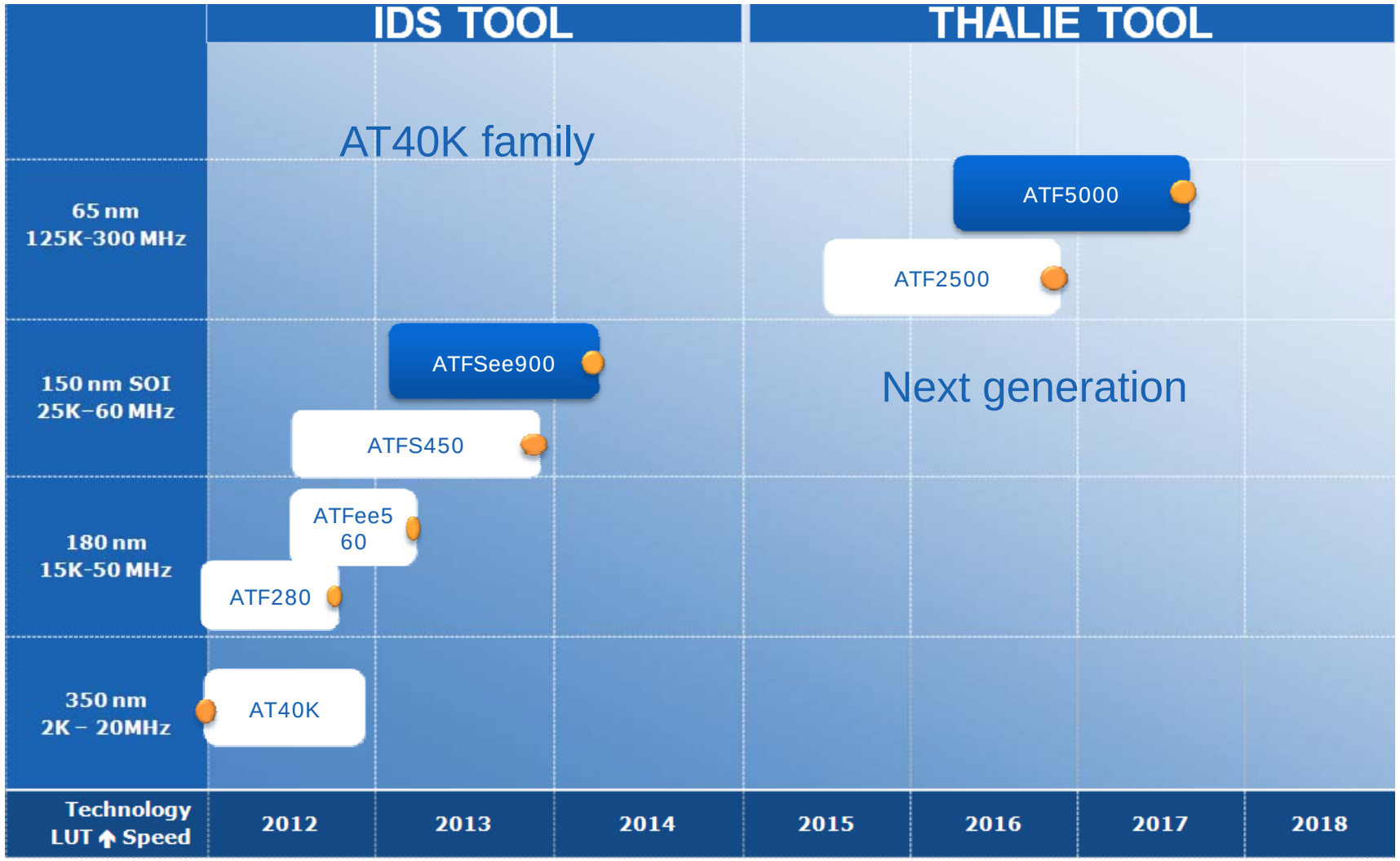
FPGAs For SPACE APPLICATIONS

2012, Sept.

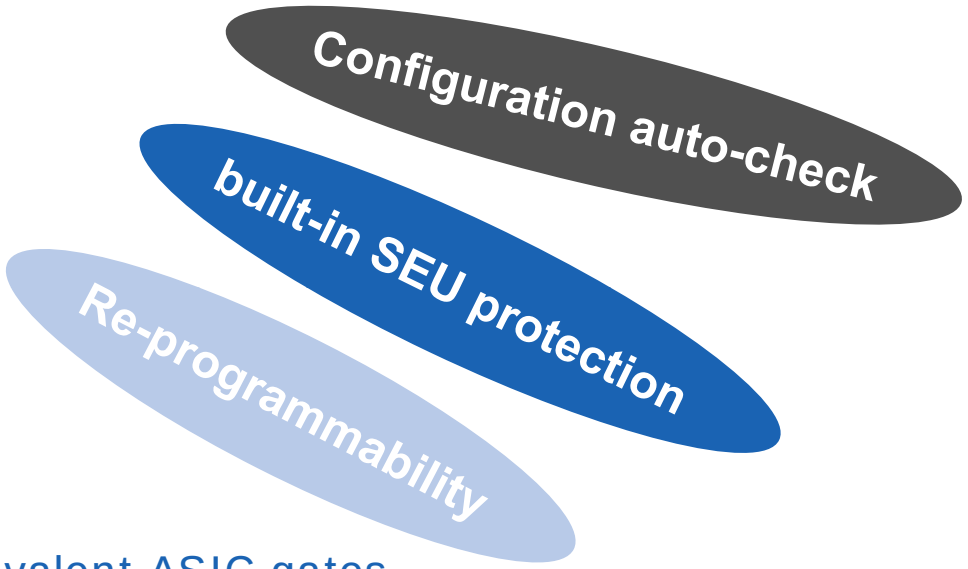
Roadmap





AT40K FPGA FAMILY

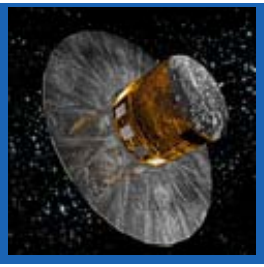
New alternatives with the AT40K SRAM-based FPGA series for low gate count designs requiring low-power applications



- **Technology**
  - From 0.35 to 0.15µm
- **AT40K architecture**
- **Products features**
  - From 40K to 450K gates equivalent ASIC gates
  - From 48*48 to 152*152 core-cells (each 2 LUT + 1 DFF)
  - Embedded memory blocks (freeRAM)
- **ATMEL EEPROM's for FPGA configuration**

FLIGHT HERITAGE & PLANNING TO FLY …

Megha-tropiques
Oct 2011



Gaïa
2012

Sentinel-1
2013

Pharao
2013

CFOSAT (swim)
2014

SeosAT
2014

Svom
2015

Bepi-Colombo
2015

AT40KEL040

- **Technology**
  - 0.35um
- **Product features**
  - 46K gates equivalent ASIC gates
  - 20 MHz clock speed
  - 2304 core-cells (each 2 LUT + 1 DFF)
  - 18 Kbit FreeRAM (144 modules of 32x4)
  - 3.3V Core and I/Os
  - Packages CQFP 160 & 256

Qualification status

DLA qualified with SMD 5962-03250
ESCC qualified with ESCC DS 9304/008

Radiation Performances

TID Tested up to 300Krads
SEL >70 MeV/mg/cm2
SEU 2.3 E-10 error/bit/day
(GEO orbit - worst case)

ATF280

- **Technology**
  - 0.18um
- **Product features**
  - 280K gates equivalent ASIC gates
  - 50 MHz clock speed
  - 14400 core-cells (each 2 LUT + 1 DFF)
  - 115 Kbit FreeRAM (900 modules of 32x4)
  - I/O's cold sparing PCI compliant
  - 8 pairs LVDS 240 Mbps
  - 1.8V Core and 3.3V I/Os
  - Packages MC/MLGA472 & CQFP 352

Qualification status: in progress
DLA qualified with SMD 5962-12225
ESCC qualified with ESCC DS 9304/xxx

Radiation Performances
TID: Tested up to 300Krads
SEL Performances: >70 MeV/mg/cm2

ATFS450

- **Technology**
  - 0.15um **SOI**

- **Product features**
  - 450K gates equivalent ASIC gates
  - 70 MHz clock speed
  - 152*152 core-cells (each 2 LUT + 1 DFF)
  - 180 Kbit FreeRAM (900 modules of 32x4)
  - I/O's cold sparing PCI compliant
  - 8 pairs LVDS 240 Mbps
  - 1.5V Core and 3.3V I/Os
  - Packages CQFP 352

Under development

Engineering samples	13Q2
Flight Models	14Q1

Radiation Performances Goal

TID: > 100Krads

SEL Performances: latch-up immune (SOI)

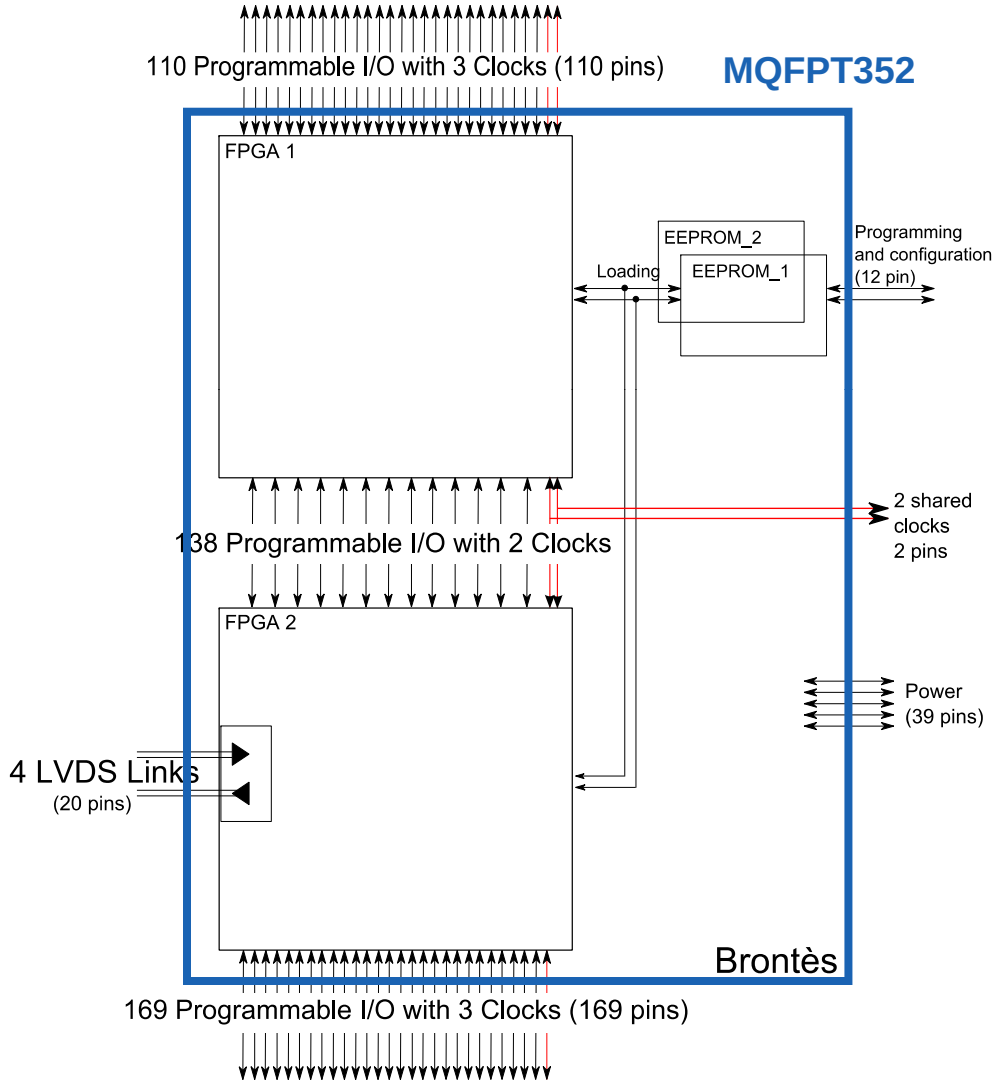
ATFee560

- **Technology**
  - 2 ATF280 and 2 Eeprom AT69170
- **Product features**
  - 2* 280K gates equivalent ASIC gates
  - 50 MHz clock speed
  - 2* 152*152 core-cells (each 2 LUT + 1 DFF)
  - 2* 115 Kbit FreeRAM (900 modules of 32x4)
  - I/O's cold sparing PCI compliant
  - 2* 8 pairs LVDS 240 Mbps
  - 1.8V Core and 3.3V I/Os
  - Packages CQFP 352

Under development

Engineering samples	12 Nov.
Flight Models	13 Q2

ATFee560



	pins
FPGA1 Programmable I/O's	110
FPGA2 Programmable I/O's	169
LVDS (4TX + 4RX)	20
Shared Clocks	2
Power Supply	39
Configuration	12

IP's SOLUTIONS

Current Development (2012-2013)

- SpaceWire / 1553
- PCI
- CAN
- UART

Under development

Future development

- ESA Core
- SMCS TM/TC
- AVR8

Each IP ported on AT40K, ATF280 and AFTS450 with the adapted level of documentation and support.

With a **DO254-like** process for high quality IP deliverables

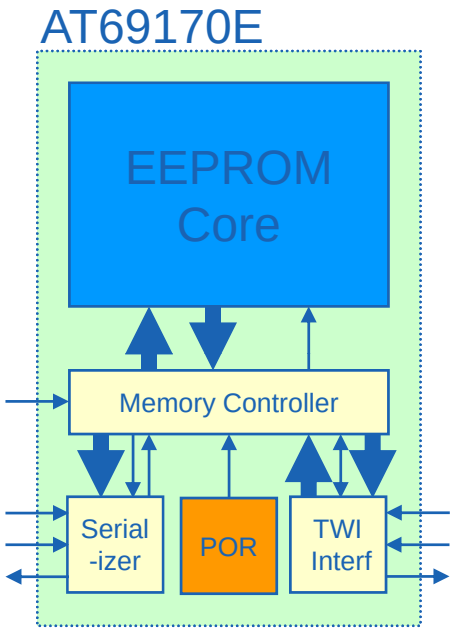
Configuration EEPROM
AT69170E Key Features

- 4 Mbit Rad Hard EEPROM
- 512 bytes Pages

- Standard TWI programming interface
- FPGA serial configuration interface

- 3.3V Supply Voltage
- FP18 Package

- Endurance: 10K cycles
- Data retention: >15 years at 125°C
- TID > 60Krd biased
- Programming tools
  - Standalone USB programmer



Qualification status: in progress
DLA qualified with SMD 5962-12xxx
ESCC qualified with ESCC DS 9xxx/xxx

Configuration EEPROM
16 / 32 Mbits EEPROM

Under Development
Flight Models in 2015

- Serial or parallel EEPROM
- ESA Program
- Endurance: 10K cycles
- Data retention: >15 years at 125°C

Radiation Performances Goal
TID: > 60kRads (100 kRads expected)

- Applications
  - Configuration memory for FPGA

  But also
  - Parameters storage or updates during missions
  - Boot memory for processors
  - Application software storage

NEXT GENERATION FPGA
Starting with AT2500

Project under Construction

- > 100k LUT & DFF
- > 5 Mbit FreeRAM
- 300 MHz clock speed
- DDR3 LVDS, HSSL

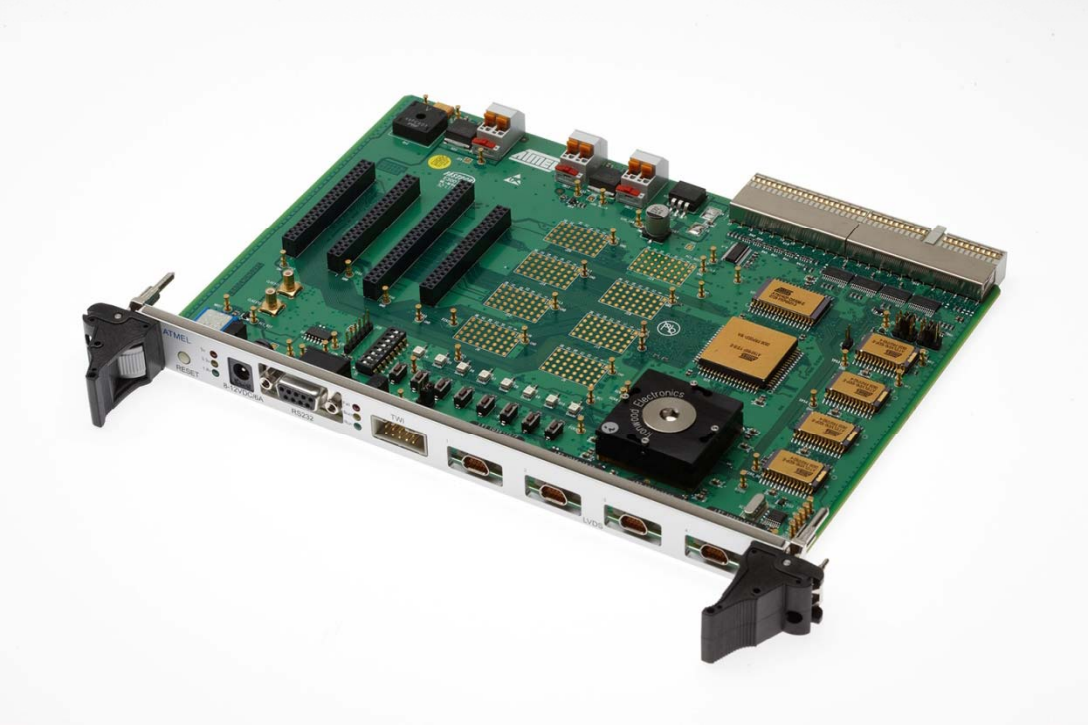
- New Place and Root tool

- Packages Flip-Chip 800-1000

DEVELOPMENT KIT

Development kit is the main platform to:

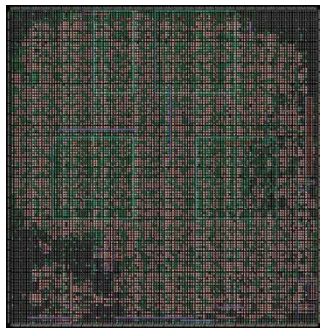
- Evaluating the Atmel FPGA
- Demonstrating the Atmel FPGA
- Developing Atmel FPGA-based applications



DESIGN TOOLS

MENTOR Precision Synthesis

- VHDL / Verilog entry
- Automatic IDS Macro detection and mapping



Example: Leon3

ATMEL Figaro IDS

- Automated Place & Route
  - STA
  - Power Estimator
  - VHDL / Verilog netlist export with SDF back-annotation
  - Bitstream generation

ATMEL Configurator Programming Tool

Contact and Documentation

- Atmel website

  http://www.atmel.com/products/other/space_rad_hard_ics/rad_hard_fpgas.aspx

- Hotline

  Radhard-fpga@atmel.com

- Dedicated Atmel-Aero-FPGA
  http://spacefpga.atmel-nantes.fr/

  Dedicated Forum for Atmel-Aero-FPGA
  http://spacefpga.atmel-nantes.fr/phpBB/index.php

- Radiation reports upon request

- Qualification Datapackage upon request