A CAD Flow for the Analysis of SEU Sensitivity of SRAM-FPGA Systems

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Goal

- Allow designers to **assess the sensitivity to SEUs** of FPGA-based applications…
  - …as **early** as possible during the design process (before prototypes are available)…
  - …with easy-to-use and cheap **software tools**

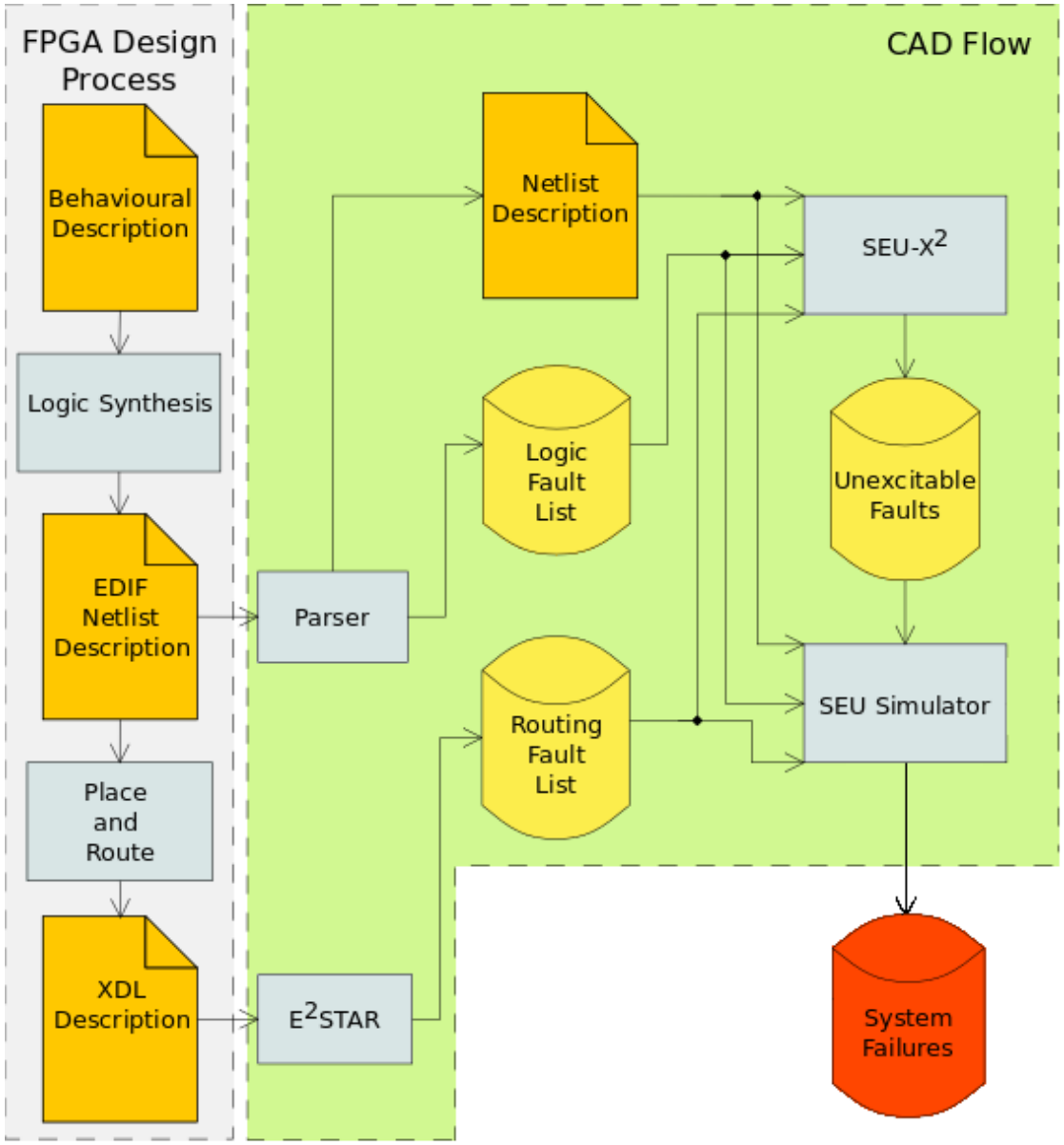
Motivation

Lack of simulation tools of <u>SEUs in the configuration memory</u> of FPGA-based systems*

Tool Name	Developer	Tech	SEU injection	SEU sim at SW speed	SEU emu at HW speed	Monitor fault propagation	SEU weak areas finding	Recognize & check TMR	SEU in FPGA Conf mem	Improve P&R of SRAM-FPGA
FT-UNSHADES	U. Seville (E)	**all**	yes		yes	yes	yes		yes	
SST	ESA (NL) / U. Antonio Nebrija (E)	**all**	yes	yes		yes	yes			
FLIPPER	INAF (I)	**Xilinx FPGA**	yes		yes	yes	yes		yes	
STAR/VPLACE /RoRA	P. Torino (I)	**Xilinx FPGA**					yes		yes	yes
INFAULT	ESA (NL)	**all**					yes	yes		
SUSANNA/ JONATHAN	P. Torino (I) / ESA (NL)	**Atmel FPGA**					yes		yes	yes

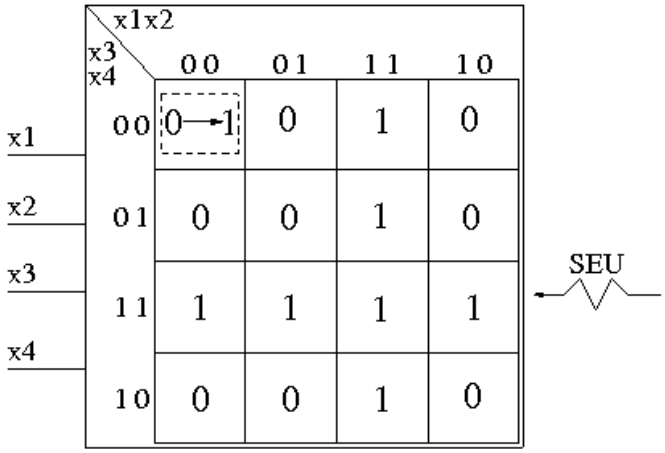
*Agustín Fernández-León. “ASIC and FPGA for space applications: technology and strategies to counteract radiation effects”, keynote talk at DCIS2010

The CAD flow



- EDIF Parser
  - Netlist description
  - Effects of SEUs in the logic
- E^{2}STAR
  - Critical configuration bits
  - Effects of SEUs in the routing
- SEU-X^2
  - Unexcitable SEUs
- SEU Simulator
  - Failures of the system

Fault Model (SEUs in the logic)



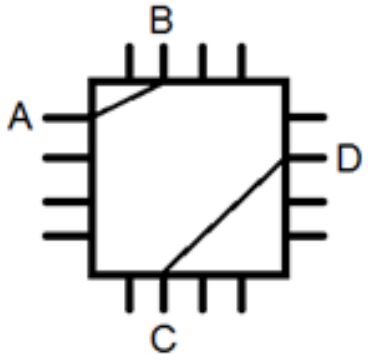
$$y=x_1 \cdot x_2 + x_3 \cdot x_4$$

$$y=x_1 \cdot x_2 + x_3 \cdot x_4 + \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3} \cdot \overline{x_4}$$

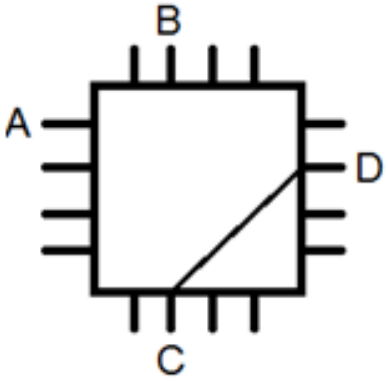
More accurate than the Stuck-at fault model*

*M. Rebaudengo *et al.* "A new functional fault model for FPGA application-oriented testing", in DFT 2002

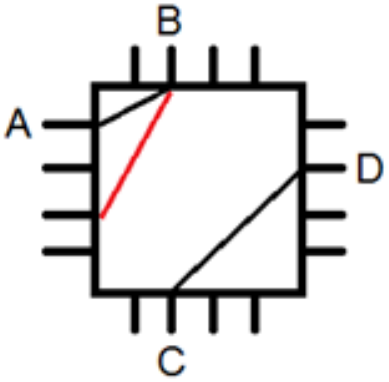
Fault Model (SEUs in the routing)



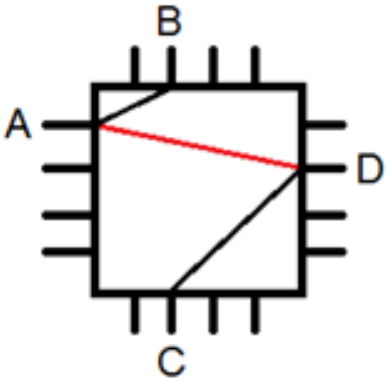
Original Configuration



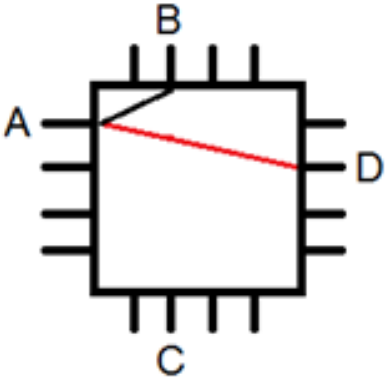
Open Fault



Antenna Fault



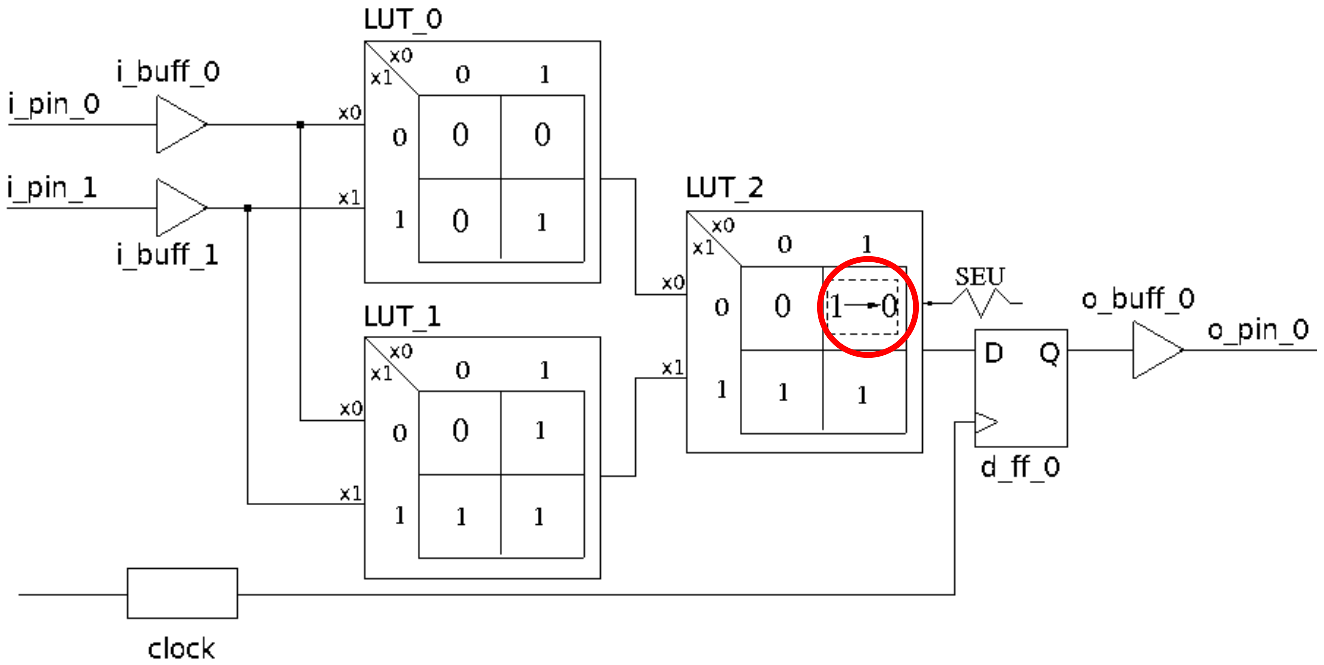
Conflic Fault



Bridge Fault

*M. Violante *et al.* "Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications", Springer Science & Business Media, 2011.

Unexcitable SEUs



The SEU in the conf. bit (x_0=1, x_1=0) of LUT_2 is

unexcitable

The system behaves correctly even after the occurrence of the SEU

The SEU-X^2 tool: system modeling

- **SAL description language** for system specification

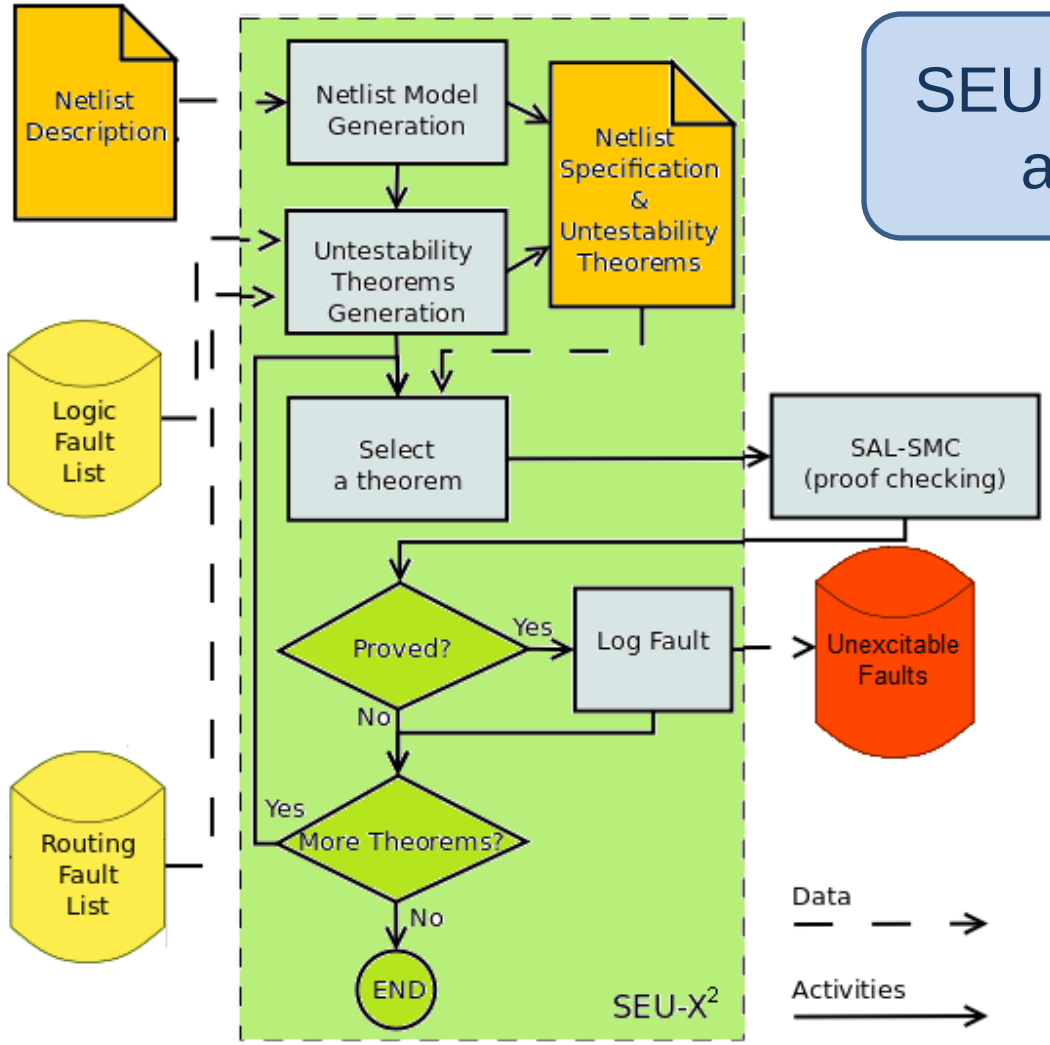
```
LOCAL LUT_2 : BOOLEAN;
x0 = LUT_0; x1 = LUT_1;
LUT_2 = x0 OR x1;
```

- **LTL formulas** for unexcitability theorems

```
G(NOT(x0=TRUE AND x1=FALSE));
```

- **SAL-SMC** (*Symbolic Model Checker*) for unexcitability theorem proofs

The SEU-X^2 tool: the software flow



SEU excitability analysis

References:
IOLTS12

SEU-X^2 automatically:

- builds the system model
- builds the unexcitability theorems
- invokes SAL-SMC
- generates the unexcitable SEU list

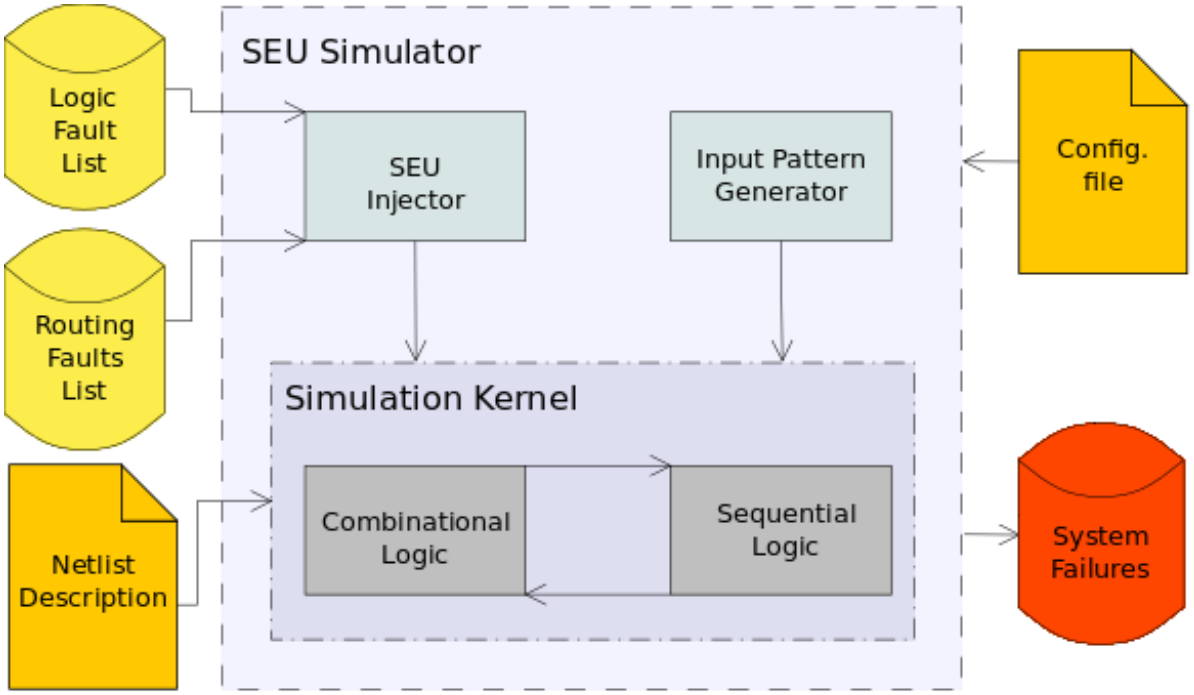
The SEU Simulator

Unexcitable SEUs **cannot** cause system failures

What about excitable SEUs?

The SEU simulator is used to determine **which of the excitable SEUs can actually lead to failures** of the system

The SEU Simulator



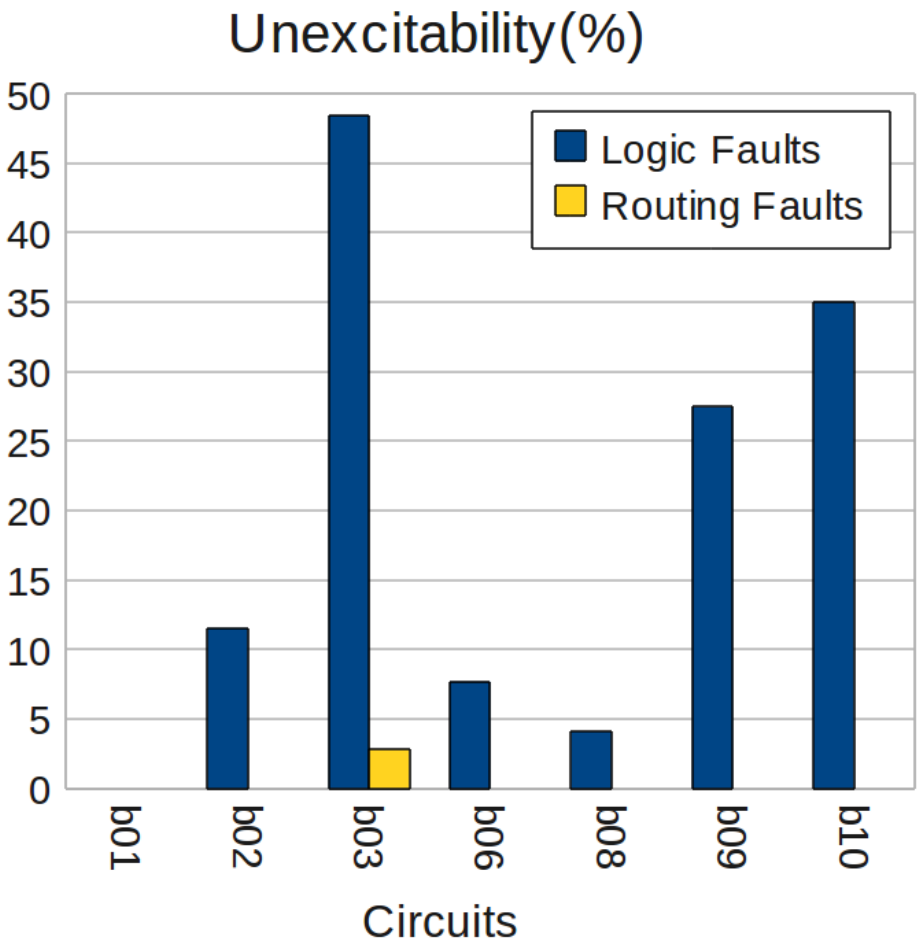
SEU sensitivity analysis

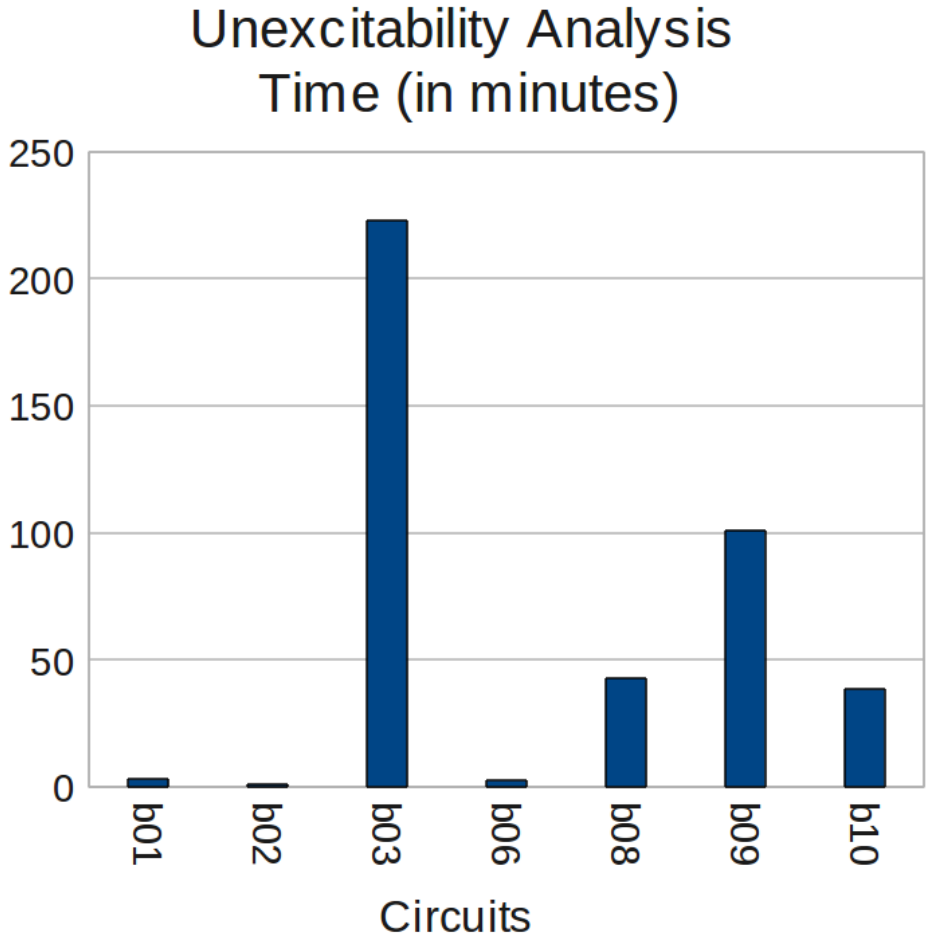
References:

FPL11, DDECS11, DFT12

- LUT level simulator
- Emulation of SEUs in the configuration memory
- Deterministic/Random input patterns
- Vendor independent

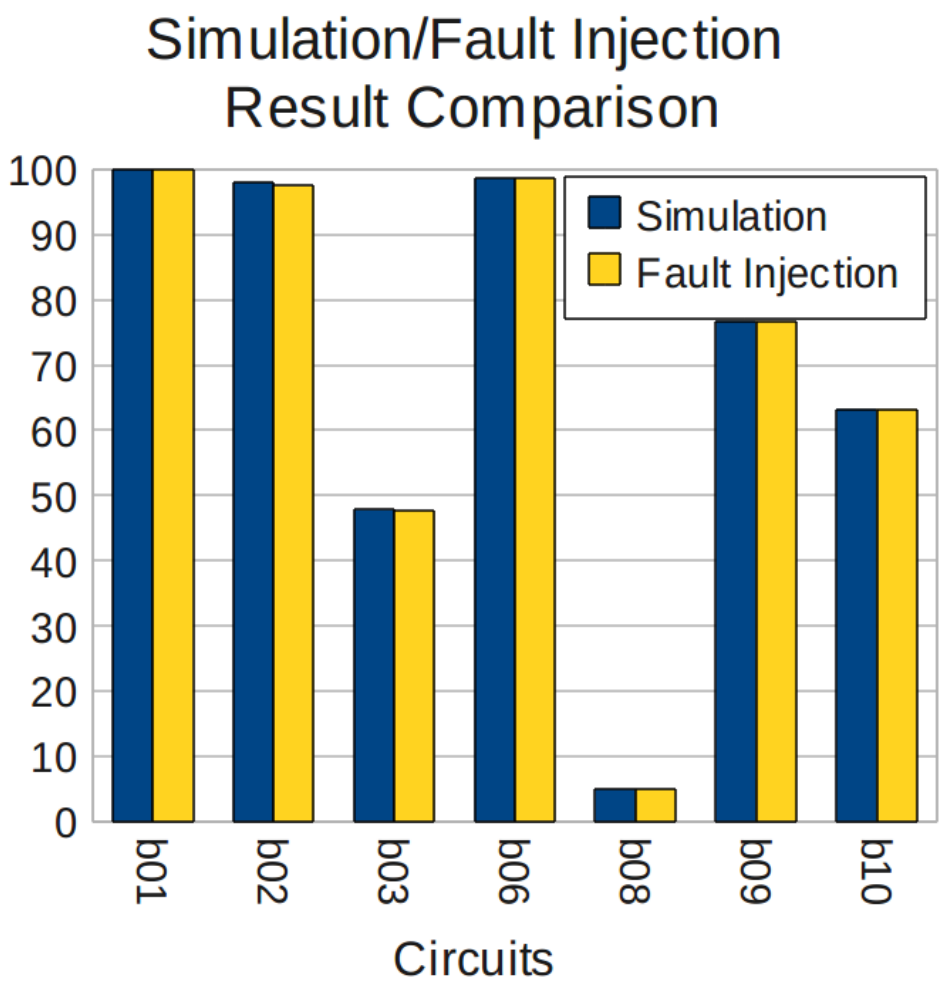
Some results: unexcitability analysis

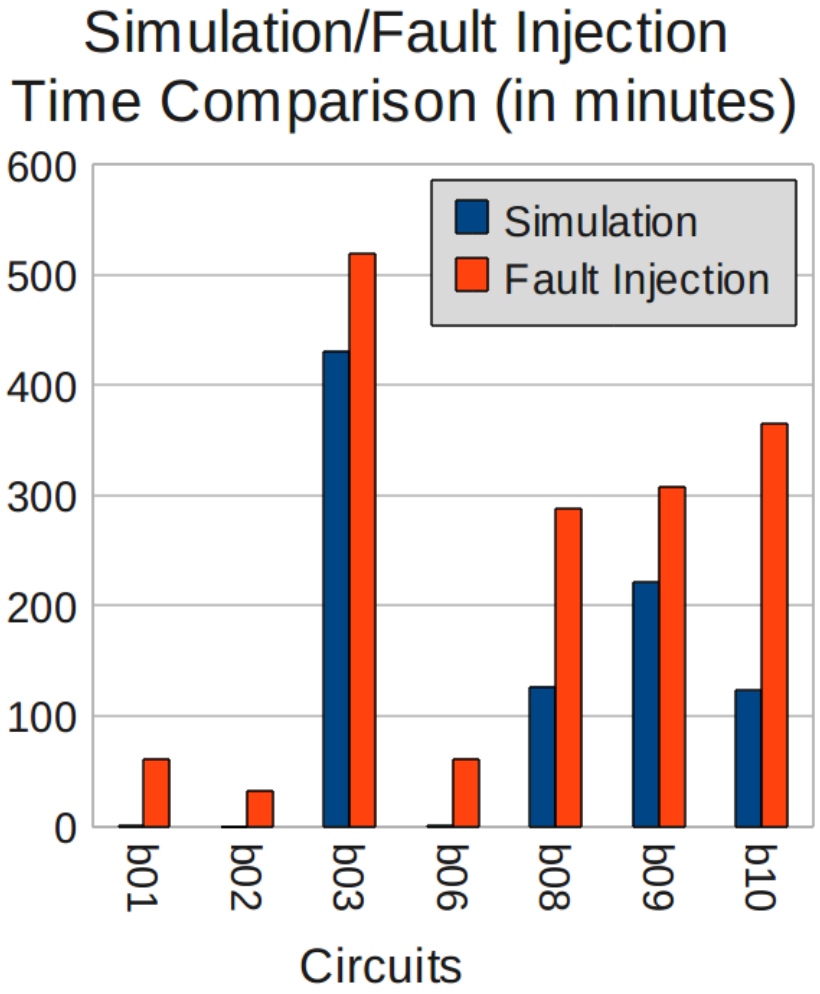




Up to 48% unexcitable SEUs in the logic

Some results: SEU simulation

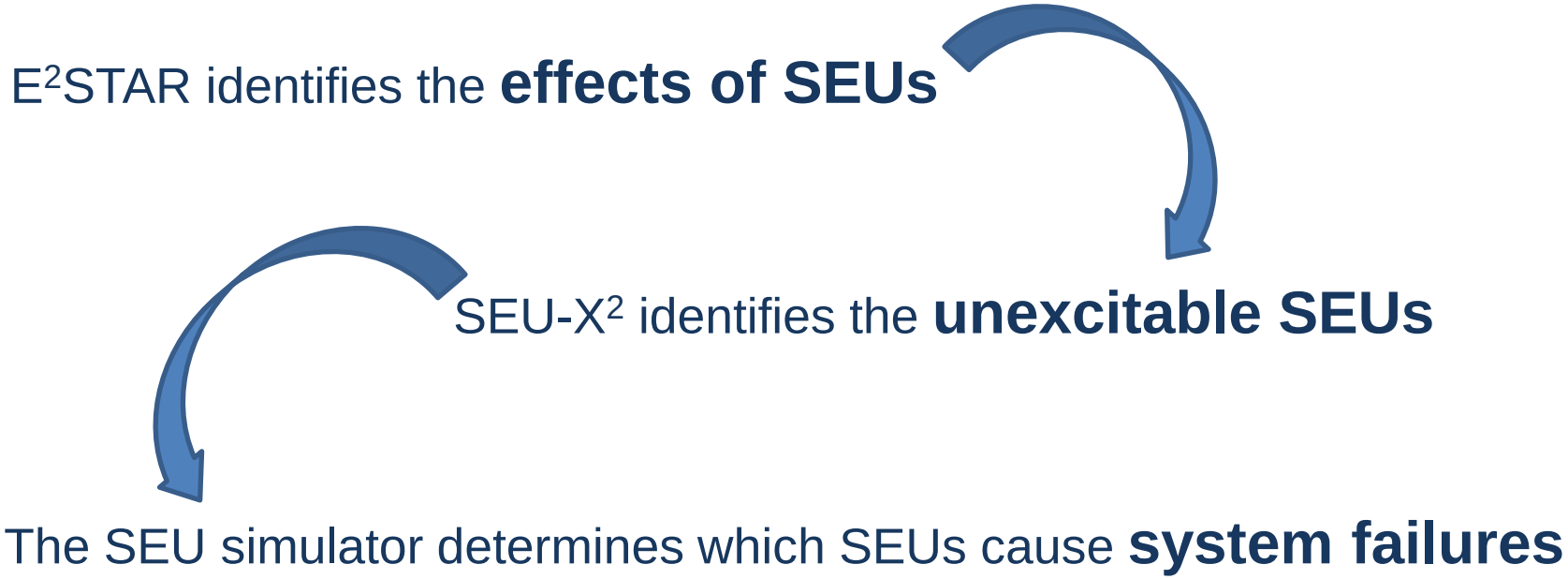




Max simulation error: 0.5%

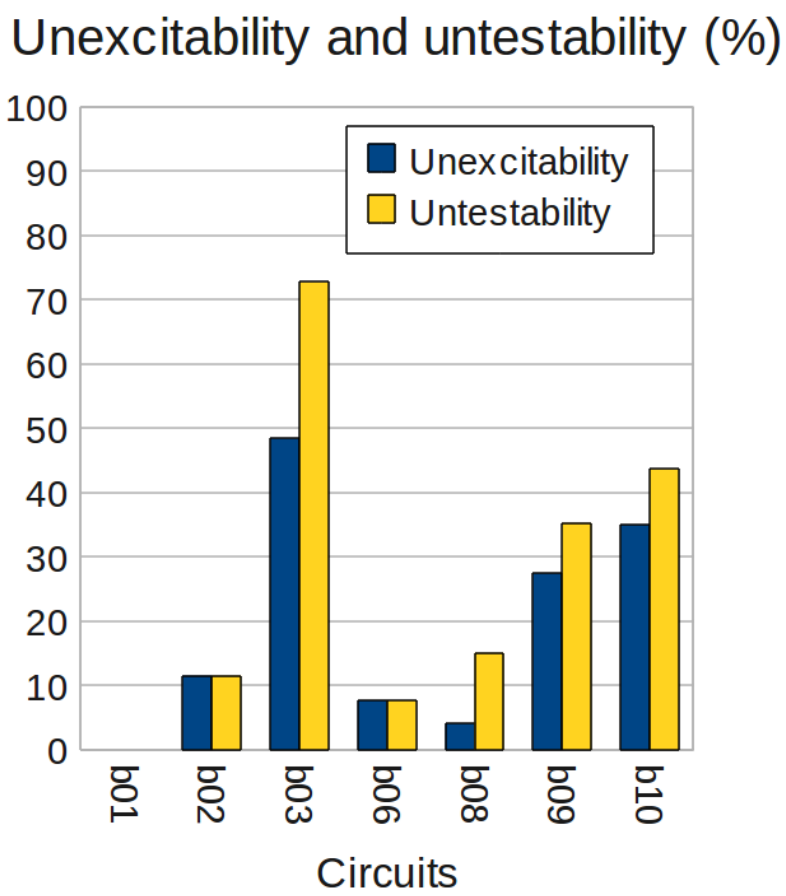
Summary

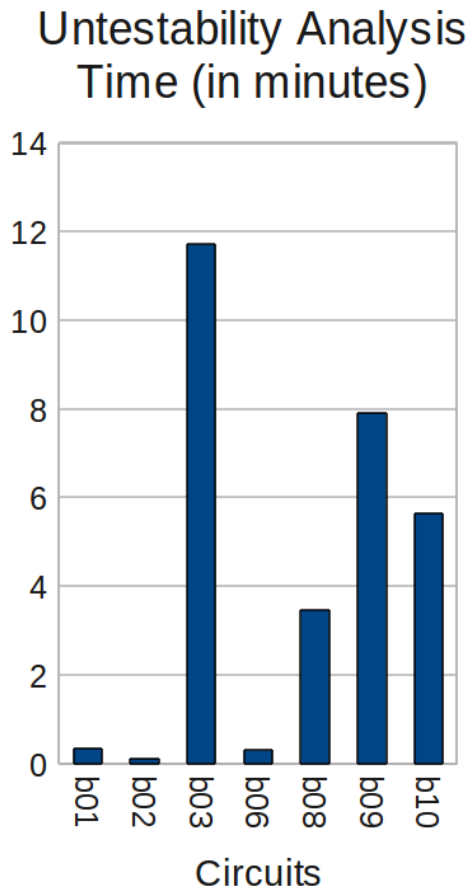
A CAD flow for **accurate** and **early** SEU sensitivity analysis



Future work: UniPi+PoliTo

- Extend the unexcitability prover
  - **Untestability analysis** (so far available only for SEUs in the logic) ➡ **No simulation required!**



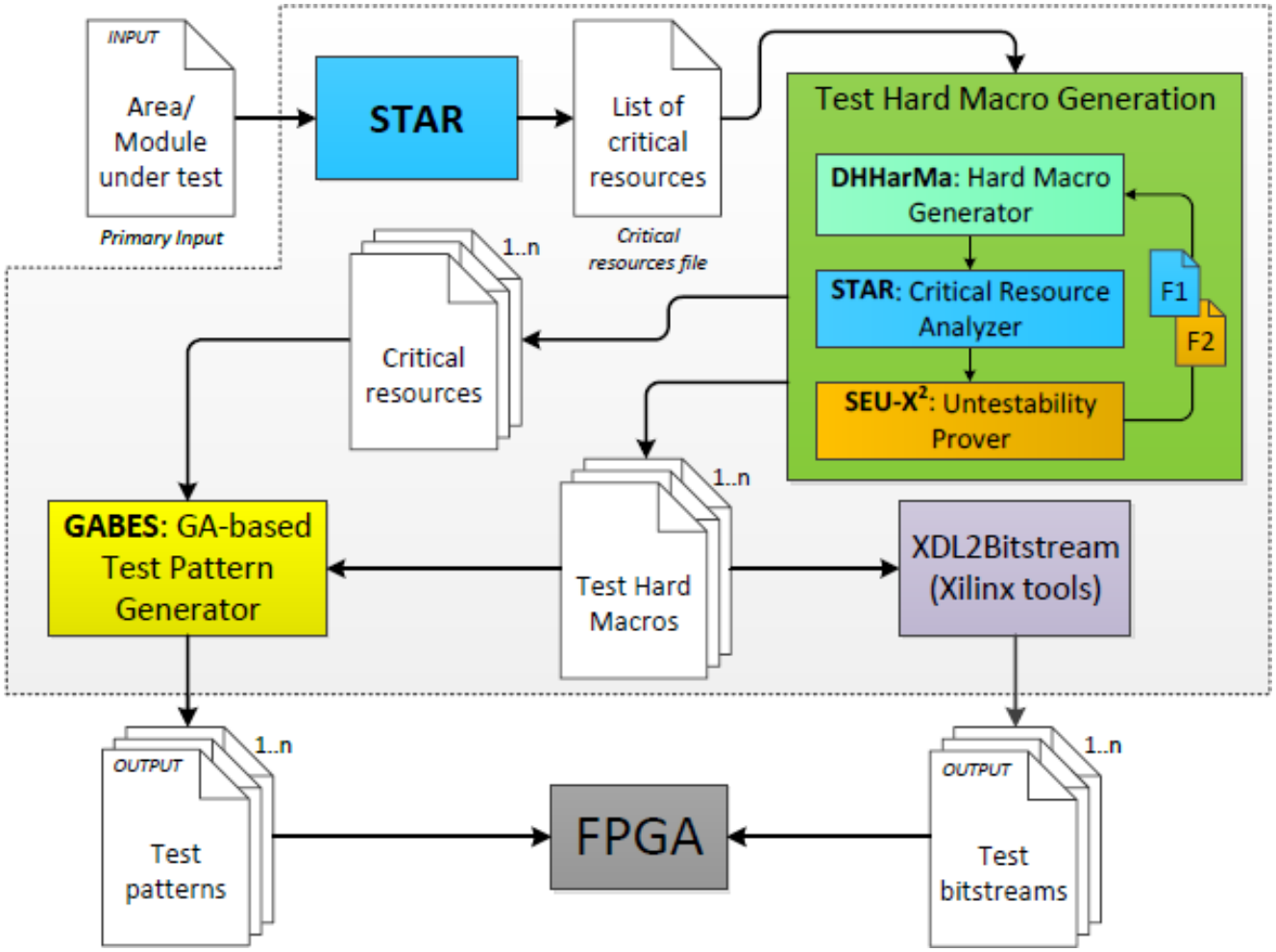


Future work: UniPi+PoliTo

- Extend the SEU simulator
  - **Probabilistic** fault injection
  - **Multiple SEU** occurrence

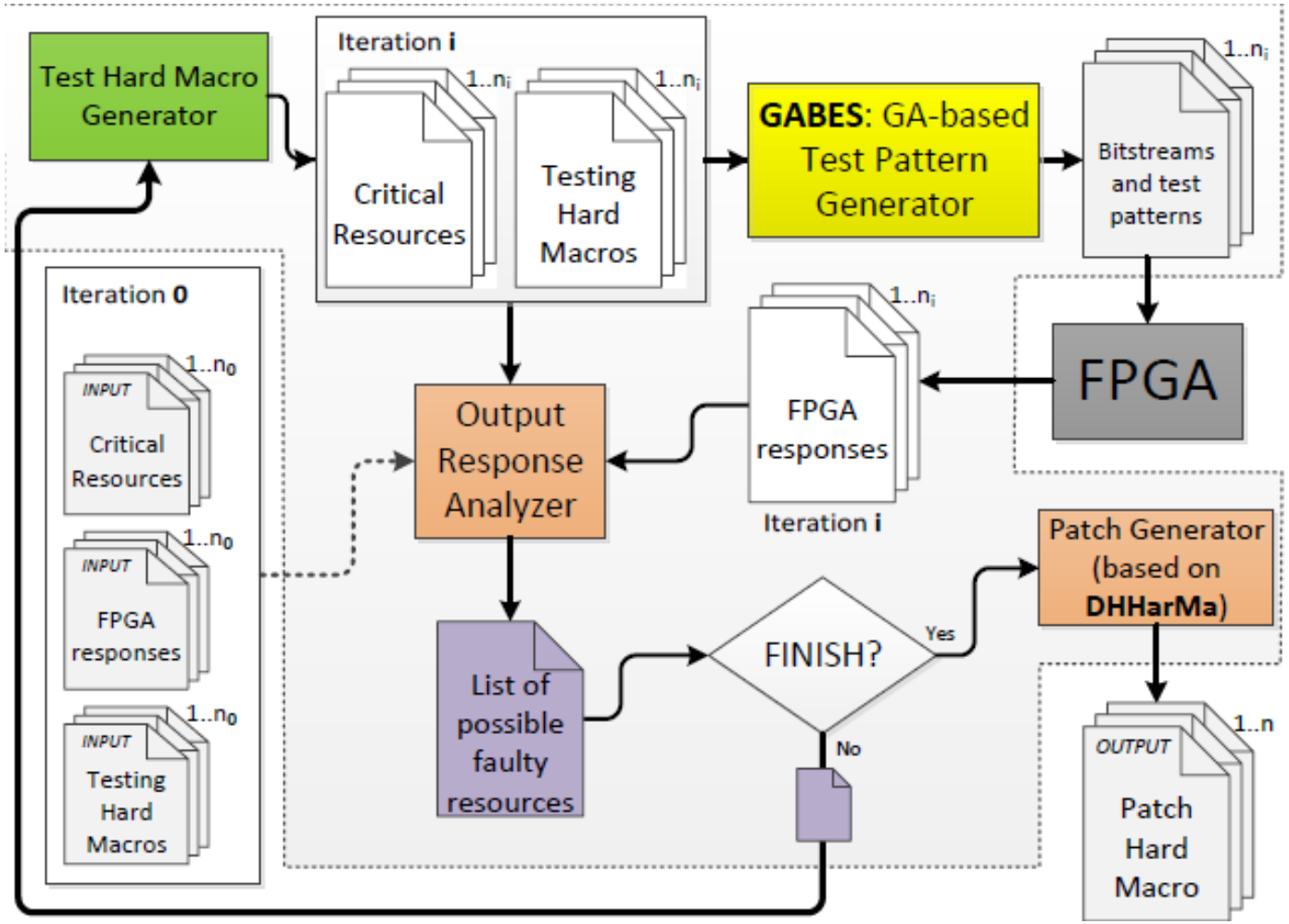
- Reproduce the functioning environment of the system
  - Assess the sensitivity to **SEU accumulation**

Future work: UniPi+PoliTo+UniBiel



On-line testing of permanent faults due to radiation

Future work: UniPi+PoliTo+UniBiel



Fault location identification & faulty resources patching

Thank you for your attention!

Questions?

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