Maya Group

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October 2012

Maya Group

- **Staff**: 117 people including 105 engineers
- **Turnover**: 9.3 M€ (3/31/2012)
- **Locations in France**: Grenoble, Aix-en-Provence, Sophia Antipolis, Toulouse, Valence, Paris
- **Strategy** : *"become a leader in the microelectronic component and embedded system design markets."*

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Fields of expertise

SOFTWARE & EMBEDDED SYSTEMS

System architecture
FPGA design, prototyping, emulation
Signal processing
Firmware & Middleware development
Driver development
OS and real time kernels : Android, Linux, Windows Mobile expertise
Object software Development

DIGITAL MICROELECTRONICS

Integrated circuit architecture (ASIC)
Modeling and simulation
Verification
Synthesis
Timing Analysis
Physical implémentation
Validation, testing
Packaging, SIP
CAD development & support

ANALOG MICROELECTRONICS

Architecture & Modeling
Analogue, RF & mixed signal design
Layout
CAD development & support
Physical Design Kit and library development
Validation, Testing
Packaging, SIP

MAYA TECHNOLOGIES
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psi electronics

Locations

***Paris** : On-site expertise*

***Grenoble** : Headquarters & general Design Center*

***Valence** : Embedded Software*

***Sophia** : Digital Design*

***Toulouse** : Critical Embedded Systems*

***Aix (Rousset)** : Analog Design*

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Maya's customers

Maya's offers

- **Technical Assistance on customer's site**: an answer to an urgent need of resources on a project.
- **Technical team on customer's site**: a complete Maya team, autonomously managed by a Maya project and/or team leader
- **'Externalized' Technical team**: a complete Maya team, autonomously managed in our locations
- **Design Centers**: project management as a package in our locations (commitment on deliverables, delays and cost, based on customer specifications)

IP 1553 : History

- First interface developped in years 2000 during a project aiming to implement GAM-T 103 services onto the 1553 bus

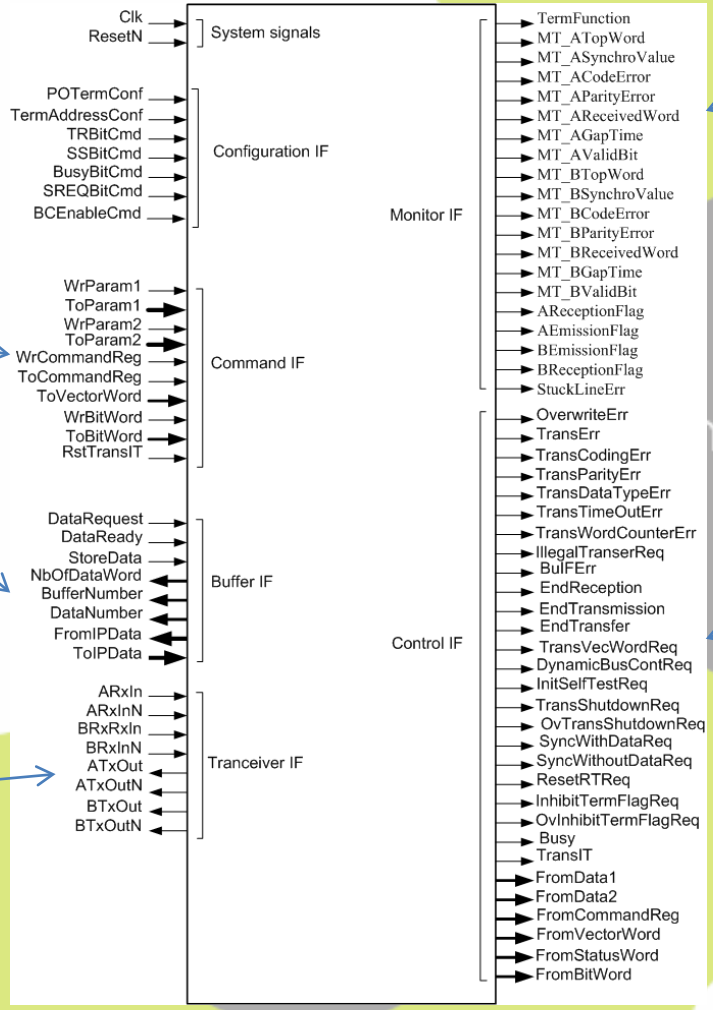
- Two macrocells have been derived from this project :
  - A Remote terminal macrocell
  - A Remote terminal/Bus Controller macrocell
- RT macrocell Selected by Thales Alenia Space for Globalstar. TAS participated to the first IP validation.

- The IP is distributed by ATMEL in its MG2-RT technology,

IP 1553 : presentation

- Developped in VHDL
  - Remote terminal version- MYA-53-RM2-IP
  - Remote terminal/Bus Controller version - MYA-53-BCRM1-IP
- Working freq : 12 MHz
- Full compatibility with MIL-STD-1553B notice II,
- Manages dual-redundancy,
- A rich interface gives an important Observability/commandability of the IP (Allows to design from the simplest to the more complex application)
- Verified according SAE Validation Test Plans
- Interface with all commercially available transceivers.

IP 1553 interface



Command register access

Memory style interface for data access

Bus interface Nominal + redondant

Monitor interface

Control signals

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IP 1553 : Using exemple 1

TM/TC interface

- **Only RT mode is used,**
- **Only transmit messages and receive messages of 1 word length to buffer 3 are allowed.**
- **For a receive message a CS16 with the received data word is transmitted onto the CS16 serial interface and operation results is acquired through AS16 serial interface,**
- **For a transmit message the last acquired operation results is transmitted onto the bus.**

IP 1553 : Using exemple 2

Implementation into a LEON 2 platform: ATMEL Project

- **Bus controller/Remote terminal capabilities**
- **Interface fully Command/Controlled via the APB**
- **1553 buffers mapped into the LEON2 memory and accessed in DMA by the interface(no SW intervention needed).**
- **Programmable interrupt generator**

IP 1553 : Verification

Compatibility with 1553 protocol requirements verification (AS4111 or AS4113: §5.2) has been verified :

- **By using DDC validation testsuites**
- **With VHDL testbenches (delivered with the IP)**

Compatibility with 1553 electrical requirements (AS4111 or AS4113: §5.1 and 5.3) :

- **Done by IP users on their final board.**
- **Weakness concerning the Sync reception has been corrected in 2010.**

MYA-53-BCRM2-IP : Licensing

The IP is licensed per project. The package includes :

- **A FPGA/ASIC gate level netlist,**
- **Some VHDL testbenches,**
- **The IP User Manual,**

The IP will be available in ATF technology through ATMEL in the form of a Hard Block.

Questions ?

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