SVOM mission: ATF280F/AT697F data processing for real-time GRB detection and localization

& ATF280E SpaceWire CEA IP recent developments


ESA, November 6 - 2012
**SVOM: Instrument**

**Gamma Ray Burst (GRB) trigger**
CXG (X/g camera)
CdTe, 4-250 keV
photon timing 10 μs

Franco-Chinese Instrument

ITAR, EAR exportation rules constraints

Real time GRB detection hardware based on
ATMEL AT697F/ATF280F components
On-board Gamma Ray Burst detection

Gamma Ray Burst (GRB)

Coded Mask

CXG camera 6400 Pixels

Photon events
(Pixel number, Hit time)

Real time complex analysis: processor

UTS

Detected GRB

Photon events

Logic device (FPGA)

Preprocessing & Formatting

Shared memory

Interruption

Processor Treatment

Detected GRB

Scientific Treatment Unit (UTS)
UTS architecture

Additional FPGA preprocessing: raw data buffers, counting per pixel (Read/Modify/Write), per camera zone, per energy. Sophisticated DMA.
UTS Data Processing Model

Compact PCI Backplane | XILINX V4 FPGA Board | AT697F CPU Board | PC (Host)

- Ethernet (TFTP ou NFS)
  - Config files
  - Result files

- Console (stdout)
  - Print output

- CPU monitor (grmon)
  - Load prog, run, status

- Injector board

Photon injection (CXG simulator)
ATF280F firmware design flow

UTS VHDL Design
Xilinx wrapper for ATF280F I/O (bibufrr, obufer..)

Synthesis, Xilinx P&R

Full system test on Data Processing Model

UTS VHDL Design
Atmel wrapper for Xilinx FIFO, RAM modules

Precision synthesis, IDS Atmel P&R

Post routing ATF280F VHDL net list with Standard Delay File timing

VHDL SIMULATION
Photon preprocessing logic

- **CXG Link 0**
  - CXG Link Emulator 0
  - CXG Link Control 0
  - CXG Link Arbiter

- **CXG Link 7**
  - CXG Link Emulator 7
  - CXG Link Control 7

- **CXG Clock**
  - ATF280F FPGA
    - Multiple Bus routing
    - Distributed Memory usage
      - (FIFO, RAM)

- **CPU Interrupt**
  - Raw Photons Buffer
  - Interrupt Controller

- **CXG Raw Data**
  - Data Processing & Routing
  - AHB Master Access

- **AHB Bus**
  - AHB / PCI Bridge
    - Modified Gaisler PCI_MT IP

- **AHB Bus**
  - AHB Slave Access
  - RAM Pointers
  - UTS Time Control
  - UTS Control & Status
  - Photon Counters 36x32-bit
Photon preprocessing logic

<table>
<thead>
<tr>
<th>Resources</th>
<th>ATF280F-MQFP352</th>
<th>XC4VLX100-10ff1513</th>
<th>ATFS450-MQFP352</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O</td>
<td>115</td>
<td>115</td>
<td>115</td>
</tr>
<tr>
<td></td>
<td>50%</td>
<td>11%</td>
<td>54%</td>
</tr>
<tr>
<td>FF</td>
<td>3147</td>
<td>3551</td>
<td>3147</td>
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<tr>
<td></td>
<td>22%</td>
<td>4%</td>
<td>14%</td>
</tr>
<tr>
<td>RAM</td>
<td>151 RAM Cells</td>
<td>11 RAMB16 176 RAM16x1</td>
<td>151 RAM Cells</td>
</tr>
<tr>
<td></td>
<td>17%</td>
<td>4%</td>
<td>10%</td>
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<tr>
<td>logic</td>
<td>8753 core cells</td>
<td>4337 LUTs</td>
<td>7866</td>
</tr>
<tr>
<td></td>
<td>for routing</td>
<td>for routing</td>
<td>for routing</td>
</tr>
<tr>
<td></td>
<td>61% 15%</td>
<td>4% 0.2%</td>
<td>34% 6%</td>
</tr>
</tbody>
</table>

Performances

| Frequency | 20 MHz* | 63 MHz** | 21 MHz* |

Atmel P&R tool: IDS 9.1.2a

* - 55°C to +125°C
** 0°C to +85°C

Only one global clock, PCI clock slowed down from 33 MHz to 20 MHz
I/O registers for all external interfaces
ATF280F 10% logic occupancy margin for future improvements
UTS processor board

Very similar to the engineering model - mechanics, thermal, components
UTS processor board (Laboratory Model)

- **PCI-bus** (ELS-FPGA board connector)
- **Test board**
  - ATMEL FPGA 20 MHz
  - Leon2 CPU 100 MHz Max
  - SDRAM 3D+ 512 MB
  - boot PROM 128 kB
  - application EEPROM 3D+ 4MB
- **connections**
  - LICE
  - SpaceWire
  - PPS
  - PCI-bus (ELS-FPGA board connector)
# UTS processor board (Laboratory Model)

<table>
<thead>
<tr>
<th>Functionalities - processor@66 MHz</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEON2 processor</td>
<td>✔</td>
</tr>
<tr>
<td>(console, DSU monitor, program execution)</td>
<td>✔</td>
</tr>
<tr>
<td>SDRAM</td>
<td>✔</td>
</tr>
<tr>
<td>Boot EEPROM</td>
<td>✔</td>
</tr>
<tr>
<td>Application EEPROM</td>
<td>✔</td>
</tr>
<tr>
<td>FPGA ATF280F</td>
<td>✔</td>
</tr>
<tr>
<td>(loading*, VHDL code execution)</td>
<td>✔</td>
</tr>
<tr>
<td>*hotline ATMEL request pending for FPGA/AT17LV10 PROM compatibility</td>
<td>✔</td>
</tr>
</tbody>
</table>

Isolate application EEPROM to allow SDRAM access @100 MHz

SpaceWire firmware to be added
UTS Design summary

• Full ATF280F firmware validated on the Data Processing Model - tightly coupled to the AT697F RT GRB trigger software

• Precision/IDS tool suit stable and easy to use - post routing simulation with modelSim SE works fine

• Major drawback of ATF280F is the final system frequency (penalties for Shadowgram RMW cycles in our application) - no major upgrade with the ATFS450
SpaceWireCEA IP Performance tests: configuration

Hardware:

Aerospace Development Kit
ATMEL (with ATF280E)

Software:

- VHDL synthesiser 'Precision RTL' 2008a1.11 OEM_Atmel from MENTOR
- Place and Route Atmel 'Figaro IDS V9.0.2'
- Programming tool 'SpaceProgrammer'
- Simulator 'ModelSim' from MENTOR

... and the SpaceWireCEA IP
SpaceWire CEA IP: Footprint

SpW IP config
FIFO Size: 9 x 32

Resource | Used | Utilization
--- | --- | ---
Combinational Cell | 576 | 4%
Sequential Cell | 198 | 1.4%
SpaceWire CEA IP: performance

<table>
<thead>
<tr>
<th>Rx \ Tx</th>
<th>10 MHz *</th>
<th>30 MHz **</th>
<th>50 MHz *</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>40 MHz</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>100 MHz</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>120 MHz</td>
<td>Fail</td>
<td>Pass</td>
<td>Fail</td>
</tr>
<tr>
<td>140 MHz</td>
<td>Fail</td>
<td>Fail</td>
<td>Fail</td>
</tr>
</tbody>
</table>

* Global clock input - ** Fast Clock
**SpaceWire CEA IP: effect of the temperature**

**Rx to Tx loop with Tx=30MHz**

<table>
<thead>
<tr>
<th>Rx freq</th>
<th>-20°C</th>
<th>0°C</th>
<th>+20°C</th>
<th>+50°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz</td>
<td>Data</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 MHz</td>
<td>Data</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>120 MHz</td>
<td>Data</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
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<td></td>
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</tr>
<tr>
<td>140 MHz</td>
<td>Data</td>
<td>Fail</td>
<td>Fail</td>
<td>Fail</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Frame generator with Rx=100MHz**

<table>
<thead>
<tr>
<th>Tx freq</th>
<th>-20°C</th>
<th>0°C</th>
<th>+20°C</th>
<th>+50°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 MHz</td>
<td>Data</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>50 MHz</td>
<td>Data</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>Time-code</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>