

New Features and IP Cores in the GRLIB IP Library

Jan Andersson

Aeroflex Gaisler

www.aeroflex.com/Gaisler

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- ▼ **1. Collection of reusable IP cores written in technology agnostic VHDL**
 - GRLIB tech. abstraction layer allows the same IP core to be implemented on any technology
- ▼ **2. Template designs for wide range of FPGA prototyping boards. ASIC templates also available.**
 - Template = SoC design + test bench
 - Template design configuration possible via GUI
 - ▼ Settings, enable/disable cores
 - ▼ Full customisation requires editing RTL
- ▼ **3. Script generation for EDA tools**

GRLIB: Complete Design Environment

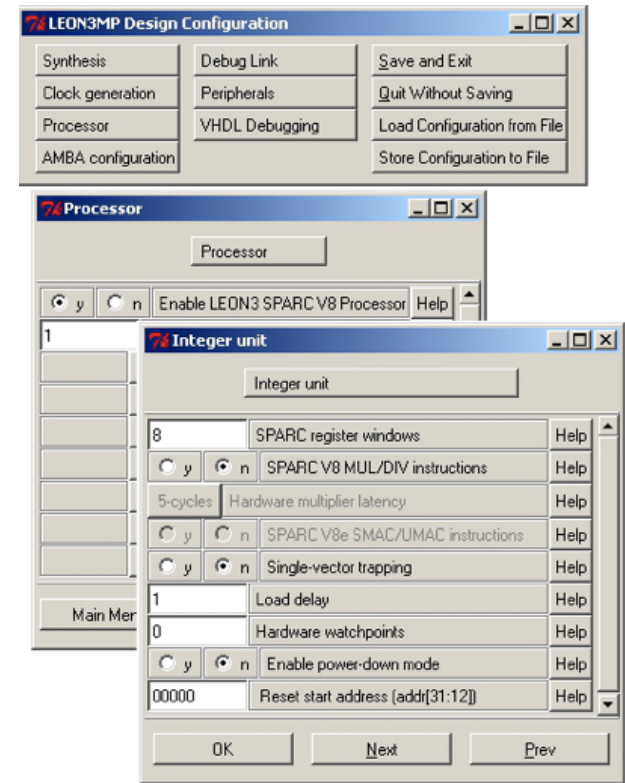
▼ IP

- Processors
- Peripherals
- Serial/Parallel interfaces
- Memory controllers
- AMBA 2.0 with PnP support
- Self-checking RTL

▼ Template designs for range of boards

▼ Portability between target technologies

- Technology maps for ASIC and FPGA



▼ Popular distributions

- GRLIB-GPL: LEON3, limited # of cores, no FT
- GRLIB-COM: LEON3, no FT cores
- GRLIB-L4-COM: LEON3/4, L2 cache, no FT
- GRLIB-FTFPGA: COM + FT cores, FPGA
 - ▼ Several combinations with SpW, FPU, 1553
- GRLIB-FT: FT for ASIC implementation

▼ FT-FPGA targeted at rad-hard programmable devices

▼ Ready-made most popular variants:

- grlib-ftfpga / -grlfpu / -grlfpu-spw / -grfpu-spw / -spw / -1553

- ▼ **Past: Netlist used for LEON3FT, SpW, FPU**
 - Producing and verifying netlists is costly
 - Subset of configurations available
 - Simulation time increase
 - Error injection inconvenient
- ▼ **Now: Replace netlists with encrypted RTL**
 - **Benefits**
 - ▼ One version per tool instead of multiple versions per technology
 - ▼ Simulation at same speed as cleartext RTL
 - ▼ All configuration options available
 - **Drawbacks:**
 - ▼ Tool costs, security

- ▼ **Support encrypted RTL**
 - Synopsys DC, Synplify, Xilinx ISE/Vivado, Mentor Model/QuestaSim/Precision, Cadence
- ▼ **Improved script generation**
 - Aldec Riviera-Pro, Alint, Xilinx Vivado, Altera Quartus
- ▼ **Support for Xilinx Vivado and PlanAhead**
- ▼ **Support for Xilinx 7-series FPGA**
 - Template designs for Virtex-7, Kintex-7 and Zynq development boards
 - Artix-7 also supported, currently no template design for development board

- ▼ **Improved support for new Altera devices**
 - Extend support for Quartus features
 - Additional template designs in development
- ▼ **Design and configuration guide**
 - Guideline document included with GRLIB
 - Defines "standard" LEON configurations
 - <http://www.gaisler.com/products/grlib/guide.pdf>
- ▼ **Add-on package for Virtex-5QV**

- ▼ **Existing IP can already today be implemented on V5QV**
- ▼ **Add-on package to GRLIB FT-FPGA created to simplify for users that want to use complete LEON3/GRLIB design**
 - Adds example/template designs, build targets and documentation
- ▼ **Main reasons for using LEON3/GRLIB:**
 - FT by design, no need to triplicate memories
 - Proven IP cores, get processor, SpW, 1553, .., from one vendor.

Virtex5 FX130 implementation #s

Table 1. LEON3FT MIN/GP/HP resource utilisation

Resource	LEON3FT with Minimal configuration	LEON3FT General-purpose configuration	LEON3FT High-performance configuration	Total available
Slice logic utilization				
Number of Slice Registers:	2659 (3%)	5696 (6%)	11157 (13%)	81,920 (100%)
Number of Slice LUTs:	6913 (8%)	12295 (15%)	25202 (30%)	81,920 (100%)
Slice Logic Distribution				
Number of occupied Slices:	3302 (16%)	6399 (31%)	11751 (57%)	20,480 (100%)
Number of LUT Flip Flop pairs used:	7537	14235	28806	
Specific Feature Utilization				
Number of 36k BlockRAM used:	4	6	4	
Number of 18k BlockRAM used:	4	16	18	

- ▼ Also includes GPTIMER, UART, IRQCTRL, AHBUART, AHBSTAT and FTMCTRL
- ▼ LEON/GRLIB SoC: 8 to 30% of FPGA

▼ Virtex-5QV add-on summary:

- Template design with LEON3FT, FTMCTRL, PCI, SpW, CAN, 1553, Ethernet, system peripherals
 - ▼ Select between GR-PCI-XC5V and custom 5QV
- Template design with LEON3FT, FTDDR2SPA, PCI, Ethernet, system peripherals
 - ▼ Select target device between QV and COM device, pinout for Xilinx ML510 development kit
- Documentation
- Make targets for
 - ▼ Pre-XTMR flow, TMRTTool, XTMR flow
- Users can select between our CLI flow and Xilinx GUI flow

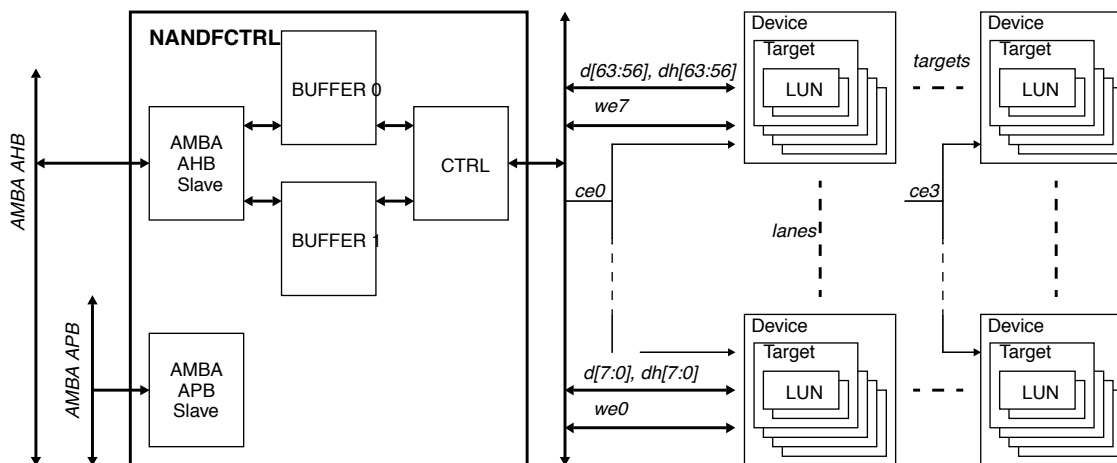
▼ What is new IP to you?

- Following slides gives a quick overview of some of our new iP
- GRLIB IP Core User's Manual available from <http://www.gaisler.com> lists all available IP

▼ Removed IP: ATACTRL, AC97, AHBCTRL_MB, HAPS and GE template designs, CoreMP7 support, ...

▼ NANDFCTRL – NAND Flash controller

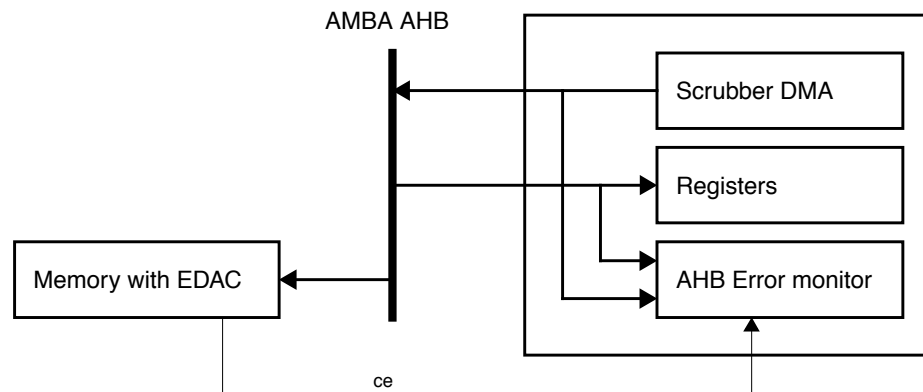
- Bridge between ext. NAND Flash and AMBA



Note: One device might have more than one target, using one chip enable signal for each target. This will reduce the number devices that can be placed horizontally in the figure. All devices (and the internal targets) placed vertically in the figure belong to the same chip enable signal, with individual write enable signals controlling each 8-bit/16-bit data lane.

- ONFI 2.2, EDAC, memory maps internal buffers

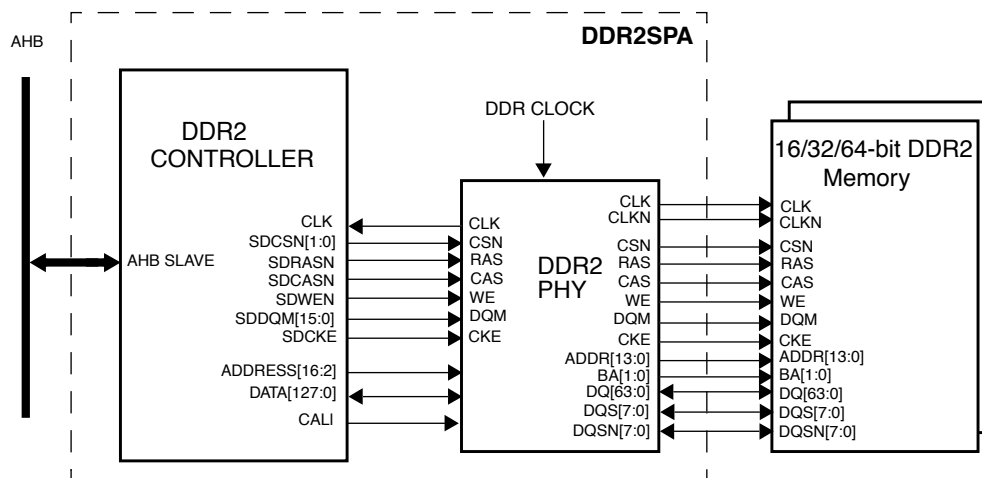
▼ Hardware memory scrubber



- Offloads processor
- Allows on-line code switch together with FTDDR2SPA memory controller
- Useful for memory initialization

▼ DDR2SPA-FT – Fault-tolerant DDR2 SDRAM controller

- Use with hardware memory scrubber to achieve on-line code switch



- 64/32/16 data bits, 32/16/8 check bits

- ▼ **AHB/AHB bridge with access protection and address translation**
- ▼ **Masters placed in groups.**
 - Each group can be disabled, pass-through or be associated with a protection data structure
- ▼ **Protection IOMMU or APV (global setting)**
 - **APV – Access Protection Vector (bit vector)**
 - ▼ **Access protection only**
 - **IOMMU – One-level page table**
 - ▼ **Access protection**
 - ▼ **Address translation**

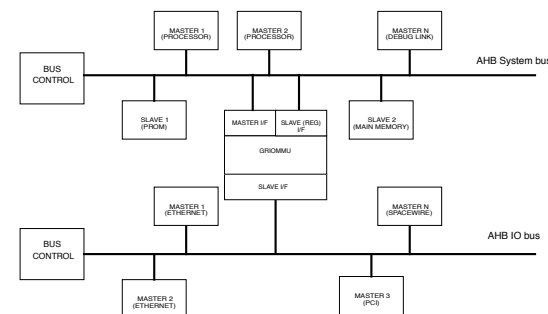


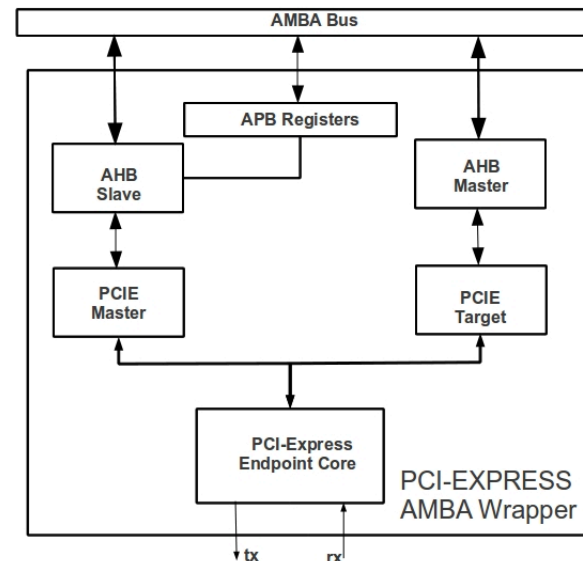
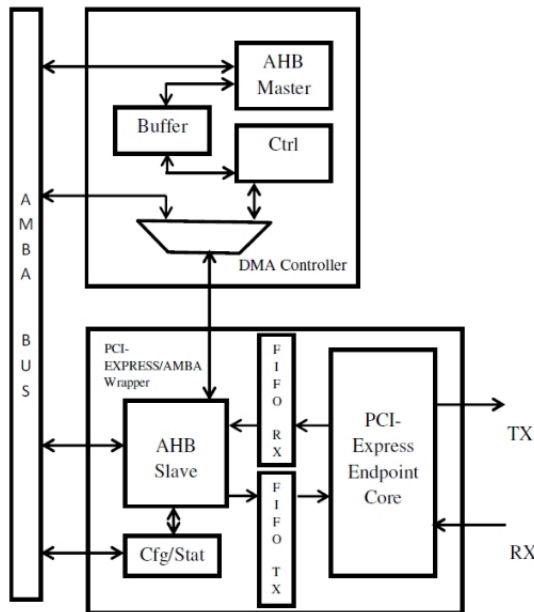
Figure 156. System with core providing access restriction/address translation for masters on AHB IO bus

▼ MMA – Memory mapped AMBA

- Attach companion device via memory-mapped IO interface (UT699, UT699e, UT700)
- Provides bridge between SRAM/PROM/IO bus to companion device's AMBA system
- Low complexity interface (compared to RMAP)
- Acts as a master on AMBA bus
- Supports multiple banks, each connected to a separate chip select. Programmable waitstates, or bus ready function
- Propagates AMBA ERROR response on bus error signal
- Available on request

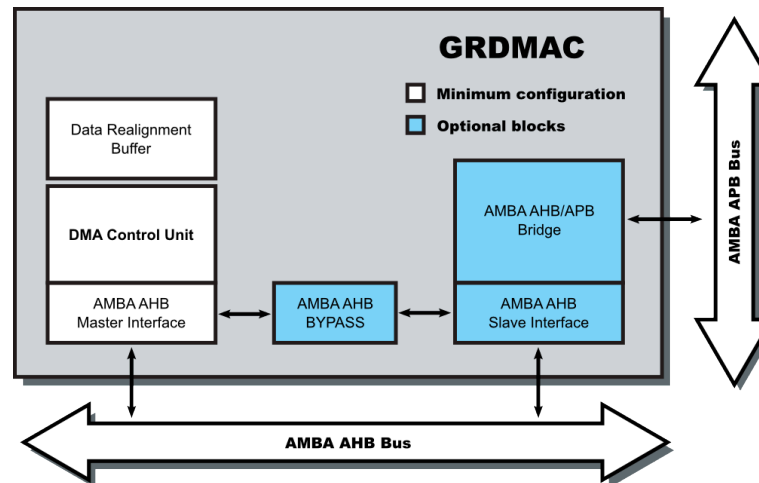
▼ PCI Express controller

- Target/Initiator, Initiator with DMA
- Currently only for Xilinx devices
 - ▼ Spartan 6, Virtex 5/6
 - ▼ Xilinx 7-series can be supported



▼ GRDMAC – DMA controller

- Direct-Memory-Access (DMA) operations
- Multiple channels controlled by descriptors in main memory, single operations possible via register interface
- Will provide DMA functionality to cores such as UART, SPI, I2C, GPIO, ..



▼ **AHB2AVL – Async. AHB to Avalon adapter**

- Designed for use with memory controllers
- Fixed size bursts with byte enabled, read data valid signaling
- Separate AHB and Avalon clock domains

▼ **AHBSWA – Wide bus adapter**

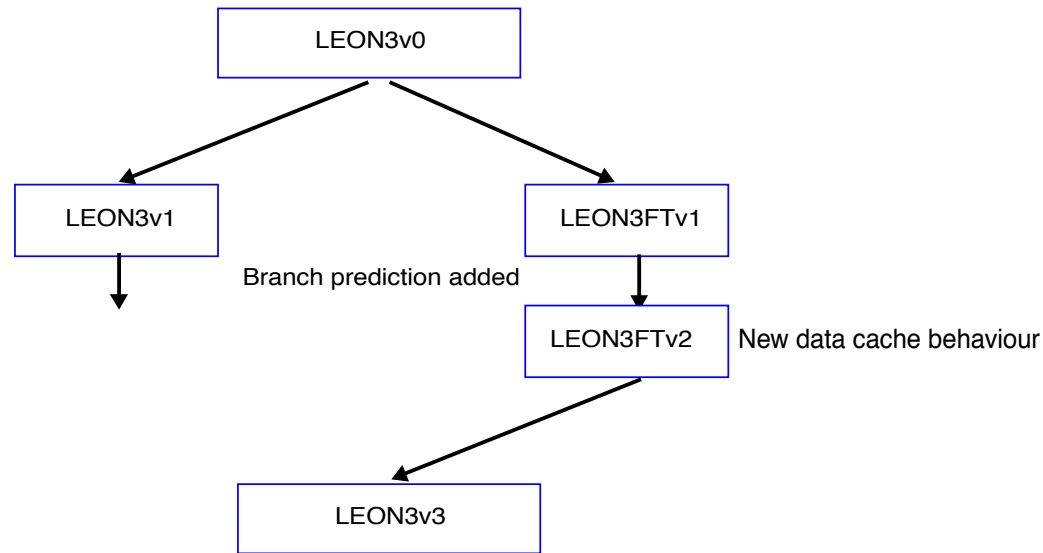
- Convert 64/128/256-bit accesses to 32-bit bursts
- Pass-through for 32-bit bursts
- Improves timing by acting as pipeline stage between slave and bus

- ▼ **Improved JTAG debug link (AHBJTAG)**
 - Allows TCK frequency > AHB frequency
 - Primarily for ASIC designs that power-up with a ~1MHz system clock
- ▼ **GRRT – Minimal "embedded RT" IP core**
 - Used to develop custom (hard) RT terminals
 - Contains 1553 codecs and RT protocol logic
 - User adds attaches logic using simple synchronous interface
 - 1150 cells on Microsemi RTAX

- ▼ **GRLIB IP Library User's Manual**
 - Describes IP library tool support and infrastructure
 - <http://www.gaisler.com/products/grlib/grlib.pdf>
- ▼ **GRLIB IP Core User's Manual**
 - IP core documentation
 - Lists all IP in table form and indicates in which distribution(s) the IP is included
 - <http://www.gaisler.com>
- ▼ **Inquiries:**
 - sales@gaisler.com

Thank you for your attention.

EXTRA SLIDES



UT699
LEON3-RTAX

GR712RC

UT699E/UT700
FT-FPGA

- ▼ **No new extensions planned**
- ▼ **Best choice for most applications**

- ▼ **Currently used in several commercial projects**
 - Mobile, crypto devices, ...
- ▼ **FT in NGMP (ESA)**
 - <http://microelectronics.esa.int/ngmp/>
- ▼ **Quad-core development board available:**
<http://www.gaisler.com/gr-cpci-leon4-n2x>
- ▼ **Several extensions planned to be rolled out during the coming months**