Simulation of the INL error of the Dual−Slope ADC. 16 bits, 100 MHz
INL Error (LSBs)
Input Voltage (V)
1
0.5
0
−0.5
−1
−1.5
−2
−2.5
−3
−0.03
−0.025
−0.02
−0.015
−0.01
−0.005
0