2nd ESA IP-Cores Day – 16/09/2013

**Roundtable Topics**

At the end of the presentations a roundtable was organized to discuss about the current status of the ESA IP-Cores service. The following topics were addressed as input to the discussion:

**Technical Aspects**

1. Additional IP-Cores to be added?
2. Major issues for specific IP-Cores
3. Bus system support
   * Is AMBA APB/AHB enough?
4. Technical documentation
   * Issues with the documents currently provided with the IPs?
   * Any other documents needed?
5. Source code quality
6. Test benches / simulation scripts
7. Precompiled models
   * Would it be useful if we provided simulation models for free before license signature?
8. IP version control
9. Inclusion of Analog IP Cores in ESA offer

**Administrative Aspects**

1. ESA IP-Cores Website
   * Is the information provided enough?
2. Comments on the Licensing Scheme
   * Clauses of the standard license
   * Fees
3. Interface to the user
   * Latency in processing an IP request
   * Format of IP-Core delivery
4. Communications
   * Adequate Technical Support
   * Mailing-lists / newsgroups?

**Roundtable Summary**

The main points raised in the roundtable were the following:

1. Some of the developers of IP-Cores which are part of the ESA IP-Core offer feel that it is not clear which type of warranty ESA gives to the licensees of the ESA IP-Cores and which is the liability of the IP-Core developer in case problems are encountered by the licensee during the use of the IP-Core.

*The position of ESA is clearly expressed in Article 11.1 of the ESA IP-Cores license, here reported:*

NO WARRANTY ON IP-CORES. Licensor gives no warranty nor guarantee whatsoever as to the adequacy or suitability of the licensed synthesizable HDL IP-Cores and shall not be held liable for any direct, indirect nor consequential damages. Use of the licensed synthesizable HDL IP-Cores by Licensee is made fully at Licensee’s own risk.

*This means that it is the IP-Core user responsibility to make sure that the licensed information (i.e. the IP-Core) is suitable for his/her needs and that it does not contain issues, faults, bugs, errors, etc. which might impair a successful use of it. Neither ESA nor the owner of the IP and the original developer are responsible orcan be held liable for any problems related to the use of the licensed IP-Core.*

1. Interest was expressed in the use of ARM-based processor cores for low power applications.

*ESA recognizes the fact that ARM-based microprocessors are gaining a larger and larger market share especially in the embedded, low power domain. It is also noted, though, that the LEON family of microprocessors appropriately fulfils the current needs of the European Space Market with multiple architectures going from simple, low power ones to complex multi-core designs.*

*ESA is anyway investigating the possibility of adopting architectures different from the LEON ones (among which there is ARM) for some of the future processor designs, especially for what concerns low-power designs.*

1. Interest was expressed in having simple but widely used interfaces (such as SPI and E2C) available as ESA IP-Cores.

*The need for IP-Cores of such interfaces is recognized by ESA and it will be taken into account during the selection of the new IP-Cores to be added to the ESA IP-Cores offer in the future.*

1. There were some complaints about the quality of the documentation shipped with the IP-Cores, often inferior to what expected from commercially available IP-Cores. Self-standing datasheets are not available for some of the IP-Cores in our offer. Documentation is also reported to be often not clear with respect to:
   * which are the technology dependent parts of the IP-Core and
   * the clock and reset structures (to be updated in relation to the specific target design).

*ESA recognizes that for some of the ESA IP-Cores the documentation does not have the same quality level that for commercial IP-Cores; often the documentation provided consists of parts of the deliverables used by ESA to monitor the development process instead of being self-standing datasheets and user manuals.*

*ESA will take these suggestions for improvements into account for future IP-Core developments.*

1. It was expressed the need to clearly document which quality process was followed during the IP-Core development, in particular in relation to the ECSS-Q-ST-60-02C.

*ESA acknowledges the demands of projects for an assessment of the process followed during the development of the IP-Core. The user manual will contain, for newly developed IP-Cores one page describing the process followed for its development in relation to the ECSS-Q-ST-60-02C standard.*

*For what concerns already existing IP-Cores, ESA can provide, on request, a list of the missions in which the IP-Core was used, to indicate its flight heritage. For these IP-Cores no specific additional documentation will be produced to document their development process.*