

Analogue and Mixed-Signal IP- Cores for Space: Status and Challenges

R Jansen
TEC-EDM/ESTEC/ESA

- Introduction
- Demand
- Standard IC Development
- Issues – Development Risk
- Satellite Specific IC Development
- Issues – Integration Platform
- Status
- Challenges
- Conclusion

What have all these satellites in common?



Alphasat



Galileo IOV



Picosat



Femtosat

The functionality and performance of the satellites is heavily constrained by **Mass**, **Size** and **Power**.

The development is heavily constrained by **Costs**.

More than half the payload electronics weight is related to analogue, mixed-signal, radio frequency and power electronics.

How can functionality and performance increase at reduced cost, mass, size and power?

Digital Electronics

The down scaling of digital electronic circuits provides for constant **Mass**, **Size** and **Power** consumption increased functionality in terms of processing bandwidth. i.e. scaling from 180nm CMOS to 65nm CMOS increases the processing power by a factor 10.

For increased functionality the availability of IP-Cores keeps the development **Cost** within bounds.

Digital Interfaces

The increased processing power requires also higher input/output data rates. The bandwidth and energy efficiency of the digital interfaces increases also for constant **Mass**, **Size** and **Power** consumption with down scaling; discrete TM/TC are replaced by buses, low power CAN is challenging MIL1553, SpF is introduced to overcome the bandwidth limitations of SpW.

Can the increased input/output data rates also be met by analogue inputs and outputs at constant or reduced Mass, Size and Power consumption?

Analogue Interfaces

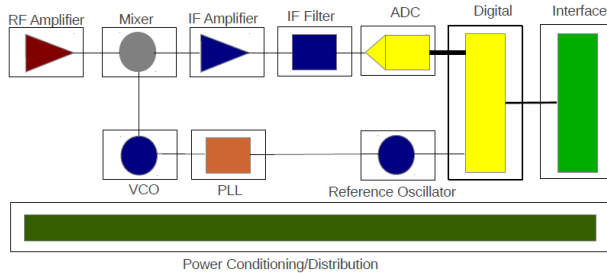
The number of analogue interfaces, types and required accuracy is slowly rising

With the current available components the increased data rates for the digital can not be provided at constant **Mass**, **Size** and **Power** consumption.

For **reduced sensitivity** the bandwidth can be increased for converters at constant **Mass**, **Size** and **Power** consumption

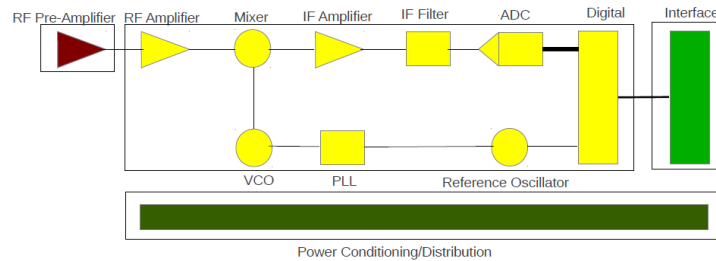
For **increased sensitivity** only integration offers the means to meet increased bandwidth at constant **Mass** and **Size**. New circuit designs and processes are required to increase performance and reduce the **Power** consumption.

Analogue and Mixed-Signal IP-Cores are required to facilitate integration and keep development **Cost** within bounds.



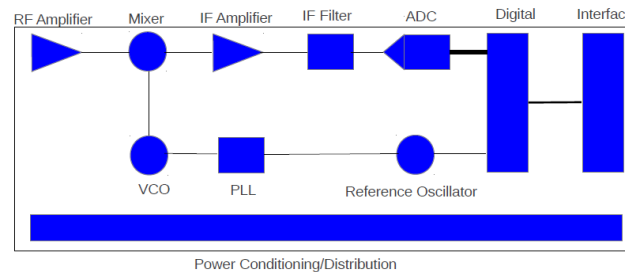
L Band Receiver - Discrete

■ GaAs ■ Bipolar ■ BiCMOS ■ SOI CMOS ■ CMOS ■ HV CMOS Component



L Band Receiver - Integrated 1

■ GaAs ■ Bipolar ■ BiCMOS ■ SOI CMOS ■ SiGe BiCMOS ■ CMOS ■ HV CMOS Component



L Band Receiver - Integrated 2

■ GaAs ■ Bipolar ■ BiCMOS ■ SOI CMOS ■ SiGe BiCMOS ■ CMOS ■ HV CMOS Component

Mixed-Signal Technology Performance Improvements

ADC performance over time and per technology node levels

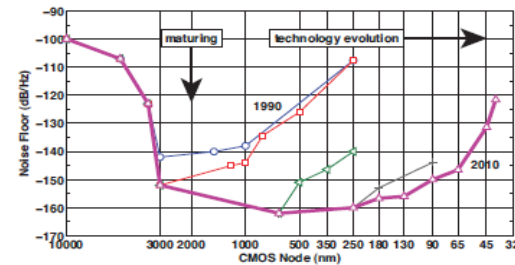
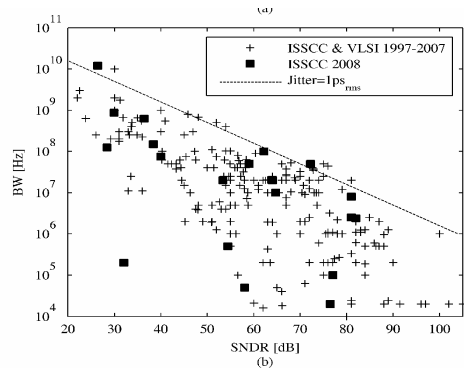
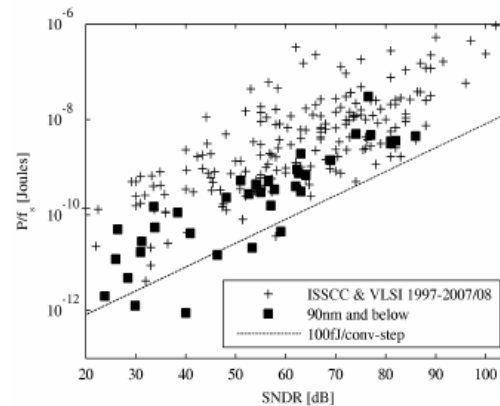


Figure 3. Relative noise floor vs. CMOS node. State-of-the-art envelopes at 1990 (○), 1995 (□), 2000 (<), 2005 (+), and 2010 (△) illustrate the evolution of CMOS.

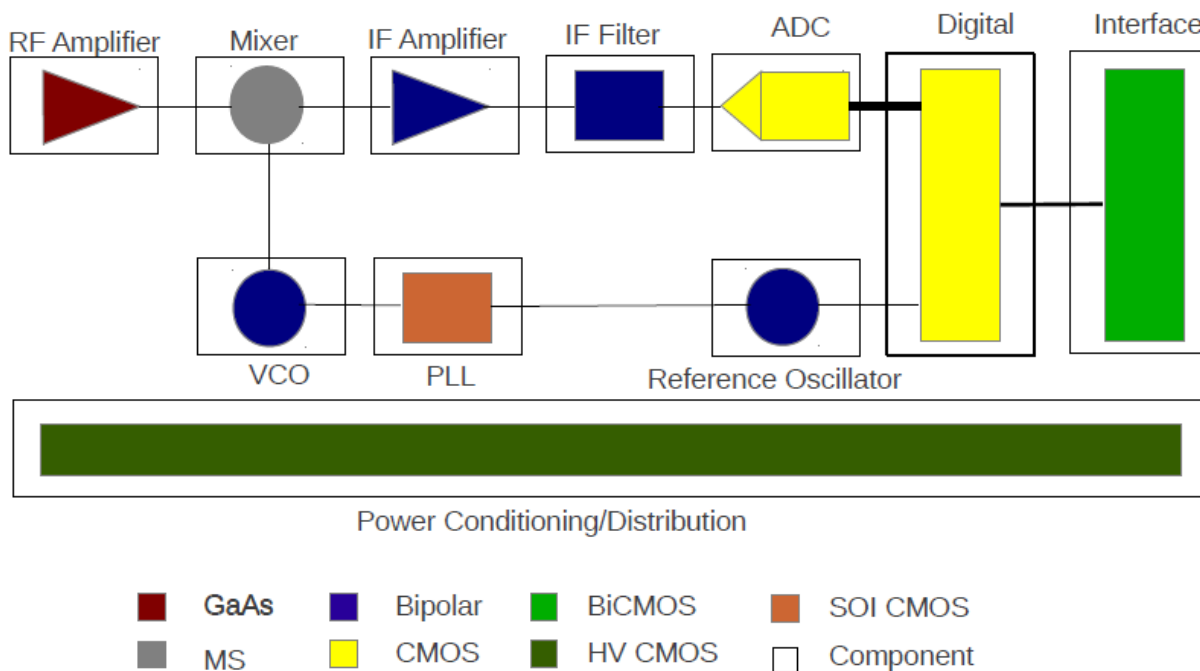
ADC power consumption reduces over time with node.



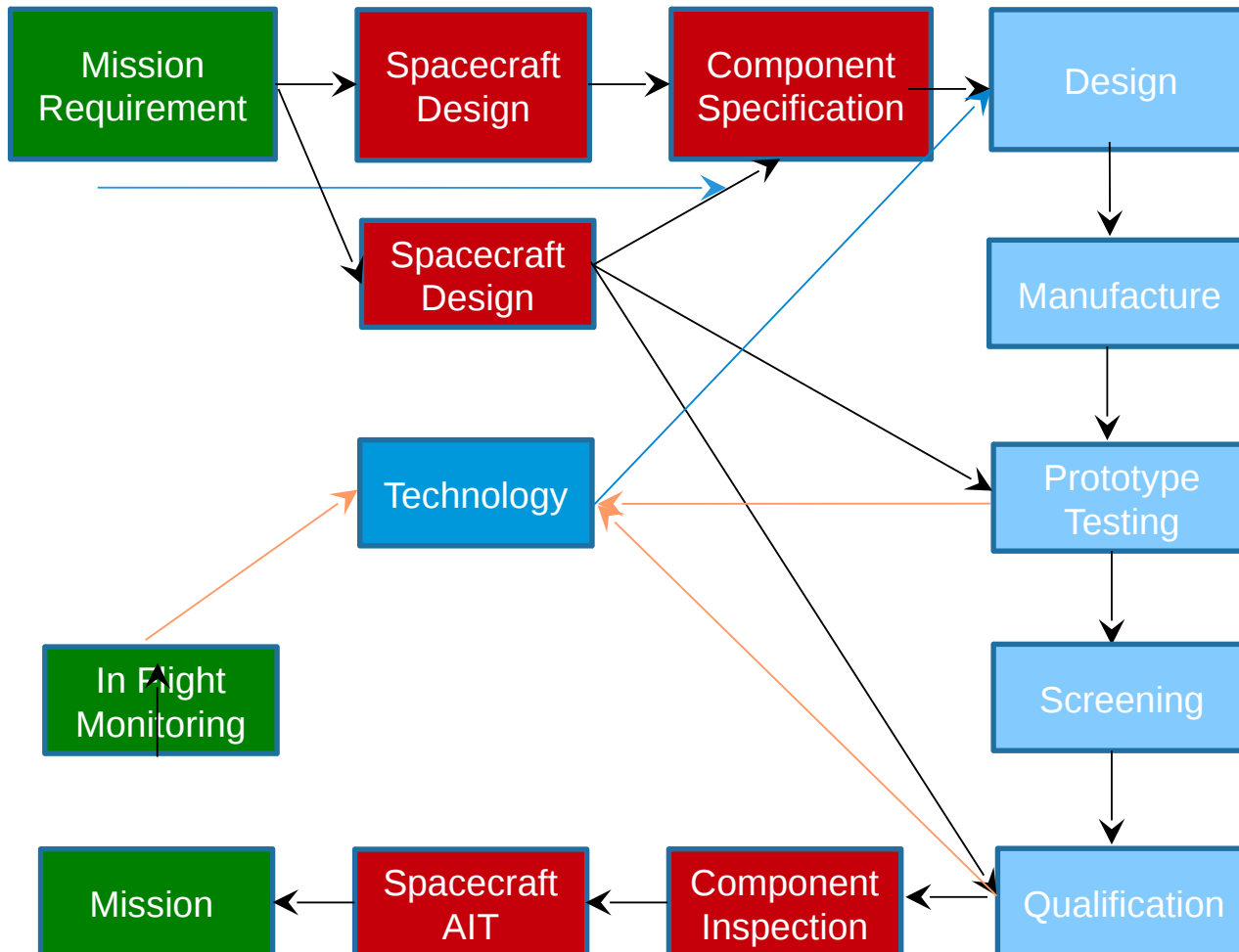
Number of converters can be increased with technology node at constant Mass, Size and Power provided

Analogue IP-Cores are available for integration (AMICSA 2012)

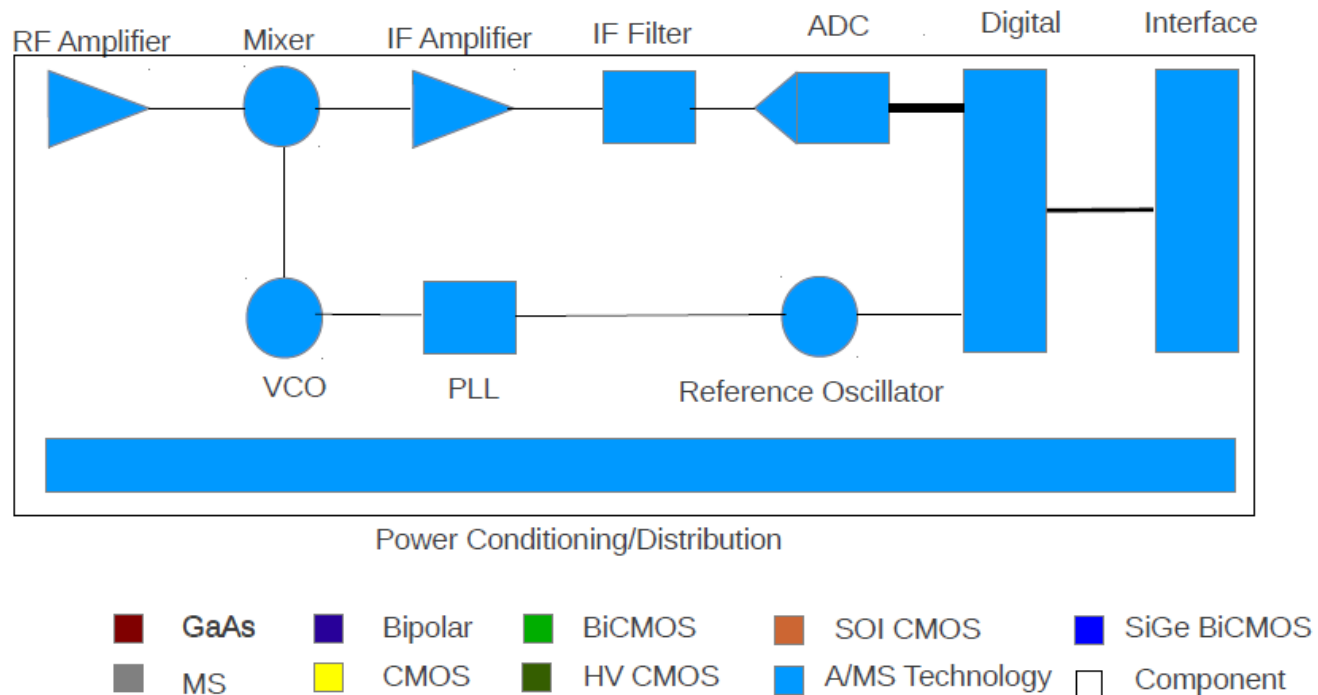
L Band Receiver - Space (Discrete)



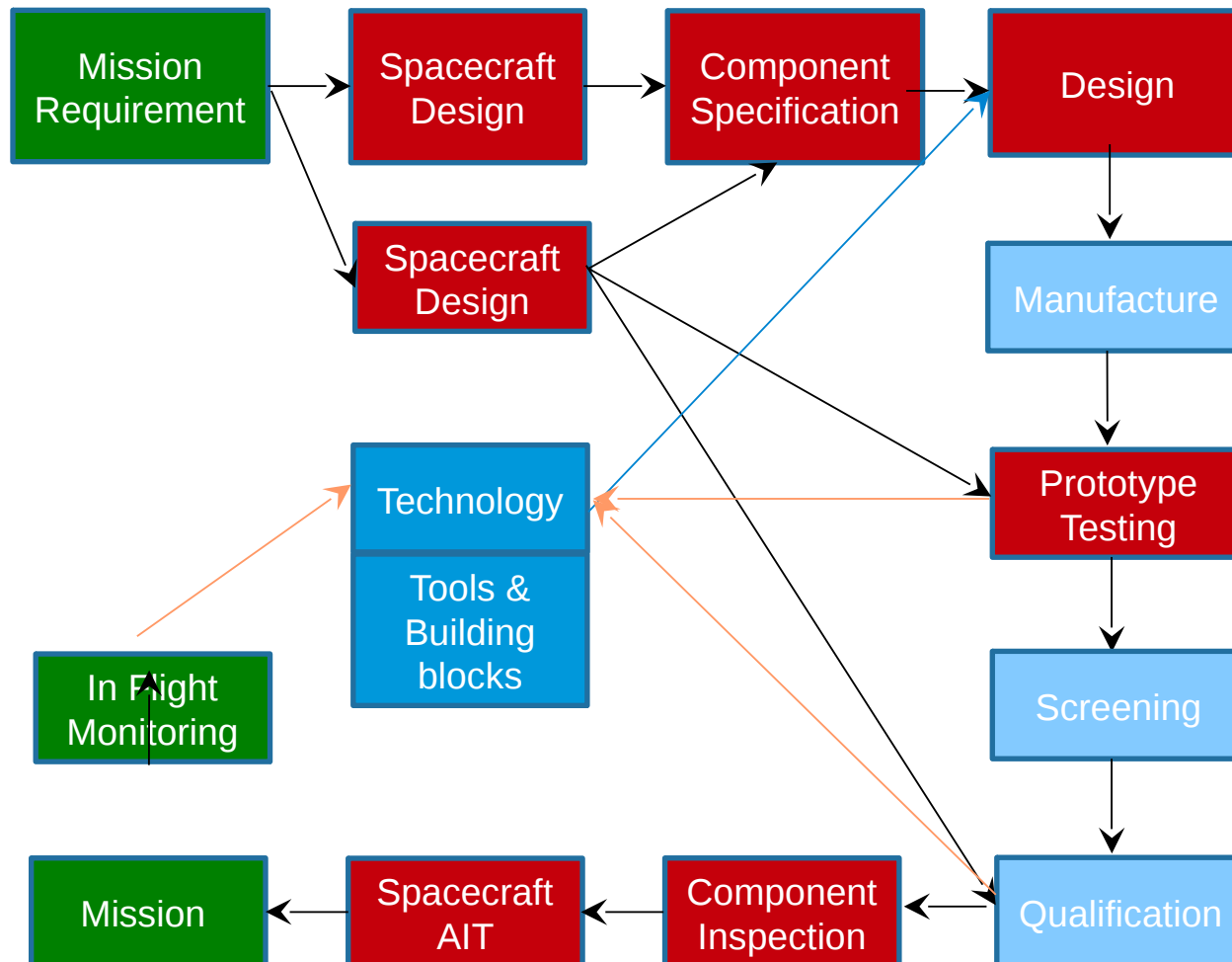
Standard Space Development



L Band Receiver - Space



Standard IC Development



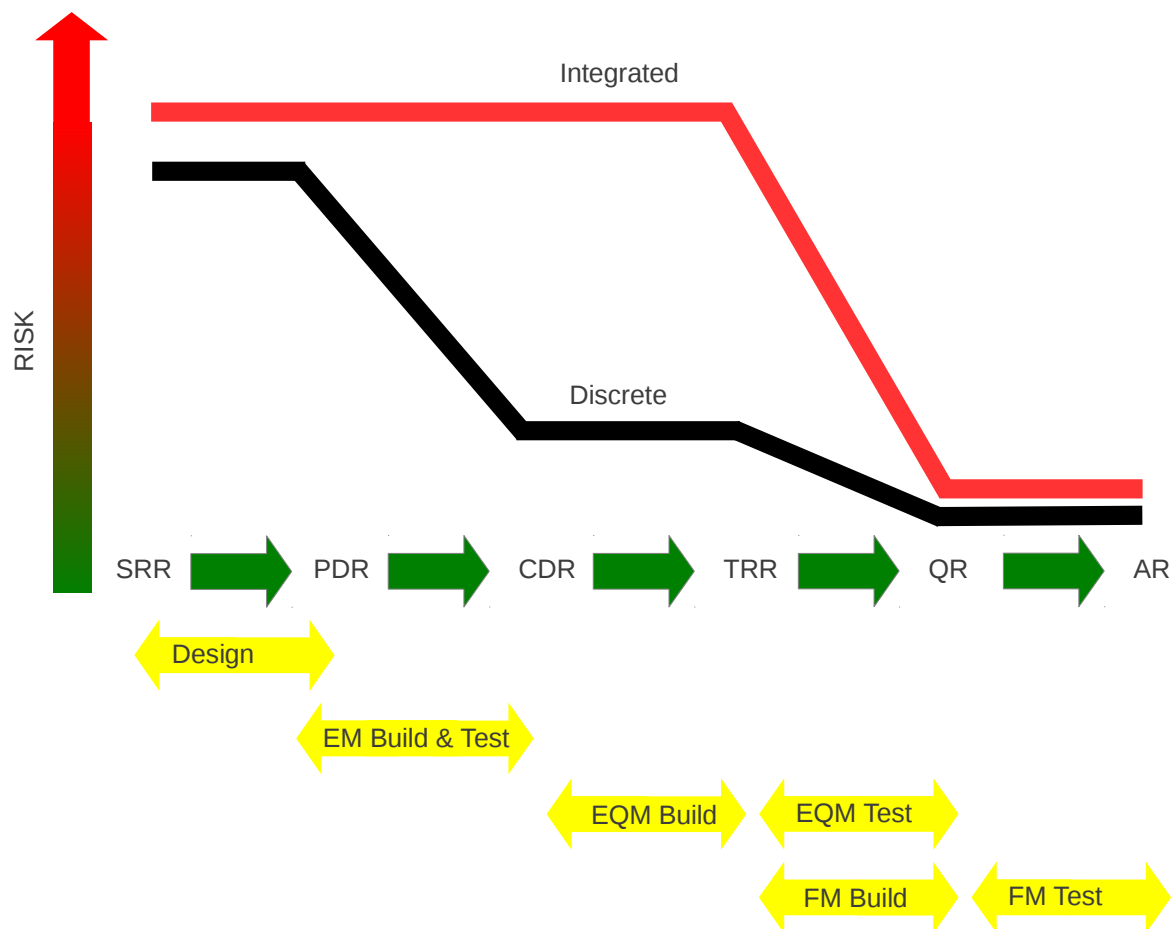
Cost

- Design of qualified IP blocks
- Design iterations
- Manufacture (low volume)
- Testing
- Qualification

Risk

- Limitations on the accuracy of library models
- Limitations of simulation tools
- Long design and manufacturing chain
 - no sub-block testing
 - late risk retirement

Development Risk



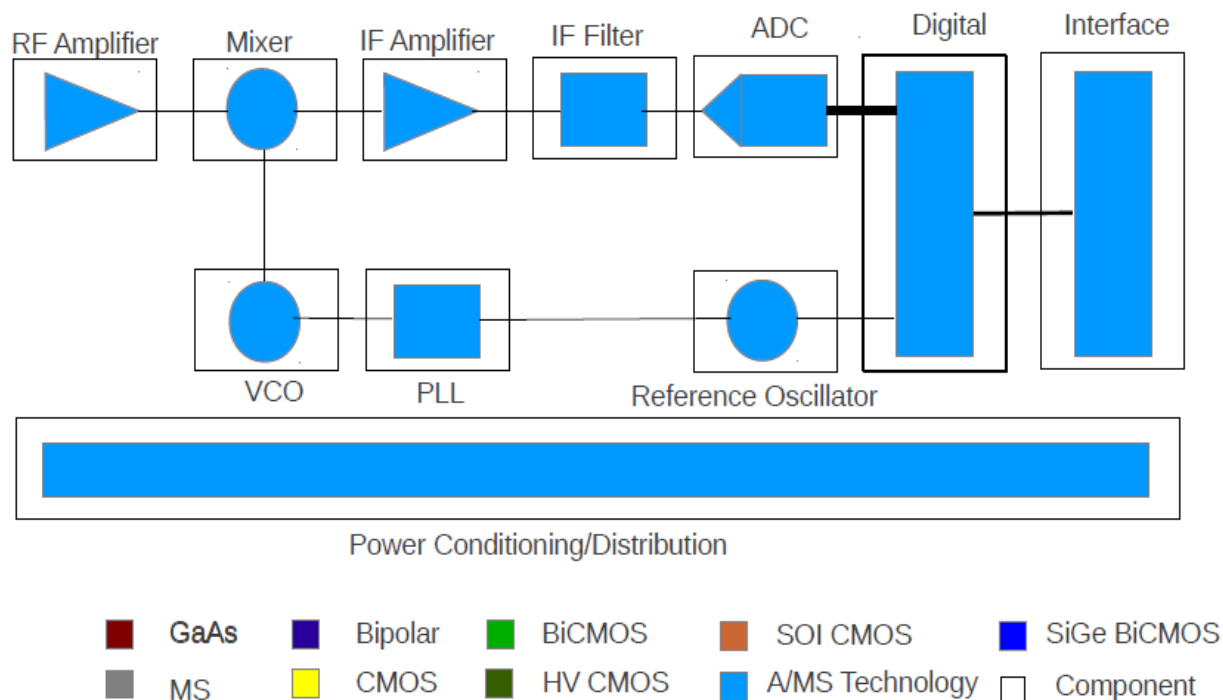
Reducing Development Risk

This integrated ASIC could be developed with a minimal risk

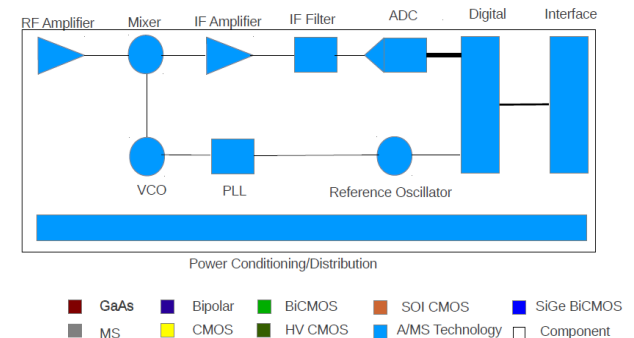
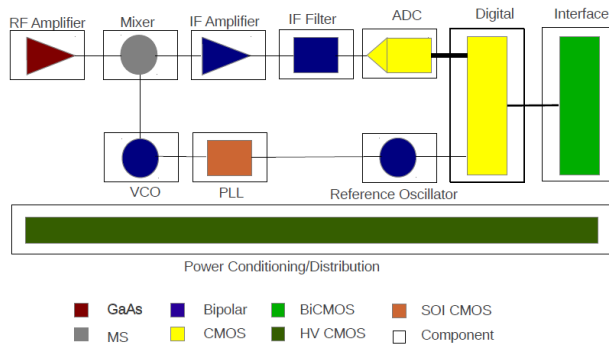
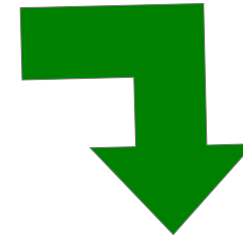
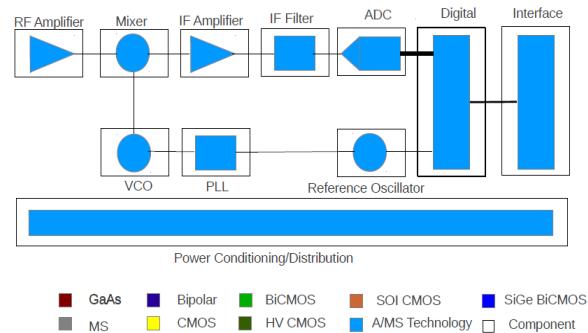
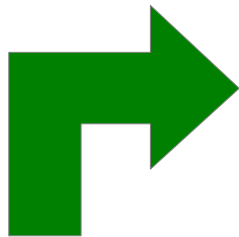
- 1) All the components/blocks have already achieved qualification with regard to functionality, performance, radiation hardness, reliability
- 2) The capability approval ensures that the repeated manufacture produces components/blocks of identical quality.
- 3) Well defined port impedances of the components/blocks ensures that the interfaces are well controlled
- 4) The EM has demonstrated the connected blocks interface, function and perform

This approach would be compatible with the satellite development programme, which ensures that at each milestone the development risk is reduced.

L Band Receiver - Space

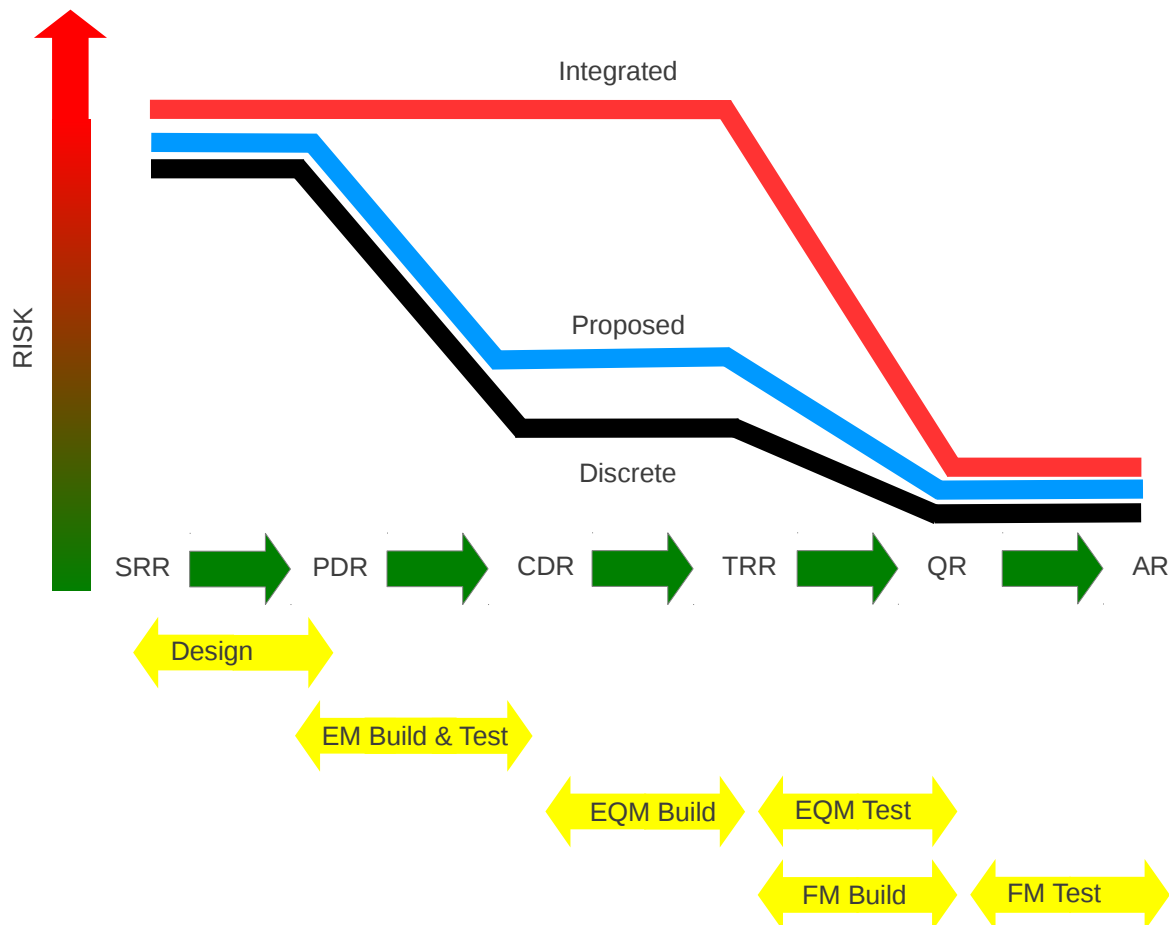


Increasing integration/enabling miniaturisation

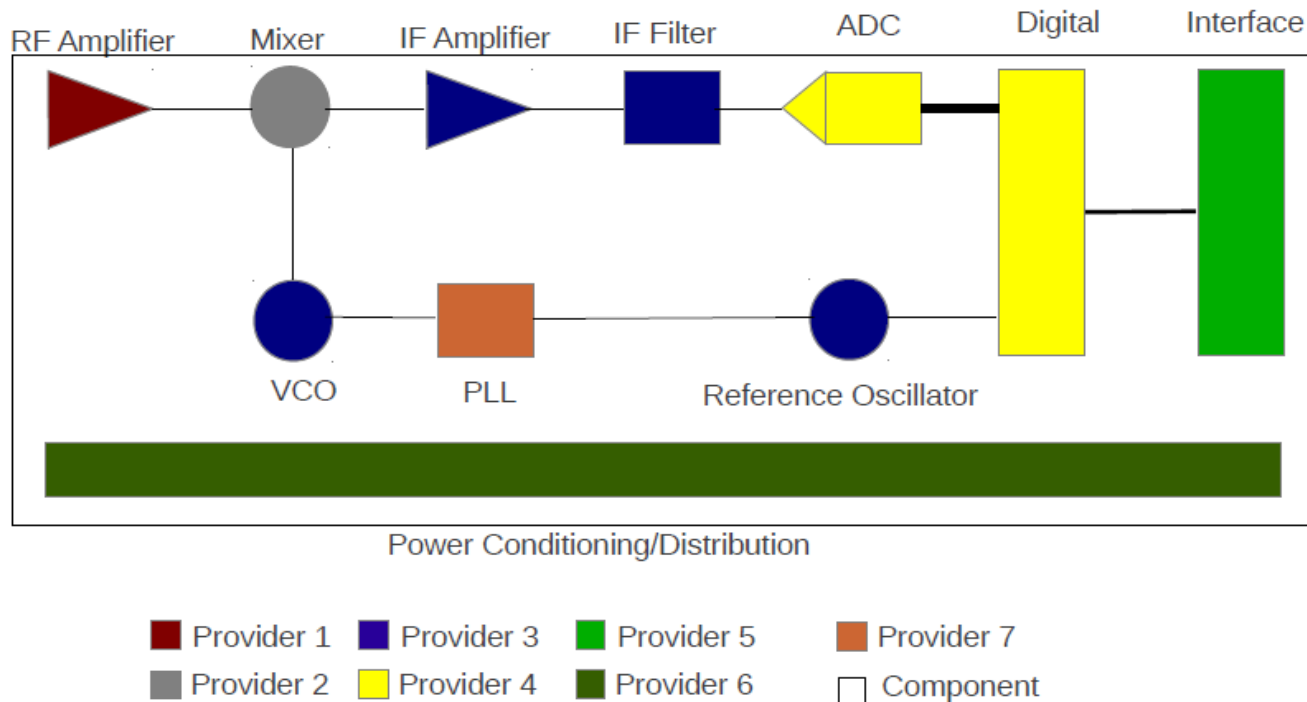


How can the advantages of the A/MS semiconductor technology be realised?

Development Risk



Increasing integration/enabling miniaturisation



Enabling Integration Platform

A comprehensive A/MS block library available from one/several companies

- The blocks ports should be defined and demonstrated to operate with other blocks on/off chip
- The blocks should provide a maximum of configurability/adaptability to limit their number
- The blocks should be ESCC space qualified for functionality / performance / radiation hardness / reliability for each operating mode

A verification/integration flow should be available on the technology

A ESCC capability approved foundry

AMICSA 2012 and IP-Cores Day provides an overview of the A/MS technologies and A/MS IP-Cores of the European space institutes and industry

Initial ASIC developments using A/MS IP-Cores started

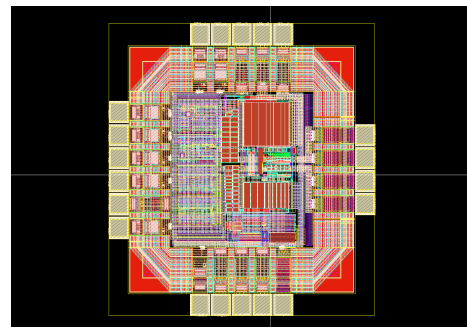
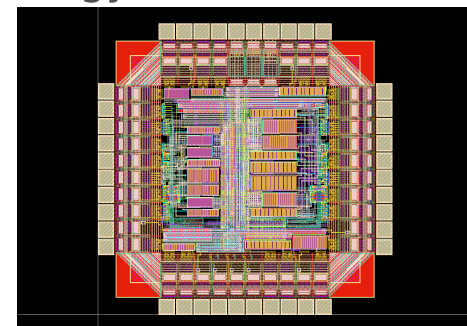
Specific ESA activities on the characterisation of A/MS Technology

- Assessment and characterisation of a mixed signal technology
- Evaluation and characterisation of a harmonised mixed signal ASIC flow
- Radiation Characterisation of Mixed-Signal Technology Test Vehicles

Internal Developments

- Analogue SET evaluation test-vehicle
- Radiation Tolerant CAN Transceiver

EAMAS Working Group



Demonstrated the need for A/MS IP-Cores and their continued performance improvement

Highlighted the issues encountered with use of A/MS IP-Cores on the development cycle of spacecrafts.

Highlighted the requirements on the A/MS IP-Cores and the target Integration Platform

Provided an overview of the A/MS IP-Cores activities