

Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)

ESA IP DAY 16/09/13

Bram De Muer, CEO ICsense



INNOVATION IN ANALOG INTEGRATION

WWW.ICSENSE.COM

ICsense in a nutshell

ICsense is an ISO9001 certified IC design company and ASIC supplier

Core competences:

High-performance analog / mixed-signal / high-voltage IC design



Markets:

Medical, industrial, consumer, automotive/aerospace

Strengths:



High-performance and low-power



Power and battery management



Sensor, actuator and MEMS interfacing/acquisition



High-voltage IC design

ICsense facts

Founded 2004

HQ Leuven, Belgium

Spin-off KULeuven

Team of 42 mixed-signal experts

ISO 9001:2008 – ISO 13485:2012

Foundry & technology independent



THine

Infineon

esa

DOLPHIN
INTEGRATION

ThalesAlenia
Space

ST

SENSIRION
THE SENSOR COMPANY

ifm electronic



ON

ON Semiconductor

NVIDIA

ENERGY
micro

NXP

TEGO

MICRONAS

imec

Cochlear

Markets served

Automotive & Aerospace

Radiation Hard mixed-signal
Fuel injection driver ASIC (95V)
Hall sensor read-out
GMR sensor ASIC
Gyroscope interface ASIC
H-bridge drivers
Xenon HID lamp driver
Battery management ASIC
...



Medical

X-ray imaging chipset
Deep brain stimulator ASIC
Li-Ion Battery charger IC
Nerve stimulation ASIC
Cochlear HA power mgmt.
Lab-on-chip interface ASIC
ECG readout
Wireless power/data transfer
...



Consumer

3-axis magnetic compass ASIC
MEMS gyroscope ASIC
Accelerometer interfacing
Power management IC
Hall sensor interface
40W PoE PD & SMPS controller
DC-DC converters
Class D audio drivers
Frac-N synthesizers
...



Industrial

Pressure & flow sensor ASIC
Inductive proximity sensor
High-power DC-DC controllers
Wheatstone bridge readout
Passive RFID tags
Embedded digital processing
Motor control and interfaces
Strain gauge interfacing
Inertial Measurement Units (IMU)...



IC design

Conditions and technologies

- Extended temperature range: -50 °C – 200 °C
- Extended voltage supply range: 0.8V – 100V
- Technology/foundry independent: 28nm – 0.8µm CMOS, BCD, ...
- Rad-hard design: +300kRad, SET simulations, ...

Complete mixed-signal IC solutions

cā dence™

Mentor
Graphics

synopsys®

MATLAB
SIMULINK

berkeley design®
automation, inc.

- Verilog-A(MS) / VHDL-AMS modeling
- Simulink / Matlab modeling
- Digital design: full ASIC/SoC, µControllers, memory, ...
- Full Mixed-Signal ASIC verification
 - Top down (wreal)
 - Bottom up
- Design for testability
- Prototype testing: in-house measurement lab
- Support for production testing (ATE)

Radiation Hard IC design flow at ICsense

SET design flow

- SET of 60 MeV.cm²/mg: inject double exponential charge of 1.2pC
 1. Typical conditions: inject in every node to find sensitive nodes
 2. SET simulations for all sensitive nodes over PVT
 3. Re-inject all nodes in worst-case corners
- Clock signals: injection time relative to clock period
- Top level: e.g. SET on bandgap does not influence PLL
- Fully automated flow integrated into our MATLAB driven design environment

TID Design flow

- Vth shifts: monitor $V_{DS} - V_{DS,SAT}$ of every device over PVT corners
- Bias conditions of matching structure are identical in all operation modes
- Extra DRC rules for proper P+ guard-ring in between N+ regions with DARE ADK
- Analog block with highest matching sensitivities use 1.8V devices
- 3.3V parts use ELT devices for NMOS

Example: Digital programmable controller

Applications:

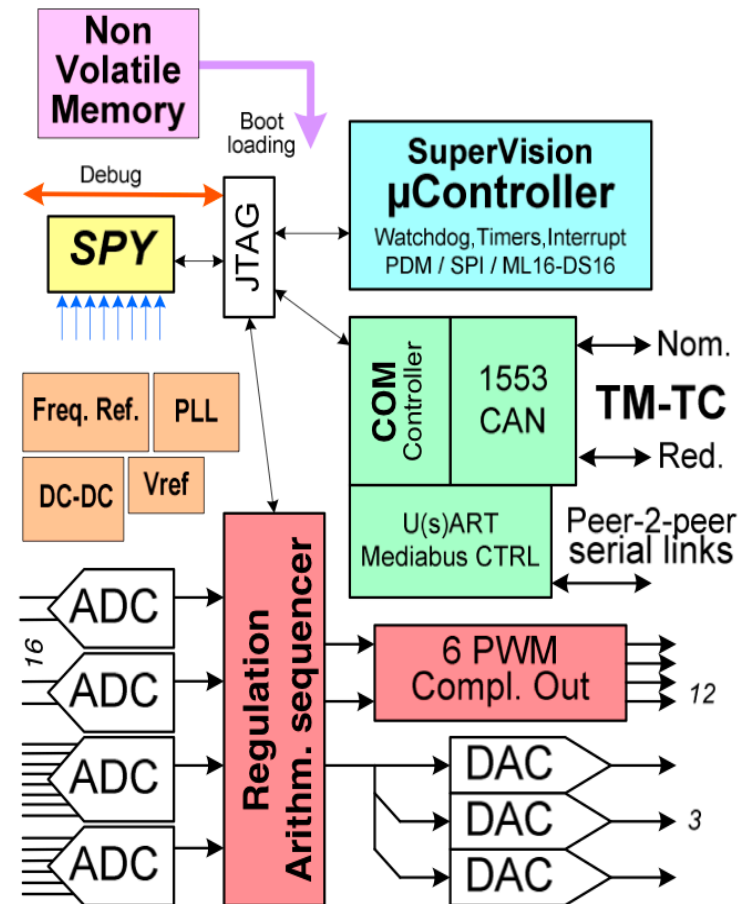
- Instrument control units
- Digitally controlled power management
- Motor controllers
- Intelligent remote sensor and controllers
- Remote terminal controllers
- Data bus protocol translation (gateway)

Requirements

- TID 100krad
- SET 60MeV.cm²/mg

Cooperation

- Thales Alenia Space ETCA
- Imec Services (DARE)



[AMICSA 2012]

High-performance mixed-signal radiation hard IP

UMC 0.18 (DARE)

- Fully compatible with imec's DARE solution supporting mixed-signal ICs
- Imec is business point of contact for DARE, incl. mixed-signal IP blocks
- Technical support by ICsense (located a few 100m from imec)

Available IPs:

- Bandgaps
- 13 bit ADCs
- 12 bit DACs
- Clocks
- PLL
- Linear regulators 3.3V to 1.8V

Other IPs, only on request:

- Instrumentations amps, PGAs
- Comparators
- Overcurrent-Overvoltage comparators
- Voltage buffers, R2R buffers
- Diff to single-ended buffers
- S&H
- UVLO
- POR (3.3V, 1.8V)
- Level shifters 3.3 to 1.8V, 1.8V to 3.3V, ...

ADC

Cyclic pipelined topology

- 100kSps – 1MSps
- 10-13 bit

Extensive input muxing

- Up to 8 analog single-ended or 4 differential signals
- Sampling time and channel selection is controllable

Features/extensions

- On-chip temperature sensor
- Offset calibration by shorting inputs
- Sensing amplifier chain

Specification	Value
Number of bits	13
Output data rate	1 MS/s
INL diff	<1.5 LSB
DNL	<0.5 LSB
SNDR	72 dB
Current consumption	< 6 mA @ 1.8V
Area	0.425 mm ²

DACs

Current steering
Dynamic element matching

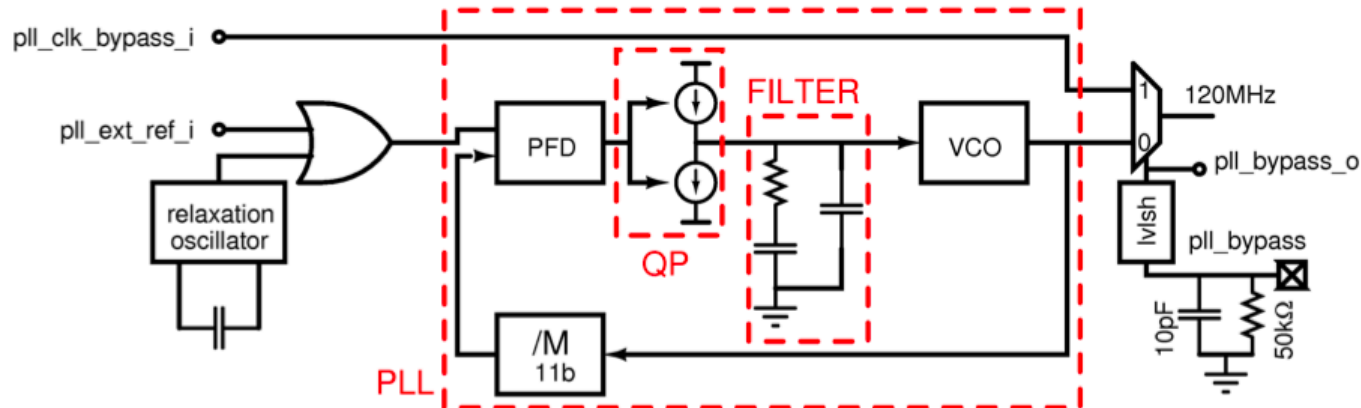
- Output:
- Buffer
 - Resistor

Specification	Value Fast DAC	Value Slow DAC
Number of bits	12	
Output data rate	3.75 MS/s	60 kS/s
Full scale current	4.1 mA	
INL (buffer)	<1.7 LSB	< 1.3 LSB
DNL	<1 LSB	< 0.75 LSB
THD	-82 dB	
Current consumption FS	< 4.5 mA	
Area	0.39 mm ²	



PLL

PLL



Specification	Value
Relaxation oscillator frequency	100 kHz
PLL output frequency	120 MHz (50-200MHz)
Max. SET frequency/phase shift	3% / 120 ns
Cycle-to-cycle jitter (over 480 cycles)	14ps
Current consumption	16 mA @ 1.8V
Area	2.3 mm ²

Oscillators

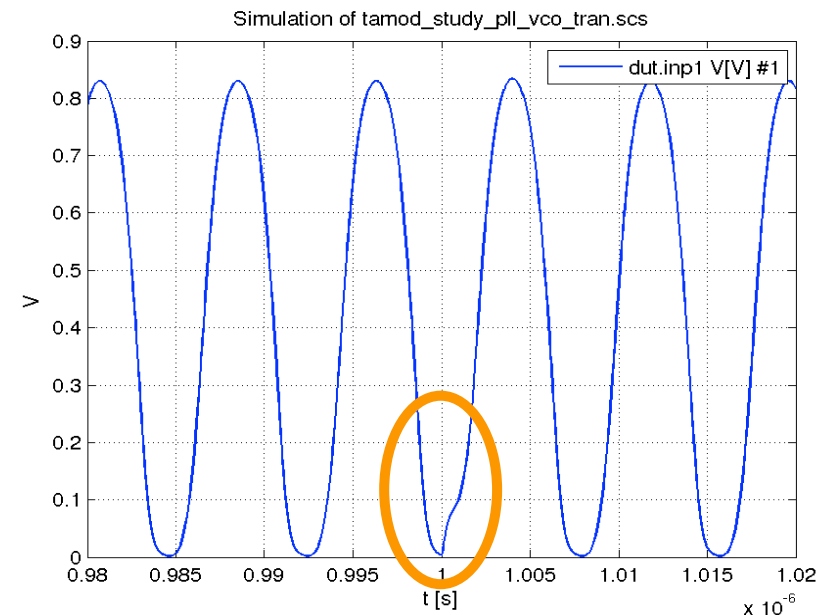
VCO 50-200 MHz

- Low-SET sensitivity

Relaxation oscillator

- External R and C for excellent stability and temperature drift
- Low-SET sensitivity
- Special topology to combine low jitter and low T drift.

Specification	Value
Frequency	100kHz
Accuracy all-in	$< \pm 5\%$
Current consumption	$< 2.5 \text{ mA}$
Area	0.45 mm^2



Reference voltage - regulator

Bandgap with external buffer capacitor

- SET sensitivity checked up to $60\text{MeV.cm}^2/\text{mg}$ on all nodes
- SET proof startup circuit

Specification	Value
Output	1V
Accuracy untrimmed	$< \pm 1.8\%$
Temp drift	$< 0.1\%$
Current consumption	$< 1.2\text{ mA}$
Area	0.23 mm^2

Linear regulators

- 3.3V to 1.8V
- External load cap
- 30mA load current
- 500mA load current

Rad Hard IP Road Map

Low-cost service fee for prototyping in ESA project

- Support
- .lib, LEF, simulation model, encrypted netlist, datasheet

Tweaking or redesign of blocks possible

Qualification of the IP blocks

- Expected Q4/2014

Similar offering in XFAB XH018

- ADC, PLL, DAC, osc, bandgap, regulators and auxiliaries
- NVM with delatcher
- Buck DCDC 15V -> 3.3V
- HV IOs
- Expected Q2/2014



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Thales Alenia Space ETCA
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