2nd ESA IP-Cores Day

16th of September 2013
ESA / ESTEC (Noordwijk, The Netherlands)

Description of the Event

On the 16th of September 2013 the 2nd ESA IP-Cores day will take place at ESA/ESTEC, in EINSTEIN meeting room.
Aim of the day is to exchange information, lessons learnt and to discuss with relevant European Space Industry some of the benefits and challenges of both developing and using IP-Cores for space integrated circuits., The current status of ESA IP-Cores offer will be presented at the beginning of the day, followed by a series of short Industry presentations showing IP user and IP development experiences, to then collect at the end ideas for improving the ESA IP Core offer.

Agenda

1) *Introduction (10:00 – 11:00)*
   - **IP-Core based design methodology**, ESA (Fossati)
   - **Current ESA IP-Cores offer and on-going developments**, ESA (Fossati)
2) *Industry Experience in Using/Designing IP-Cores (11:00 – 14:15)*
   - **ASIC, FPGA, ASSPs platforms development through IP-Cores re-use**, Atmel (Bancelin)
   - **TTEthernet 2.0 IP Cores for Space**, TTTech (Make-Kail)

   Coffee Break: 11:30 – 11:45
   - **SITAEL IP Cores**, Sitael (Bigongiari)
   - **New features and IP Cores in the GRLIB IP Library**, Aeroflex Gaisler (Andersson)
   - **Remote terminal Macrocells**, Maya Tech. (Mercier)

   Lunch: 12:30 – 13:30
   - **IP-Cores design using SEE mitigation techniques for Flash-based FPGAs**, ESA (Furano, Urbina)
   - **Experience in developing SpaceWire and SpaceFibre IP Cores**, Star-Dundee (Parkes)
   - **Advanced CCSDS File Delivery Protocol Hardware IP Core**, TU Braunschweig (Berekovich)
3) *Analog IP-Cores (14:30 – 15:45)*
   - **Analogue and Mixed-Signal IP cores for Space: Status and Challenges**, ESA (R. Jansen)
   - **Analog rad hard ASICs for cosmic vision - reusability of IP-Cores**, Arquimea (Gutierrez)

- **Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)**, ICSense (De Muer)
- **Development of RHBD mixed-signal ASICs and IP-Blocks in AMS-0.35um**, IMSE-CNM-CSIC / Universidad de Sevilla (Meana)

Coffee Break (15:45 – 16:00)

4) *Round-Table – 11 years of ESA IP-Cores service (16:00 – 16:30)*
   - Discussion on the status of the ESA IP-Core service, brainstorming on negative and positive aspects, improvements for the future both in terms of the service and of the IP-Cores part of the offer.
5) *Q/A and Conclusions* (16:30 – 17:00)

Abstracts

Industry Experience in Using/Designing IP-Cores (11:00 – 14:15)

ASIC, FPGA, ASSPs platforms development through IP-Cores re-use, Atmel (Bancelin)

ATMEL sets up platforms for the development of ASIC, FPGA and ASSPs. From 180nm, ATMEL is now moving to mixed 150nm, high voltage (>=60V) SOI deep trench, 90nm and 65nm. For space business and similar markets, it becomes mandatory to share and reuse the developments to better amortize cost and to benefits from proven and validated development. It was done for digital libraries. It must be done for analog libraries with electrically and radiation proven blocks. It must be done for IPs hard and soft to ensure safe multiple use and fruitful maintenance.

Atmel is setting up a flow able to collect IPs, digital and analog, from various developers in Europe and to guarantee a safe use.

TTEthernet 2.0 IP Cores for Space

TTTech (Make-Kail)

TTTech will present which TTEthernet IP cores are planned for global space use.
This includes IP cores for different types of end-systems as well as for a space-graded switch.
The base IP was developed for cross-industry use without any ESA funding.
Currently ESA support for space validation is sought. Special licensing for ESA projects to be discussed.
Interfaces to other IP cores will be shown as well as differences to core variants used in other industries.

SITAEL IP Cores

Sitael (Bigongiari)

The last IP cores developed by SITAEL will be presented: CCIPC (CANOpen Controller IP Core),
IMMIPC (Improved Memory Module IP Core) and V8uC (Sparc V8 based micro-controller IP).
For each IP Cores features, performances and possible improvements will be shown.
Finally, validation procedure, maintenance and long-term support for IP Cores will be addressed and discussed.

New features and IP Cores in the GRLIB IP Library

Aeroflex Gaisler (Andersson)

The GRLIB IP library provides the LEON3FT processor together with a wide range of peripheral cores. During the past two years a transition has been made from technology specific netlists, with fixed LEON3FT configurations, to a solution with encrypted RTL. The presentation will discuss this transition and advantages of using encrypted RTL. New IP cores and other new features of the GRLIB IP library will also be presented.

Remote terminal Macrocells
Maya Tech. (Mercier)

The MYA-1553-RM2-IP and MYA-1553-BRM1-IP are two macrocells that can be used to implement
a remote terminal only or remote terminal + bus controller 1553 interface into
an ASIC or FPGA device. The macrocells are technology independent and silicon proven both
in satellite and aeronautic applications.
The presentation gives an overview about the key features and benefit of the macrocells, licensing conditions,
and presents some application examples that instantiate them.

IP-Cores design using SEE mitigation techniques for Flash-based FPGAs, ESA (Furano, Urbina)

Enhancing commercial IP-Cores with rad-hard by design tecuniques: using SEE mitigation techniques for Flash-based FPGAs

Experience in developing SpaceWire and SpaceFibre IP Cores, Star-Dundee (Parkes)

Abstract not present

Advanced CCSDS File Delivery Protocol Hardware IP Core, TU Braunschweig (Berekovich)

Under ESA contract "Development of CCSDS File Delivery Protocol IP Core" TU-Braunschweig is developing the reference CFDP Hardware IP Core that shall be used as accelerator in future space flight projects. The CCSDS File Delivery Protocol (CFDP) was introduced by the Consultative Committee for Space Data Systems (CCSDS) as a response to the rapid evolution of storage media in space-flight. This file delivery protocol will lead the way for space missions with mass memory storage, large data files and onboard real-time operating systems that will require the presence of a file-system.

The CFDP hardware IP-Core is developed as a streaming-oriented Co-Processor with separate high performance AMBA interfaces, that will be used in conjuction with a LEON2 Processor. The core will support CFDP Class1 and Class2 services and is suited for offloading the host processor from the demanding task of CFDP protocol processing and PDU encapsulation/ decapsulation.

A SystemC IP-Model was created as a part of this project to enable design entry at Electronic System Level (ESL). The model was integrated in the ESA reference SoCRocket Virtual Platform for performance and throughput analysis. The selected approach allowed to start SW driver development early and enhance the IP-Core architecture before migration to RTL.

In this talk we will present the status of the IP-Core development, the SocRocket simulation framework and the results of the Design Space Exploration.

Analog IP-Cores (14:45 – 16:00)

Analogue and Mixed-Signal IP cores for Space: Status and Challenges
ESA (R. Jansen)

The level of integration of functions within one chip has been steadily increasing. This has been visible for digital space ASICs with the SoCs like the SCOC3 and MDPA and recently also for mixed-signal space ASIC like the KNUT and DPC. Without the use of IP cores such developments would take much longer to achieve and would have uncertain outcomes. The importance of digital IP cores has been recognised early on and receives active support and attention. In contrast the mixed-signal space IP cores are relatively new and their incorporation into mixed-signal SoCs is being explored. The status of this work and its challenges are presented.

Analog rad hard asics for cosmic vision - reusability of IP-Cores
Arquimea (Gutierrez)

In this talk the IPs resulting from the development of two Mixed Signal ASICS for COSMIC VISION (ESA TRP projects) will be presented including the analysis about how these IPs can be reused from both technical and procurement points of view.

Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)
ICSense (De Muer)
The analog, mixed-signal IC design company ICsense offers high-performance, radiation-hard analog IP blocks as part of the imec DARE solution. These blocks are ideally suited for rad-hard mixed-signal ICs and include 13 bit, 1MSps ADCs, a SET-hard 120MHz PLL, 8-12 bit DACs, high-voltage IOs, high voltage DCDC converters, linear regulators, clocks, voltage references, opamps, comparators and other auxiliaries. The low-voltage IP blocks are available in DARE UMC 0.18um and both low- and high-voltage blocks will be available in DARE XFAB XH018 by the end of 2013. ICsense has developed a proprietary design environment to simulate effects of radiation and ensure radiation hardness by design. ICsense provides support for these blocks and other custom analog, high-voltage and mixed-signal IP.

Development of RHBD mixed-signal ASICs and IP-Blocks in AMS-0.35um
IMSE-CNM-CSIC / Universidad de Sevilla (Meana)

Ongoing efforts at IMSE-CNM-CSIC/University of Sevilla have the objective of establishing a solid foundation for the design of mixed-signal ASICs for space use. We have focused initially in a specific bulk CMOS technology, Austriamicrosystems 0.35um. Present results include the characterization of radiation effects (TID) on transistors with different layout styles and geometries, and of SEE on a number of analog and digital circuits with different layout styles and RHBD techniques, and on analog and digital I/O cells. A Rad Hard digital library has been developed and has been used together with custom analog circuitry in the design of two specific mixed-signal ASICs. The first of them is a transceiver for diffuse-light intra-satellite communications, while the other is a semi-general purpose front-end including multiple, reconfigurable channels for signal

adaptation and AD conversion with a standard SPI interface for programming and data handling.

For more information and registration please refer to webpage http://www.esa.int/TEC/Microelectronics/SEMCVIT2WEH_0.html or contact Luca.Fossati@esa.int.