Single Event Transient Effects on Microsemi ProASIC Flash-based FPGAs: analysis and mitigation

L. Sterpone
Dipartimento di Automatica e Informatica
Politecnico di Torino, Torino, ITALY
Motivations and Goals

• Evaluation of Single Even Transients (SETs) impact on complex designs is an increasing challenge
• Their analysis have to face several issues
  – Simulation
    Model is intrinsically approximative, simulation campaigns take long time
  – Effective analysis
    Laser and Radiation testing are expensive and not applicable at the design early stage
• A CAD tool able to analyze and reduce the impact of SETs affecting VLSI technology is very welcome
  – Early stage design analysis
  – Fast and effective analysis
Outline

• Introduction
• Single Event Transient phenomena
• Preliminary studies on Flash-based FPGAs
• Gates characterization – PIPB effect
• SETA main flow
  – Main routines
  – SET generation
  – SET propagation
• Tool execution and experimental results
• Conclusions
Introduction

• Different scenarios may influence SET propagation
  – Logical masking
  – Electrical broadening or filtering
  – Latching window

• Not all the SETs are transformed in circuit errors

• SET sensitivity is intrinsically related to the technology cell
  – Different sensitivity figures
Source of SET effects

• Generation of SET effects is due to the injunction of charge collection
  – When a charged particle crosses a junction area, it generates an amount of current, provoking a “glitch”
• Propagation of voltage glitches may be for notable distances
• SET may become indistinguishable from normal signal
Single Event Transient - info

- SET can be defined considering four main parameters:
  - SET width
  - SET amplitude
  - Rise $\Delta V/\Delta T$
  - Fall $\Delta V/\Delta T$
Single Even Transient Phenomena

• Two transitions are possible
  0-1-0 or 1-0-1
• SET is generated into the sensitive area of a logic gate
• It propagates until a sequential element is reached
• During the propagation the SET may pass through different gates:
  – INV, NAND, OR, AND, ...
The effect of an SET is mainly due to:
- Location
- Arrival time
- Pulse’s width.

The sensitivity of a FF can be measured as the ratio between the SET’s width and the CLK period.
The Flash-based FPGAs are composed of:
- Logic, I/O, Routing
- The basic element is the **VersaTile logic block**
- A Flash configuration memory controls all the resources
- Bitstream programs the desired circuit
Radiation effects in Flash-based FPGAs

- **VersaTile** may undergo to three possible effects due to radiation particle hits:
  1. Induce a pulse propagated through the logic
  2. Affect a logic cell configured as a latch
  3. Affect a junction of the floating gate

SET pulse shape may be:
- Broadened / filtered
- Amplified / attenuated
SET propagation background

- SETs are generated into the sensitive area of a logic gate
  - Two transitions are possible (0-1-0 and 1-0-1)

Fist Region: If $\tau_n < k*tp$ then $\tau_{n+1} = 0$

Second Region: If $(\tau_n > (k+3)*tp)$ then $\tau_{n+1} = \tau_n + \Delta tp$

Third Region: If $((k+1)*tp < \tau_n < (k+3)*tp)$ then $\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta tp$

Fourth Region: If $(k*tp < \tau_n < (k+1)*tp)$ then $\tau_{n+1} = (k+1)*tp(1 - e^{(k - (\tau_n/tp))}) + \Delta tp$

For a 1→0→1 transition $\Delta tp$ is defined as:
$$\Delta tp = tp_{HL} - tp_{LH}$$

For a 0→1→0 transition $\Delta tp$ is defined as:
$$\Delta tp = tp_{LH} - tp_{HL}$$

Wirth et al, NSREC 2008
Sterpone, Battezzati, Lima RADECS 2010
SETs on Actel Flash-based FPGAs

- Radiation tests have been executed:
  - Measurement of the pulse’s width
  - Frequency impact on SEE on Flash-based FPGAs
SETs on Actel Flash-based FPGAs

- Experimental results

Mean number of SETs occurrences

<table>
<thead>
<tr>
<th>Time [ns]</th>
<th>&lt; 0.96</th>
<th>0.96 - 1.92</th>
<th>1.92 - 2.88</th>
<th>2.88 - 3.84</th>
<th>3.84 - 4.80</th>
<th>4.80 - 5.76</th>
<th>5.76 - 6.72</th>
<th>&gt; 6.72</th>
</tr>
</thead>
<tbody>
<tr>
<td>Count</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Luca Sterpone, SET project, ESA final presentation days
SETs on Actel Flash-based FPGAs

- **Ni ions**
- **Ag ions**
SETs on Actel Flash-based FPGAs

- Radiation tests performed at the HIF, Louvain-La-Neuve, Belgium
- Iodine beam LET 61.8 MeV cm\(^2\)/mg
- DUT: pipelined multiplier
## SETs on Actel Flash-based FPGAs

<table>
<thead>
<tr>
<th>Circuit</th>
<th>FF tiles [#]</th>
<th>Combinational Tiles [#]</th>
<th>Routing resources [#]</th>
</tr>
</thead>
<tbody>
<tr>
<td>v1</td>
<td>2,484</td>
<td>3,405</td>
<td>126,840</td>
</tr>
<tr>
<td>v2</td>
<td>2,484</td>
<td>3,405</td>
<td>252,446</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Observed events [#]</th>
<th>Design Cross-section</th>
</tr>
</thead>
<tbody>
<tr>
<td>v1</td>
<td>710</td>
<td>1.052 E-04</td>
</tr>
<tr>
<td>v2</td>
<td>729</td>
<td>1.217 E-04</td>
</tr>
</tbody>
</table>

[TNS’09]
Existing CAD tools for SET analysis

• 2D and 3D device model simulation or technology CAD (TCAD) or SPICE are generally adopted
  – effective only on a reduced portion of a circuit thousands of gates
  – very low speed
  – Cannot be realistically applied to an entire circuit

• PIPB effect is not modeled and characterized with respect to a given technology
  – Dynamic PIPB model embedded in SPICE has proven and demonstrated to be effective

Sterpone et al, TNS 2011
The developed CAD tool for SET

Native implementation flow starting from the VHDL/Verilog configuration bitstream or GDS ASIC layout files

Luca Sterpone, SET project, ESA final presentation days
The developed SETA tool

Native implementation starting from the VHDL, leading to the FPGA configuration bitstream.

SET sensitivity computation for each FF of the circuit.

Logic gates and routing description including PIPB characterizations.

Luca Sterpone, SET project, ESA final presentation days
Netlist to Physical Design Description

- The circuit netlist is loaded
- A directed graph structure is generated
  - I/O element, FFs, RAM/ROM pins, ... are considered as terminal points
  - Logic gates are considered as crossing points
  - Interconnections are defined as direct edges between nodes
• The circuit graph is organized in a matrix-based graph
  – Vertices placed on the same layout position
  – Edges related to the FPGA routing model
SETA algorithm

• A set of SET pulse shape is generated
  – Defined as a voltage spike
  – Voltage amplitude / width
  – Defined as 100,000 points (resolution of 1ps)

1. Generate the list of SET pulse: SET_{GP}
2. For each generated pulse \( p \in (\text{SET}_{GP}) \)
   2. For each sensitive node \( i \in (\text{SN}) \)
      Apply pulse \( p \) to \( i \)
      Find destination node \( dn \in (\text{SN}, i) \)
      3. For each \( dn \)
         Propagate \( p \) on \((i, dn)\)
SETA algorithm

- The generated voltage pulse is applied to the selected sensitive node

1. Generate the list of SET pulse: \( \text{SET}_{GP} \)
2. For each generated pulse \( p \in (\text{SET}_{GP}) \)
   2. For each sensitive node \( i \in (\text{SN}) \)
      - Apply pulse \( p \) to \( i \)
      - Find destination node \( dn \in (\text{SN}, i) \)
      3. For each \( dn \)
         Propagate \( p \) on \((i, dn)\)
SETA algorithm

- The list of destination node is created

1. Generate the list of SET pulse: \( SET_{GP} \)
2. For each generated pulse \( p \in (SET_{GP}) \)
   2. For each sensitive node \( i \in (SN) \)
      Apply pulse \( p \) to \( i \)
      Find destination node \( dn \in (SN, i) \)
      3. For each \( dn \)
         Propagate \( p \) on \((i, dn)\)
SETA algorithm

- The voltage array $p$ is propagated through the logic element $G_1$ to the next destination node $G_2$
- The propagation is computed on the basis of the crossing-PIPB
- Propagation is performed assuming no-logic masking [actual version of SETA]

$$P_{G_1} \text{ is propagated in } P_{G_2}$$

Output Pulse Width $(x) = \text{Input Pulse Width (}x\text{)} \times K(x)_{\text{broadening}}$
The tool set – Microsemi / Actel

• The PDT CAD tool is compiled under Linux
  – Compatible with Windows or MaCOSx operative systems

• The tool set contains the following executables:
  – **AFL2PDD**: conversion of the EDIF netlist to the PDD file
  – **PDC_PDD**: conversion of the PDD coordinates to the Physical Design Constraint (PDC) format
  – **PDD_Place**: the placement algorithm
  – **SET_analyzer**: the SET analyzer algorithm
Step 1: generation of the files

- The first step consists on generating the support files from the Microsemi tools (IDE libero).

- Two files may be generated:
  - AFL: Flat Netlist description file
    It can be generated after the Symplyfy Synthesis
  - PDC (optional): Physical Constraints File
    It can be generated after the place and route phase
Step 2: generation of the PDD file

• The second step consists on the generation of the PDD file
• This operation is performed by executing: 
  ./AFL2PDD design_name.afl
• The execution may require some minutes
• It generates a PDD file: design_name.afl.pdd
Step 2.1: the PDD file

- The PDD file contains the graph-based architecture of the circuit
  - All the circuit logic cells are vertex
  - All the circuit interconnections are edges

```
53
u1/gen_pipe_12_Pipe/Yo[8]
F DFN1E1
1 4
0
0
1
U
1 1659 A Y
1 3003 Y A
2 1846 Y A
3 2458 Y A
4 385 Y A
```
Step 3: the SET analysis

• Once the PDD file is generated and there is an available PDC file it is possible to perform the SET analysis

• An example of command may be the following:

```bash
./SET analyzer name.pdd name.pdc 1 10 mine 0.450
```
Step 3.1: the SET analysis

- The parameter you may use are the following:
  - Source netlist (PDD)
  - Source placement (PDC)
  - Start pulse width (1: about 8ns)
  - End pulse width
  - Name of the report generated files
  -Verbose
  - Limit for the “gate to gate”
Step 3.2: the SET analysis

- The design sensitivity overview

<table>
<thead>
<tr>
<th>P_S [ns]</th>
<th>L_M [#]</th>
<th>T_F [#]</th>
<th>P_F [#]</th>
<th>P_B [#]</th>
<th>O_L [#]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.660940</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>1325</td>
</tr>
<tr>
<td>1.383990</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>361</td>
</tr>
<tr>
<td>1.186026</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>237</td>
</tr>
<tr>
<td>1.038044</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>189</td>
</tr>
<tr>
<td>0.923033</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>41</td>
</tr>
<tr>
<td>0.830024</td>
<td>605</td>
<td>0</td>
<td>33</td>
<td>82</td>
<td>39</td>
</tr>
<tr>
<td>0.755016</td>
<td>605</td>
<td>17</td>
<td>16</td>
<td>82</td>
<td>5070</td>
</tr>
<tr>
<td>0.693010</td>
<td>605</td>
<td>17</td>
<td>16</td>
<td>82</td>
<td>5064</td>
</tr>
<tr>
<td>0.639004</td>
<td>605</td>
<td>18</td>
<td>2</td>
<td>95</td>
<td>5064</td>
</tr>
<tr>
<td>0.593000</td>
<td>605</td>
<td>18</td>
<td>2</td>
<td>95</td>
<td>5064</td>
</tr>
<tr>
<td>0.553996</td>
<td>605</td>
<td>18</td>
<td>2</td>
<td>95</td>
<td>5064</td>
</tr>
<tr>
<td>0.519993</td>
<td>605</td>
<td>18</td>
<td>2</td>
<td>95</td>
<td>5062</td>
</tr>
<tr>
<td>0.487994</td>
<td>605</td>
<td>19</td>
<td>1</td>
<td>95</td>
<td>5058</td>
</tr>
<tr>
<td>0.461994</td>
<td>605</td>
<td>19</td>
<td>1</td>
<td>95</td>
<td>5220</td>
</tr>
</tbody>
</table>

Gate to gate interconnection where SET are broadened more than the inserted user limit (i.e. 0.450 ns)

Logically masked pulses

Luca Sterpone, SET project, ESA final presentation days
Step 3.3: SET detailed report

- Further reports are generated for designer help:
  - Max_pulse_report: it provides for each FF the maximal SET pulse
  - Max_broad_report: it provides for each FF the maximal broadening effect
  - Gate 2 Gate: it provides the broadening effect specifically observed between a couple of logic gates inside of the design
  - FF reports: it provides several detailed information on the pulses observed on each FF

Can be used for selective filtering technique application
## SET sensitivity report: an example

<table>
<thead>
<tr>
<th>FF id and position (X,Y)</th>
<th>Source SET</th>
<th>Destination SET</th>
<th>Broadening</th>
<th>Destination SET / Clock period</th>
<th>% filtering gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>-- D FF[#]</td>
<td>P S[ns]</td>
<td>P D[ns]</td>
<td>Broad[ns]</td>
<td>Sens[%]</td>
<td>Gain[%]</td>
</tr>
<tr>
<td>-- 230(81,48)</td>
<td>0.487994</td>
<td>0.006957</td>
<td>-0.481037</td>
<td>0.006957</td>
<td>98.574448</td>
</tr>
<tr>
<td>-- 332(70,4)</td>
<td>0.487994</td>
<td>0.000206</td>
<td>-0.487788</td>
<td>0.000206</td>
<td>99.957863</td>
</tr>
<tr>
<td>-- 388(57,31)</td>
<td>0.487994</td>
<td>0.000000</td>
<td>-0.487994</td>
<td>0.000000</td>
<td>100.000000</td>
</tr>
<tr>
<td>-- 458(69,10)</td>
<td>0.487994</td>
<td>0.938037</td>
<td>0.450043</td>
<td>0.938037</td>
<td>-92.223206</td>
</tr>
<tr>
<td>-- 1953(35,15)</td>
<td>0.487994</td>
<td>0.038000</td>
<td>-0.449994</td>
<td>0.038000</td>
<td>92.213112</td>
</tr>
<tr>
<td>-- 2052(60,36)</td>
<td>0.487994</td>
<td>0.000610</td>
<td>-0.487384</td>
<td>0.000610</td>
<td>99.875076</td>
</tr>
<tr>
<td>-- 2375(86,37)</td>
<td>0.487994</td>
<td>0.038000</td>
<td>-0.449994</td>
<td>0.038000</td>
<td>92.213112</td>
</tr>
<tr>
<td>-- 2406(82,30)</td>
<td>0.487994</td>
<td>0.045002</td>
<td>-0.442992</td>
<td>0.045002</td>
<td>90.778137</td>
</tr>
</tbody>
</table>
Step 4: the PDD placement

- The placement maybe performed independently from the SET analysis
- This operation is performed by executing:
  ```
  ./PDD_place source_design.pdd destination_design.pdd X Y N 1
  ```
- The execution may require several minutes
## Circuit characteristics

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>Device Type</th>
<th>Sensitive Nodes [#]</th>
<th>FFs [#]</th>
<th>Propagation Path [#]</th>
<th>SETA elaboration time [min]</th>
</tr>
</thead>
<tbody>
<tr>
<td>B04</td>
<td>A3P600</td>
<td>493</td>
<td>67</td>
<td>49,512</td>
<td>54</td>
</tr>
<tr>
<td>B05</td>
<td>A3P600</td>
<td>415</td>
<td>66</td>
<td>19,820</td>
<td>12</td>
</tr>
<tr>
<td>B12</td>
<td>A3P600</td>
<td>565</td>
<td>123</td>
<td>5,717</td>
<td>4</td>
</tr>
<tr>
<td>B13</td>
<td>A3P250</td>
<td>162</td>
<td>50</td>
<td>518</td>
<td>0.3</td>
</tr>
<tr>
<td>8051</td>
<td>A3P1000</td>
<td>3,414</td>
<td>249</td>
<td>1,772,044</td>
<td>642</td>
</tr>
</tbody>
</table>
# SETA analysis data

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>SET pulses evaluated [#]</th>
<th>SET pulse masked [#]</th>
<th>SET pulse observed [#]</th>
<th>SET pulse observed [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>B04</td>
<td>6,902</td>
<td>6,747</td>
<td>155</td>
<td>2.25</td>
</tr>
<tr>
<td>B05</td>
<td>5,810</td>
<td>5,711</td>
<td>99</td>
<td>1.70</td>
</tr>
<tr>
<td>B12</td>
<td>7,910</td>
<td>7,601</td>
<td>309</td>
<td>3.91</td>
</tr>
<tr>
<td>B13</td>
<td>2,268</td>
<td>2,057</td>
<td>211</td>
<td>9.30</td>
</tr>
<tr>
<td>8051</td>
<td>47,796</td>
<td>47,557</td>
<td>239</td>
<td>0.50</td>
</tr>
</tbody>
</table>
Average broadening increases proportionally with the circuit complexity (number of propagation paths).

Actel Microsemi A3P ProAsic family delay threshold is around 440 ps.

Very narrow SETs are intrinsically filtered by the device delay threshold.
SET occurrences

Narrow SETs may elongate up to 8 ns
Results validation

- Results have been validated through electrical fault injection
  - Selective injection of SET pulses
  - SETs counted by a sampler circuit on a Virtex-5 FPGA
  - Injection is performed instrumenting the circuits
Results validation

- Results have been validated through electrical fault injection

![Graph showing electrical injection points]
RISC hardening analysis

- **Circuits characteristics**

<table>
<thead>
<tr>
<th>RISC version</th>
<th>Logic Gates</th>
<th>FFs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unhardened</td>
<td>1,401</td>
<td>1,156</td>
</tr>
<tr>
<td>Full TMR+ GG</td>
<td>20,808</td>
<td>3,468</td>
</tr>
<tr>
<td>TMR + FF</td>
<td>4,203</td>
<td>3,468</td>
</tr>
<tr>
<td>PDT CAD tool</td>
<td>5,514</td>
<td>3,468</td>
</tr>
</tbody>
</table>
## RISC hardening analysis

- SET analysis results by means of fault simulation

<table>
<thead>
<tr>
<th>RISC version</th>
<th>SETs</th>
<th>SEUs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unhardened</td>
<td>1,401</td>
<td>1,839</td>
</tr>
<tr>
<td>Full TMR+ GG</td>
<td>1,562</td>
<td>0</td>
</tr>
<tr>
<td>TMR + FF</td>
<td>2,302</td>
<td>0</td>
</tr>
<tr>
<td>PDT CAD tool</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>
Conclusions

• A CAD tool – SETA – is available and able to automatically evaluate the SET sensitivity of complex circuits
  – Applied on Flash-based FPGAs
  – Embedding the PIPB effect characterization

• The SETA tool allows to
  – Investigate the behavior of individual FFs
  – Selectively apply mitigation solutions (guard-gates, selective TMR, others…)

• SETA results embedded into P&R flow
  – Completely DONE for the placement
Future works

• Compare the SETA analysis with laser and radiation testing
• Creating an IDE user interface and web-user access
• Extend the SETA flow to ASIC gate library
Thank you..

- For your attention

Question and comments:
Luca Sterpone
luca.sterpone@polito.it
Spare slide
Crossing-PIPB calculation

- The crossing-PIPB is calculated on the basis of the following routing parameter
  - \( \tau = RC \) (sum of all the fan-out and fan-in contributions)
  - Logic gates manhattan distance
  - Size weight associated to destination gates

Output Pulse Width \((x)\) = Input Pulse Width \((x)\) \times K(x)_{\text{broadening}}
Computing $K_{broadening}$

SETA flow

1. Netlist to PDD
2. Circuit Allocated Graph
3. SETA Algorithm

Diagram:
- $K_{broadening}$
- Gate size weight
- Decrease wire length
- Increase wire length
- $\Sigma PIB$ [ns/gate size weight]
## SET sensitivity report: an example

<table>
<thead>
<tr>
<th>FF id and position (X,Y)</th>
<th>Source SET</th>
<th>Destination SET</th>
<th>Destination SET / Clock period</th>
<th>Broadening</th>
<th>% filtering gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>-- D FF[#]</td>
<td>P S[ns]</td>
<td>P D[ns]</td>
<td>Broad[ns]</td>
<td>Sens[%]</td>
<td>Gain[%]</td>
</tr>
<tr>
<td>-- 230(81,48)</td>
<td>0.487994</td>
<td>0.006957</td>
<td>-0.481037</td>
<td>0.006957</td>
<td>98.574448</td>
</tr>
<tr>
<td>-- 332(70,4)</td>
<td>0.487994</td>
<td>0.000206</td>
<td>-0.487788</td>
<td>0.000206</td>
<td>99.957863</td>
</tr>
<tr>
<td>-- 388(57,31)</td>
<td>0.487994</td>
<td>0.000000</td>
<td>-0.487994</td>
<td>0.000000</td>
<td>100.000000</td>
</tr>
<tr>
<td>-- 458(69,10)</td>
<td>0.487994</td>
<td>0.938037</td>
<td>0.450043</td>
<td>0.938037</td>
<td>-92.223206</td>
</tr>
<tr>
<td>-- 1953(35,15)</td>
<td>0.487994</td>
<td>0.038000</td>
<td>-0.449994</td>
<td>0.038000</td>
<td>92.213112</td>
</tr>
<tr>
<td>-- 2052(60,36)</td>
<td>0.487994</td>
<td>0.000610</td>
<td>-0.487384</td>
<td>0.000610</td>
<td>99.875076</td>
</tr>
<tr>
<td>-- 2375(86,37)</td>
<td>0.487994</td>
<td>0.038000</td>
<td>-0.449994</td>
<td>0.038000</td>
<td>92.213112</td>
</tr>
<tr>
<td>-- 2406(82,30)</td>
<td>0.487994</td>
<td>0.045002</td>
<td>-0.442992</td>
<td>0.045002</td>
<td>90.778137</td>
</tr>
</tbody>
</table>
## Circuit characteristics

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>Device Type</th>
<th>Sensitive Nodes [#]</th>
<th>FFs [#]</th>
<th>Propagation Path [#]</th>
<th>SETA elaboration time [min]</th>
</tr>
</thead>
<tbody>
<tr>
<td>B04</td>
<td>A3P600</td>
<td>493</td>
<td>67</td>
<td>49,512</td>
<td>54</td>
</tr>
<tr>
<td>B05</td>
<td>A3P600</td>
<td>415</td>
<td>66</td>
<td>19,820</td>
<td>12</td>
</tr>
<tr>
<td>B12</td>
<td>A3P600</td>
<td>565</td>
<td>123</td>
<td>5,717</td>
<td>4</td>
</tr>
<tr>
<td>B13</td>
<td>A3P250</td>
<td>162</td>
<td>50</td>
<td>518</td>
<td>0.3</td>
</tr>
<tr>
<td>8051</td>
<td>A3P1000</td>
<td>3,414</td>
<td>249</td>
<td>1,772,044</td>
<td>642</td>
</tr>
</tbody>
</table>
## SETA analysis data

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>SET pulses evaluated [#]</th>
<th>SET pulse masked [#]</th>
<th>SET pulse observed [#]</th>
<th>SET pulse observed [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>B04</td>
<td>6,902</td>
<td>6,747</td>
<td>155</td>
<td>2.25</td>
</tr>
<tr>
<td>B05</td>
<td>5,810</td>
<td>5,711</td>
<td>99</td>
<td>1.70</td>
</tr>
<tr>
<td>B12</td>
<td>7,910</td>
<td>7,601</td>
<td>309</td>
<td>3.91</td>
</tr>
<tr>
<td>B13</td>
<td>2,268</td>
<td>2,057</td>
<td>211</td>
<td>9.30</td>
</tr>
<tr>
<td>8051</td>
<td>47,796</td>
<td>47,557</td>
<td>239</td>
<td>0.50</td>
</tr>
</tbody>
</table>