Single Event Transient Effects on Microsemi ProASIC Flash-based FPGAs: analysis and mitigation

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Motivations and Goals

- Evaluation of Single Even Transients (SETs) impact on complex designs is an increasing challenge
- Their analysis have to face several issues
  - Simulation

    Model is intrinsically approximative, simulation campaigns take long time
  - Effective analysis

    Laser and Radiation testing are expensive and not applicable at the design early stage
- A CAD tool able to analyze and reduce the impact of SETs affecting VLSI technology is very welcome
  - Early stage design analysis
  - Fast and effective analysis

Outline

- Introduction
- Single Event Transient phenomena
- Preliminary studies on Flash-based FPGAs
- Gates characterization – PIPB effect
- SETA main flow
  - Main routines
  - SET generation
  - SET propagation
- Tool execution and experimental results
- Conclusions

Introduction

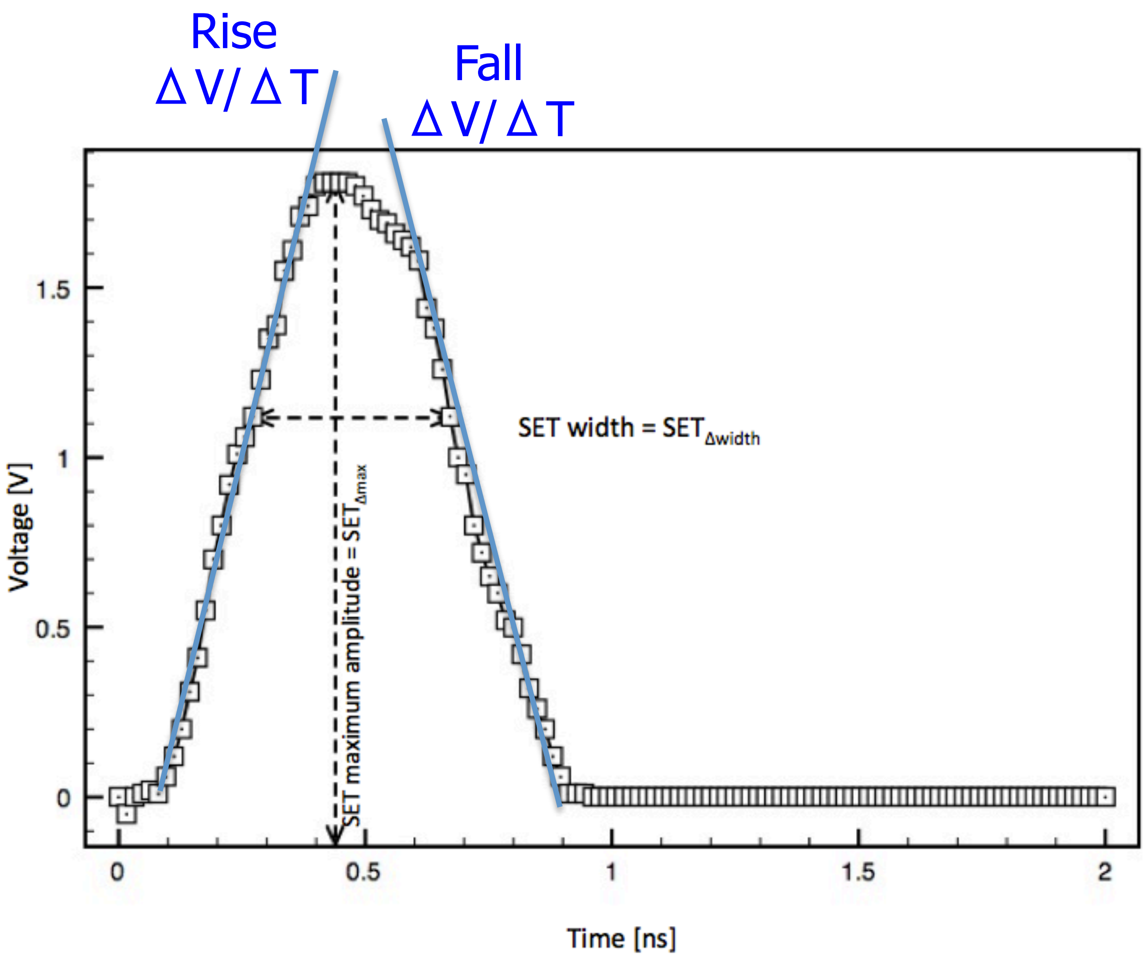
- Different scenarios may influence SET propagation
  - Logical masking
  - Electrical broadening or filtering
  - Latching window
- Not all the SETs are transformed in circuit errors
- SET sensitivity is intrinsically related to the technology cell
  - Different sensitivity figures

Source of SET effects

- Generation of SET effects is due to the injunction of charge collection
  - When a charged particle crosses a junction area, it generates an amount of current, provoking a “glitch”
- Propagation of voltage glitches may be for notable distances
- SET may become indistinguishable from normal signal

Single Event Transient - info

- SET can be defined considering four main parameters:
  - SET width
  - SET amplitude
  - Rise ΔV/ΔT
  - Fall ΔV/ΔT



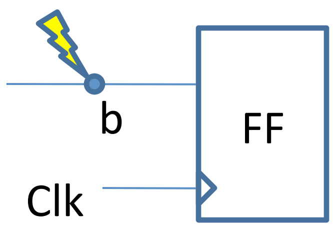
Single Even Transient Phenomena

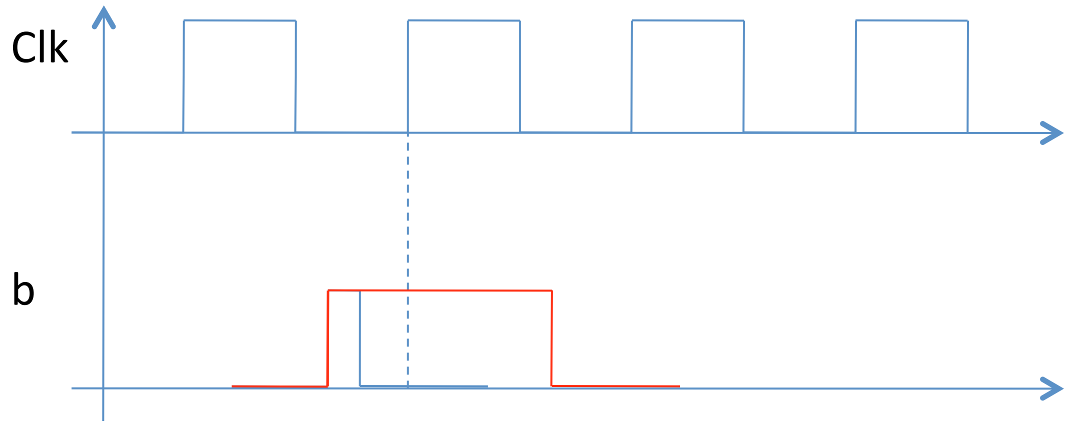
- Two transitions are possible
  0-1-0 or 1-0-1
- SET is generated into the sensitive area of a logic gate
- It propagates until a sequential element is reached
- During the propagation the SET may pass through different gates:
  - INV, NAND, OR, AND, …

SET sampling

- The effect of an SET is mainly due to:
  - Location
  - Arrival time
  - Pulse's width.

Infinite number of combinations

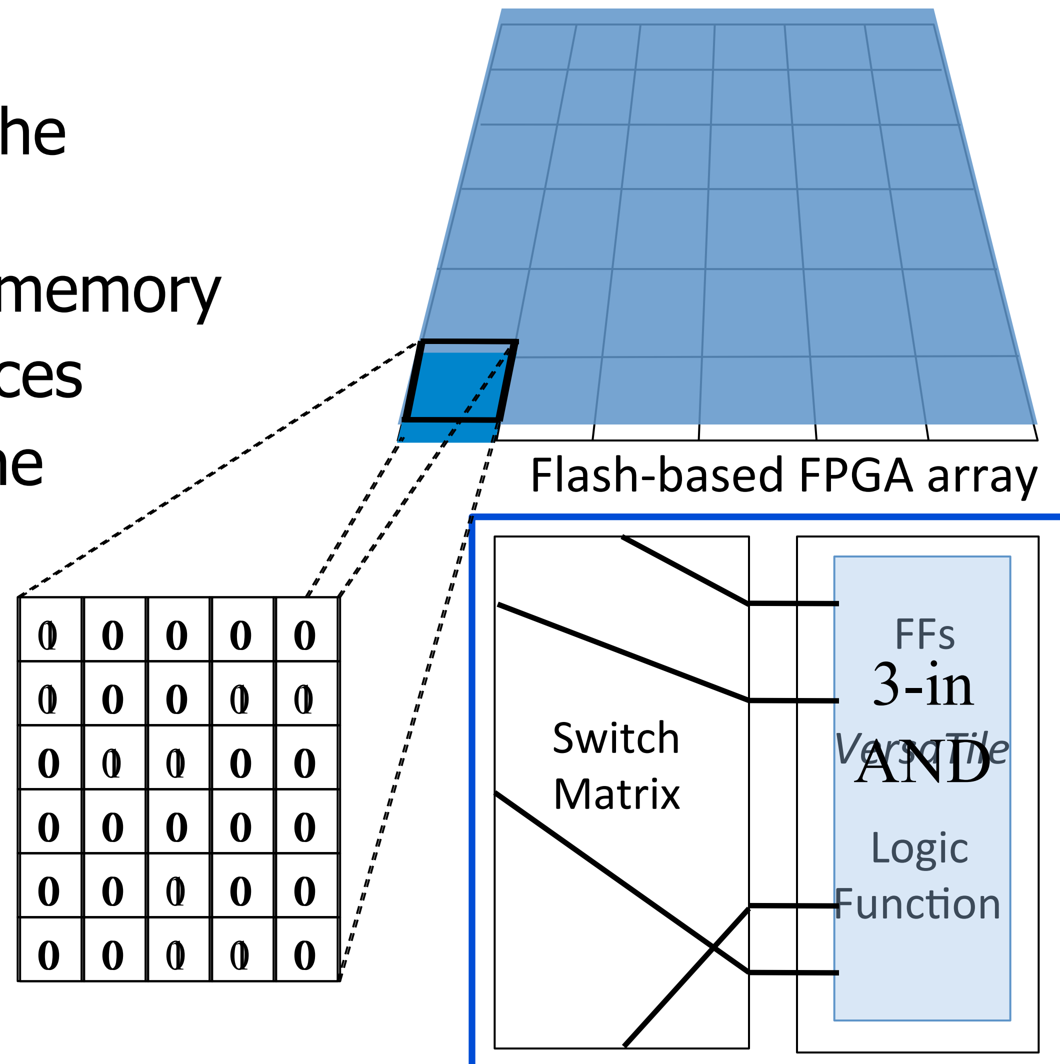




- The sensitivity of a FF can be measured as the ratio between the SET's width and the CLK period

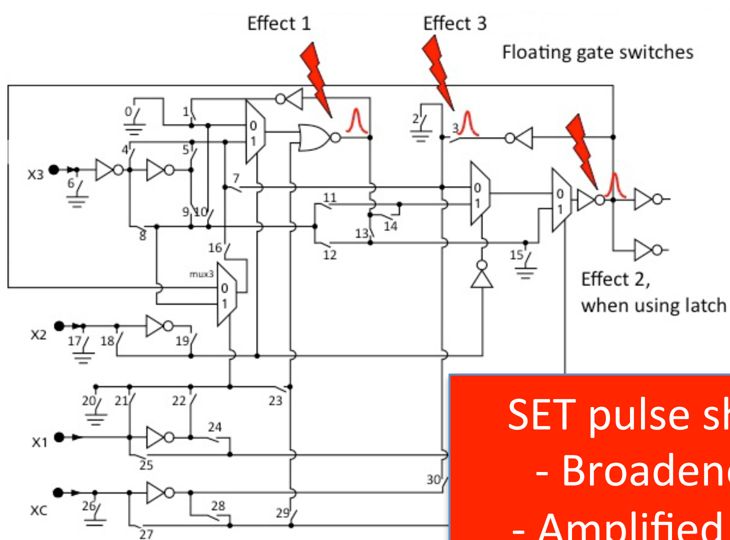
Flash-based FPGAs background

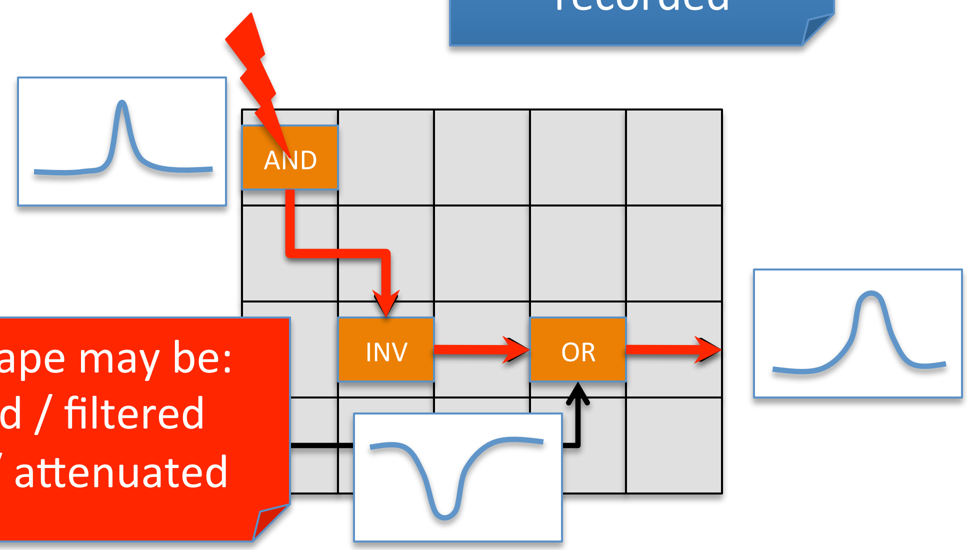
- The Flash-based FPGAs are composed of:
  Logic, I/O, Routing
- The basic element is the VersaTile logic block
- A Flash configuration memory controls all the resources
- Bitstream programs the desired circuit



Radiation effects in Flash-based FPGAs

- VersaTile may undergo to three possible effects due to radiation particle hits:
  1. Induce a pulse propagated through the logic
  2. Affect a logic cell configured as a latch → SEU
  3. Affect a junction of the floating gate → No transient effects have been recorded





SET pulse shape may be:
- Broadened / filtered
- Amplified / attenuated

SET propagation background

- SETs are generated into the sensitive area of a logic gate
  - Two transitions are possible (0-1-0 and 1-0-1)

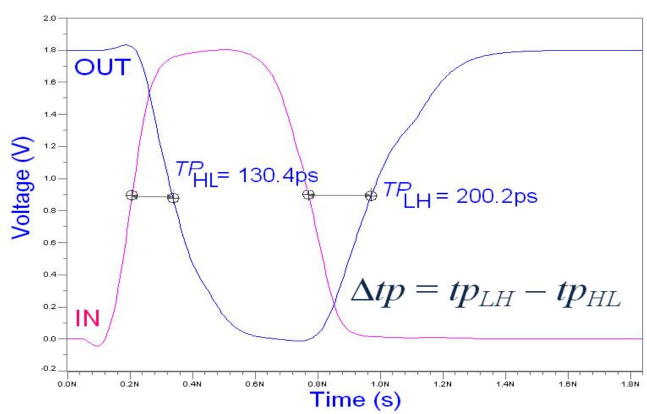
Fist Region: If($\tau_n < k*tp$) then $\tau_{n+1} = 0$

Second Region: If ($\tau_n > (k+3)*tp$) then $\tau_{n+1} = \tau_n + \Delta tp$

Third Region: If ($(k+1)*tp < \tau_n < (k+3)*tp$) then $\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta tp$

Fourth Region: If ($k*tp < \tau_n < (k+1)*tp$) then $\tau_{n+1} = (k+1)*tp(1 - e^{(k-(\tau n / tp))}) + \Delta tp$

Wirth et al, NSREC 2008
Sterpone, Battezzati, Lima RADECS 2010

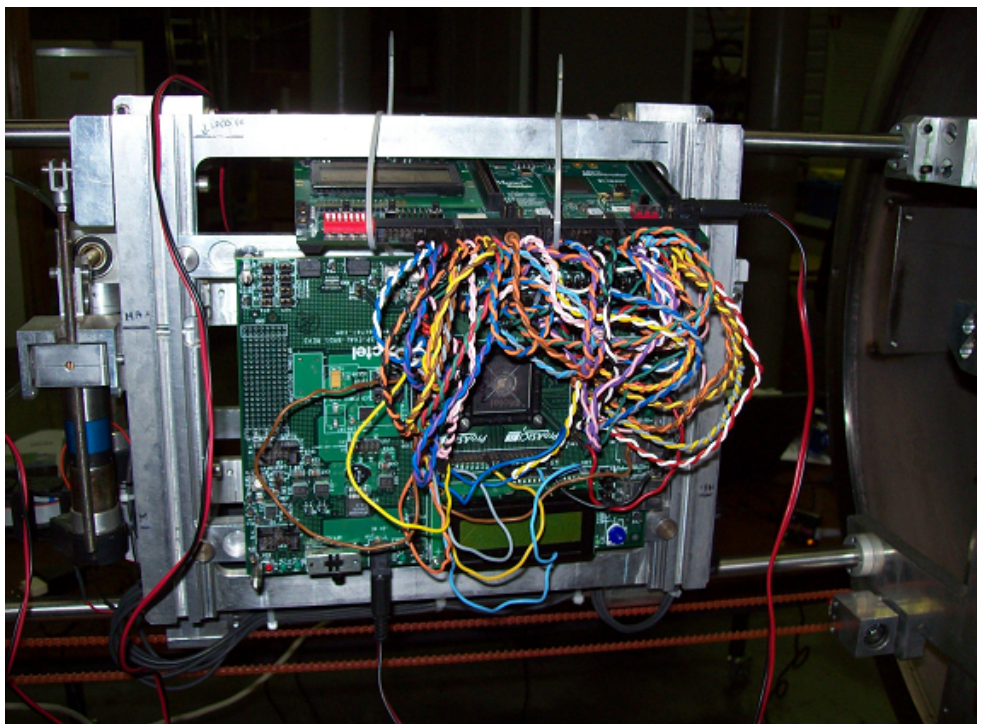


For a 1→0→1 transition Δtp is defined as:
$\Delta tp = tpHL - tpLH$

For a 0→1→0 transition Δtp is defined as:
$\Delta tp = tpLH - tpHL$

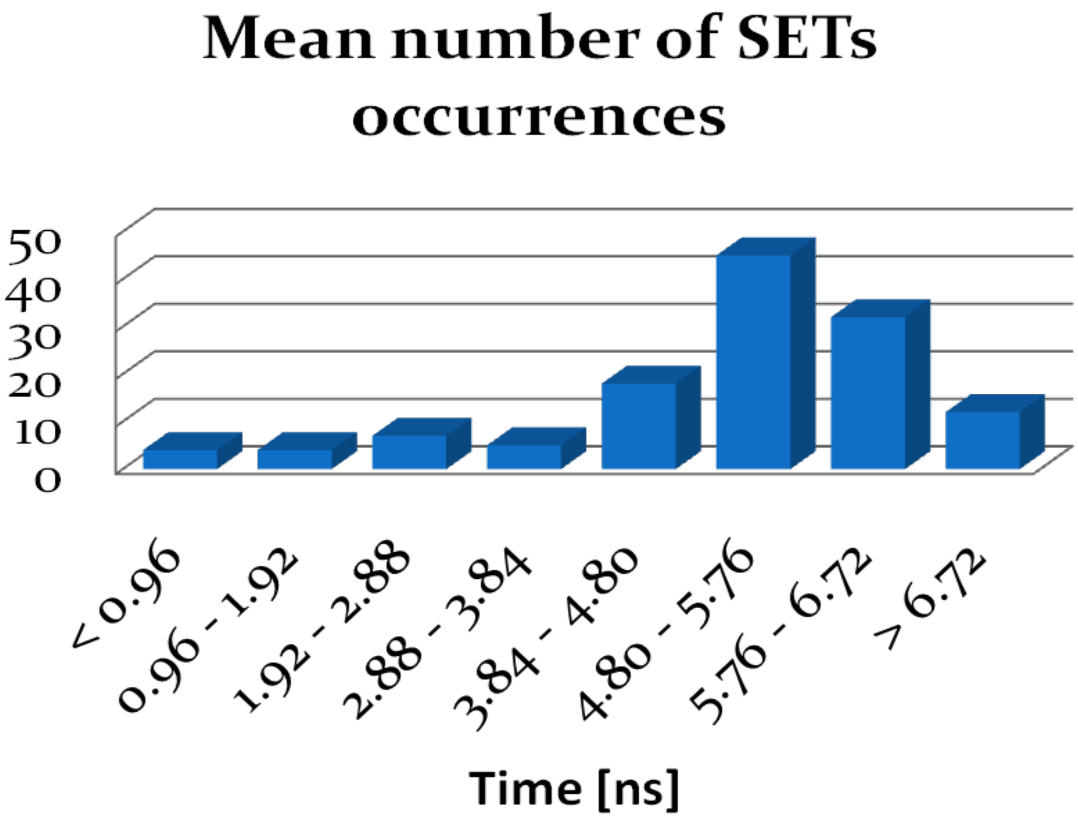
SETs on Actel Flash-based FPGAs

- Radiation tests have been executed:
  - Measurement of the pulse's width
  - Frequency impact on SEE on Flash-based FPGAs

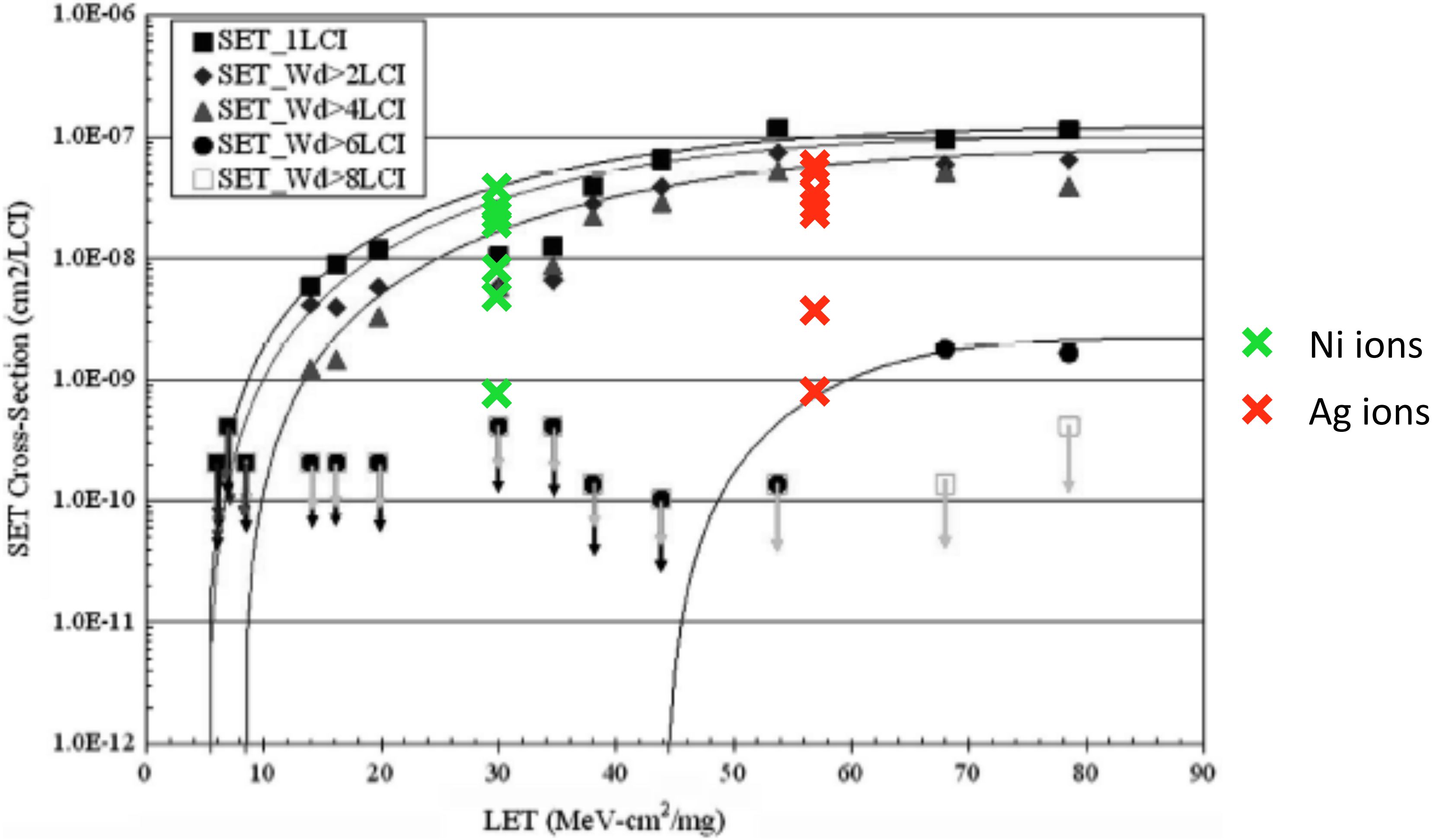


SETs on Actel Flash-based FPGAs

- Experimental results

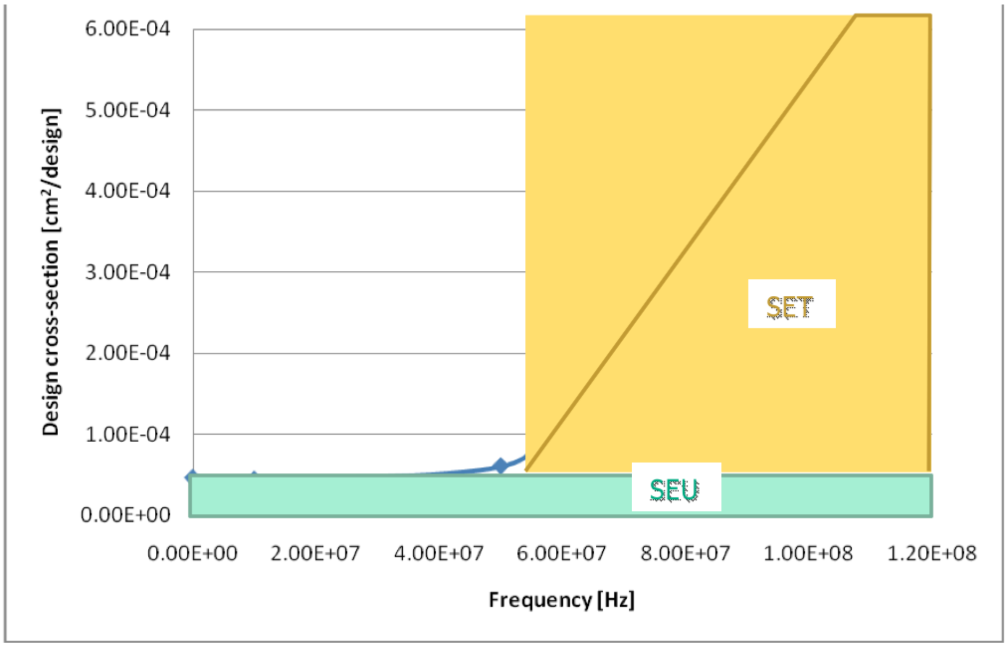


SETs on Actel Flash-based FPGAs



SETs on Actel Flash-based FPGAs

- Radiation tests performed at the HIF, Louvain-La-Neuve, Belgium
- Iodine beam LET 61.8 MeV cm^2 / mg
- DUT: pipelined multiplier



SETs on Actel Flash-based FPGAs

Circuit	FF tiles [#]	Combinational Tiles[#]	Routing resources [#]
v1	2,484	3,405	126,840
v2	2,484	3,405	252,446

Circuit	Observed events [#]	Design Cross-section
v1	710	1.052 E-04
v2	729	1.217 E-04

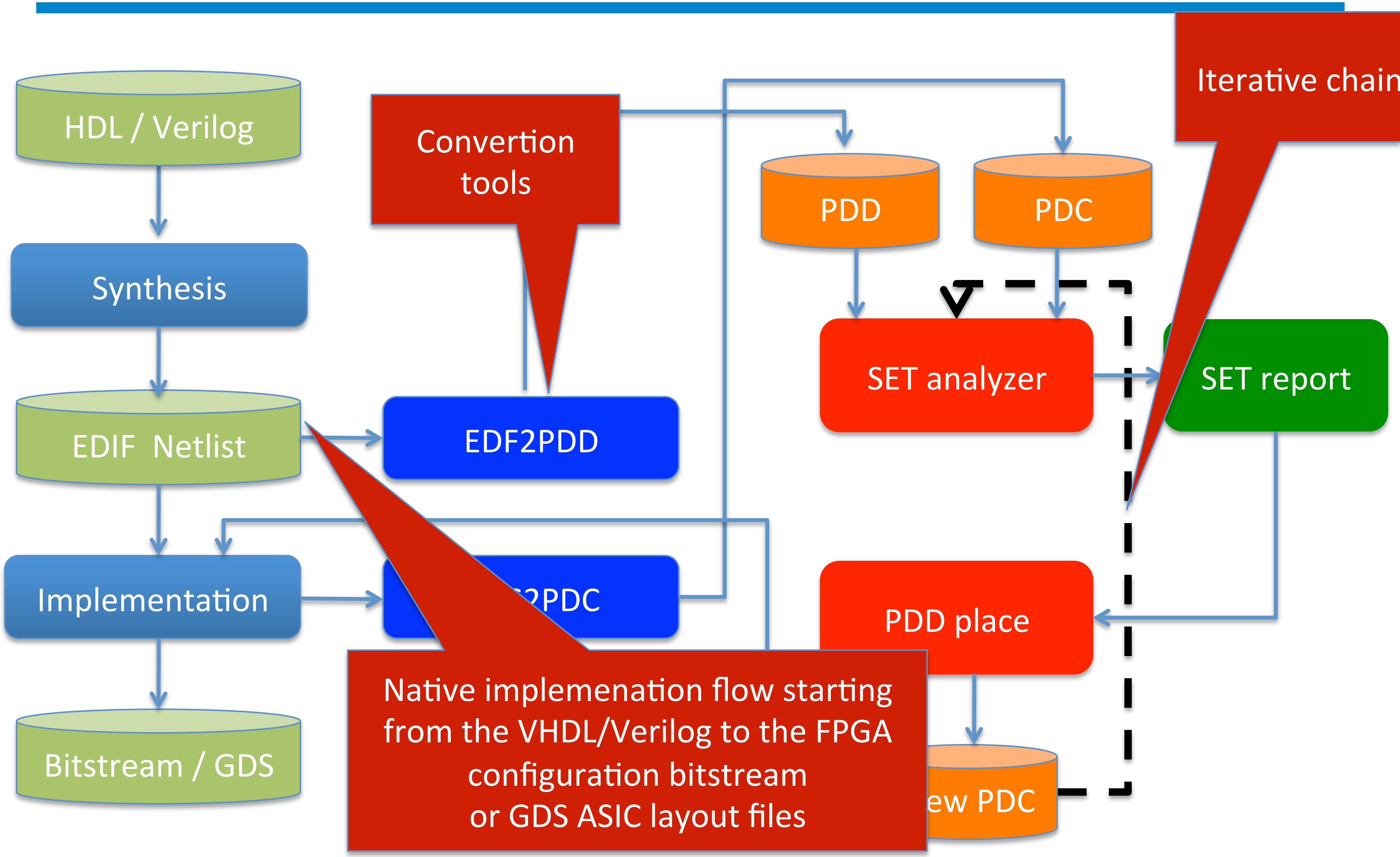
[TNS'09]

Existing CAD tools for SET analysis

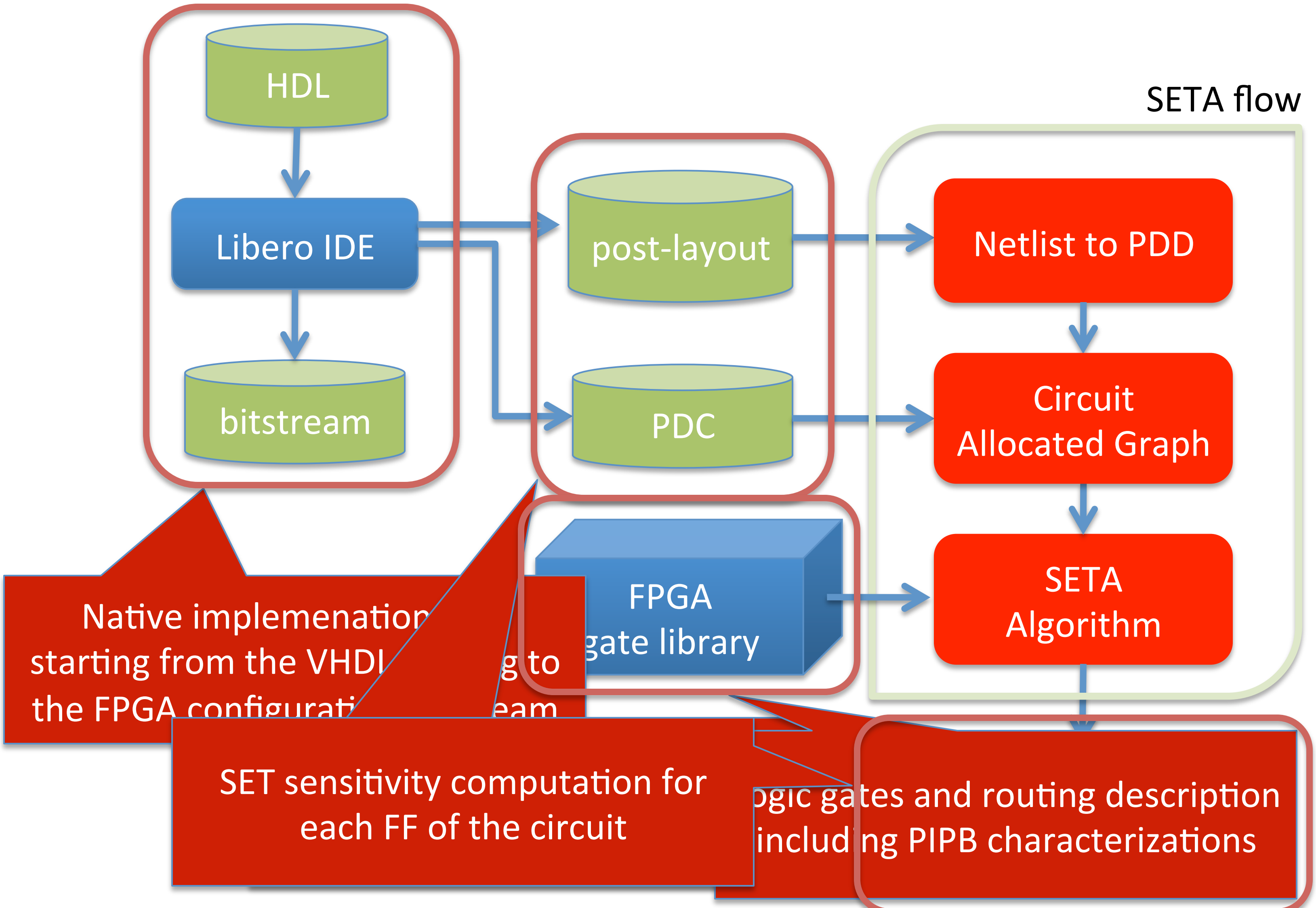
- 2D and 3D device model simulation or technology CAD (TCAD) or SPICE are generally adopted
  - effective only on a reduced portion of a circuit thousands of gates
  - very low speed
  - Cannot be realistically applied to an entire circuit
- PIPB effect is not modeled and characterized with respect to a given technology
  - Dynamic PIPB model embedded in SPICE has proven and demonstrated to be effective

Sterpone et al, TNS 2011

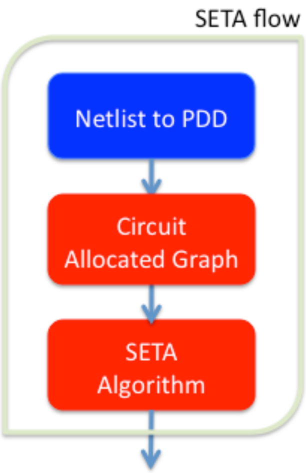
The developed CAD tool for SET



The developed SETA tool

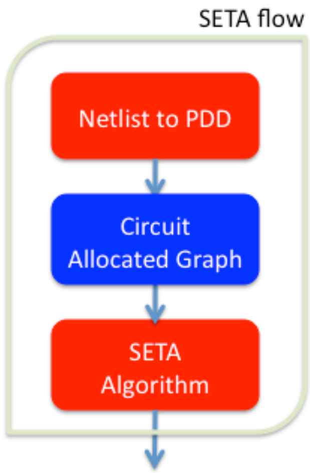


Netlist to Physical Design Description

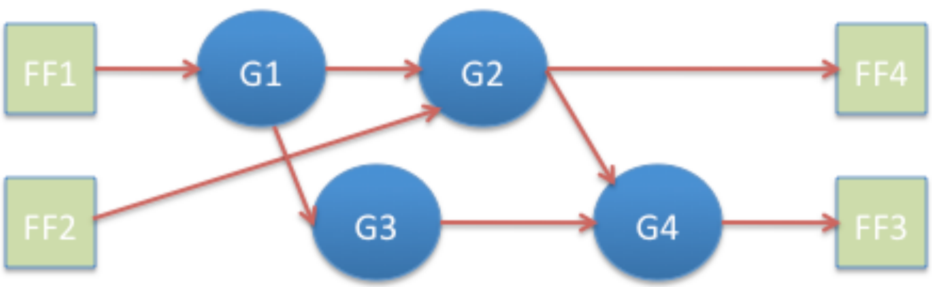


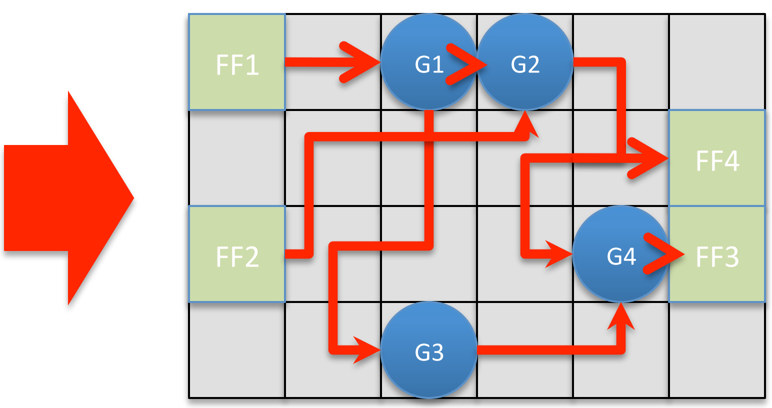
- The circuit netlist is loaded
- A directed graph structure is generated
  - I/O element, FFs, RAM/ROM pins, … are considered as terminal points
  - Logic gates are considered as crossing points
  - Interconnections are defined as direct edges between nodes

Circuit allocated graph

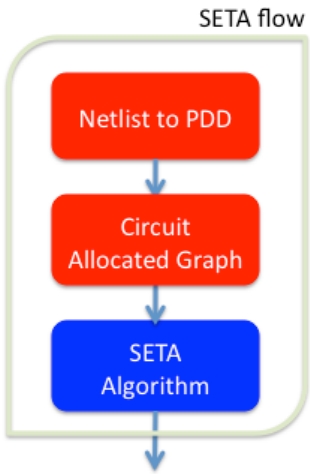


- The circuit graph is organized in a matrix-based graph
  - Vertices placed on the same layout position
  - Edges related to the FPGA routing model



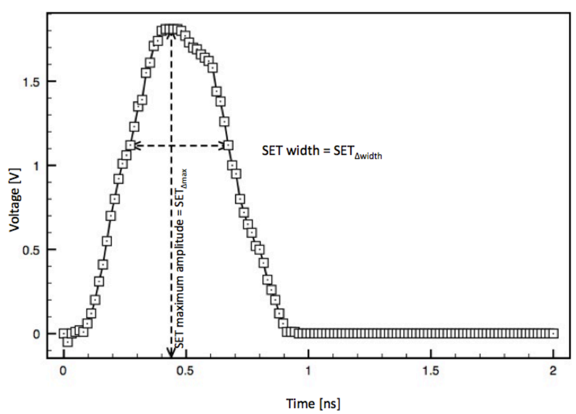


SETA algorithm



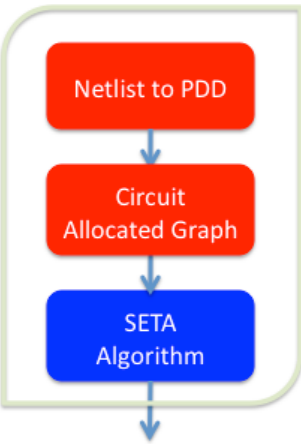
- a set of SET pulse shape is generated
  - defined as a voltage spike
  - voltage amplitude / width
  - Defined as 100.000 points (resolution of 1ps)

1. Generate the list of SET pulse: SET_{GP}
2. For each generated pulse $p \in (SET_{GP})$
   2. For each sensitive node $i \in (SN)$
   Apply pulse *p* to *i*
   Find destination node $dn \in (SN, i)$
      3. For each *dn*
      Propagate *p* on (*i*, *dn*)

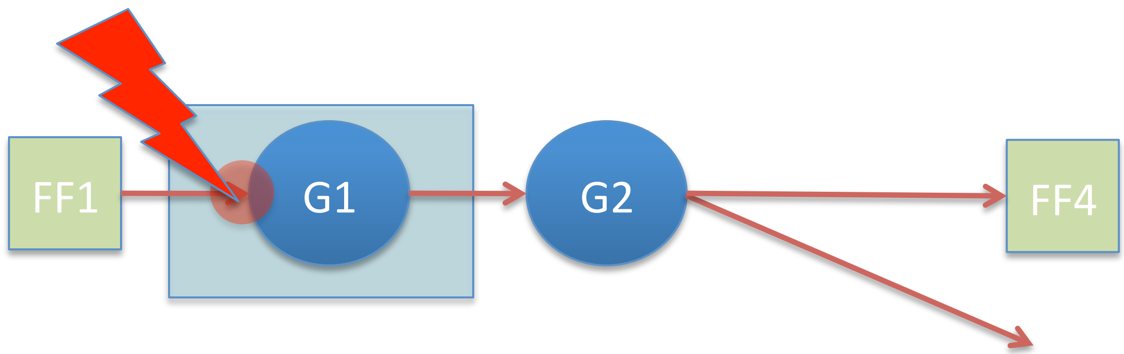


SETA algorithm

SETA flow



- The generated voltage pulse is applied to the selected sensitive node



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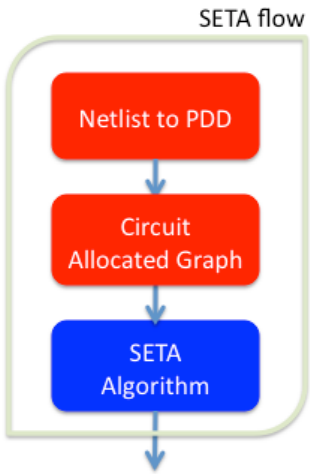
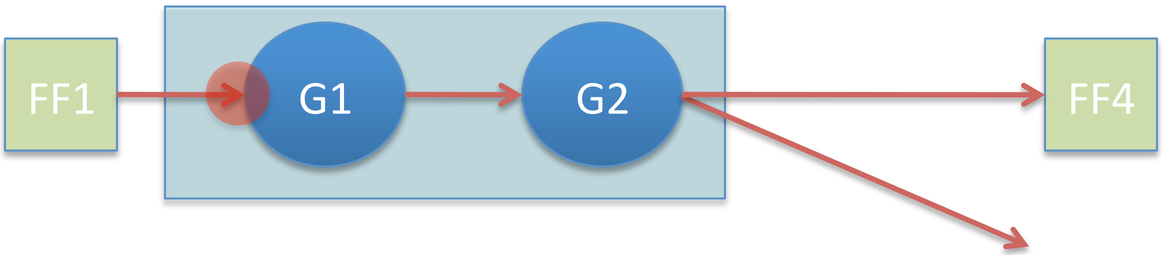
SETA algorithm



- The list of destination node is created



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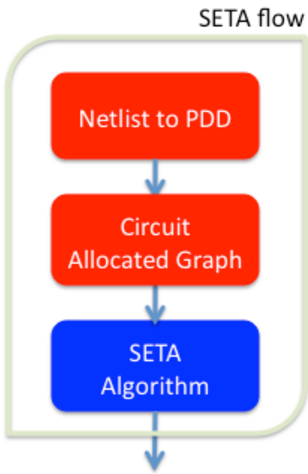
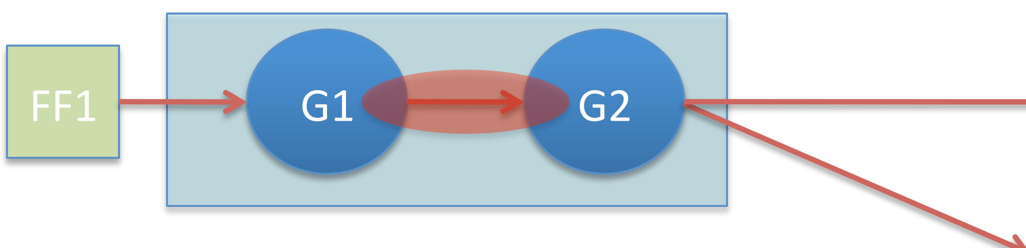
SETA algorithm



- The voltage array p is propagated through the logic element G1 to the next destination node G2
- The propagation is computed on the basis of the crossing-PIPB
- Propagation is performed assuming no-logic masking [actual version of SETA]

P_{G1} is propagated in P_{G2}

Output Pulse Width (x) = Input Pulse Width (x) x $K(x)_{broadening}$



The tool set – Microsemi / Actel

- The PDT CAD tool is compiled under Linux
  - Compatible with Windows or MaCOSx operative systems
- The tool set contains the following executables:
  - **AFL2PDD**: conversion of the EDIF netlist to the PDD file
  - **PDC_PDD**: conversion of the PDD coordinates to the Physical Design Constraint (PDC) format
  - **PDD_Place**: the placement algorithm
  - **SET_analyzer**: the SET analyzer algorithm

Step 1: generation of the files

- The first step consists on generating the support files from the Microsemi tools (IDE libero)
- Two files may be generated:
  - AFL: Flat Netlist description file

  It can be generated after the Symplify Synthesis
  - PDC (optional): Physical Constraints File

  It can be generated after the place and route phase

Step 2: generation of the PDD file

- The second step consists on the generation of the PDD file
- This operation is performed by executing:

  ./AFL2PDD design_name.afl

- The execution may require some minutes
- It generates a PDD file: **design_name.afl.pdd**

Step 2.1: the PDD file

- The PDD file contains the graph-based architecture of the circuit
  - **All the circuit logic cells are vertex**
  - **All the circuit interconnections are edges**

```
53
u1/gen_pipe_12_Pipe/Yo[8]
F DFN1E1
1 4
0
0
1
U
1 1659 A Y
1 3003 Y A
2 1846 Y A
3 2458 Y A
4 385 Y A
```

Logic node name

Type and Library name

Input / Ouput edges

Step 3: the SET analysis

- Once the PDD file is generated and there is an available PDC file it is possible to perform the SET analysis
- An example of command may be the following:

./SET analyzer name.pdd name.pdc 1 10 mine n 0.450

Step 3.1: the SET analysis

- The parameter you may use are the following:
  - Source netlist (PDD)
  - Source placement (PDC)
  - Start pulse width (1: about 8ns)
  - End pulse width
  - Name of the report generated files
  - Verbose
  - Limit for the “gate to gate”

Step 3.2: the SET analysis

- The design sensitivity ov

Gate to gate interconnection where SET are broadened more than the inserted user limit (i.e. 0.450 ns)

Logically masked pulses

-- Legenda
-- P_S: Origina
-- L_M: Logically M ulses
-- T_F: Totally Ele lly Filtered Pul
-- P_F: Partially E rically Filtered lses
-- P_B: Broadened P es
-- O_L: Gate to Gat broadening over the limit 0.450000 ns #]

--	P_S [ns]	L_M [#]	T_F [#]	P_F [#]	P_B [#]	O_L [#]
--	1.660940	605	0	33	82	1325
--	1.383990	605	0	33	82	361
--	1.186026	605	0	33	82	237
--	1.038044	605	0	33	82	189
--	0.923033	605	0	33	82	41
--	0.830024	605	0	33	82	39
--	0.755016	605	17	16	82	5070
--	0.693010	605	17	16	82	5064
--	0.639004	605	18	2	95	5064
--	0.593000	605	18	2	95	5064
--	0.553996	605	18	2	95	5062
--	0.519993	605	18	2	95	5062
--	0.487994	605	19	1	95	5058
--	0.461994	605	19	1	95	5220

Step 3.3: SET detailed report

- Further reports are generated for
  - **Max_pulse_report**: it provides for each F
  - **Max_broad_rerport**: it provides for
    broadening effect
  - **Gate 2 Gate**: it provides the broadening effect specifically observed between a couple of logic gates inside of the design
  - **FF reports**: it provides several detailed information on the pulses observed on each FF

Can be used for selective filtering technique application

SET sensitivity report: an example

-- D FF[#]	P S[ns]	P D[ns]	Broad[ns]	Sens[%]	Gain[%]
-- 230(81,48)	0.487994	0.006957	-0.481037	0.006957	98.574448
-- 332(70,4)	0.487994	0.000206	-0.487788	0.000206	99.957863
-- 388(57,31)	0.487994	0.000000	-0.487994	0.000000	100.000000
-- 458(69,10)	0.487994	0.938037	0.450043	0.938037	-92.223206
-- 1953(35,15)	0.487994	0.038000	-0.449994	0.038000	92.213112
-- 2052(60,36)	0.487994	0.000610	-0.487384	0.000610	99.875076
-- 2375(86,37)	0.487994	0.038000	-0.449994	0.038000	92.213112
-- 2406(82,30)	0.487994	0.045002	-0.442992	0.045002	90.778137

FF id and position (X,Y)

Source SET

Destination SET

Broadening

Destination SET / Clock period

% filtering gain

Step 4: the PDD placement

- The placement maybe performed independently from the SET analysis
- This operation is performed by executing:

./PDD_place source_design.pdd destination_design.pdd X Y N 1

- The execution may require several minutes

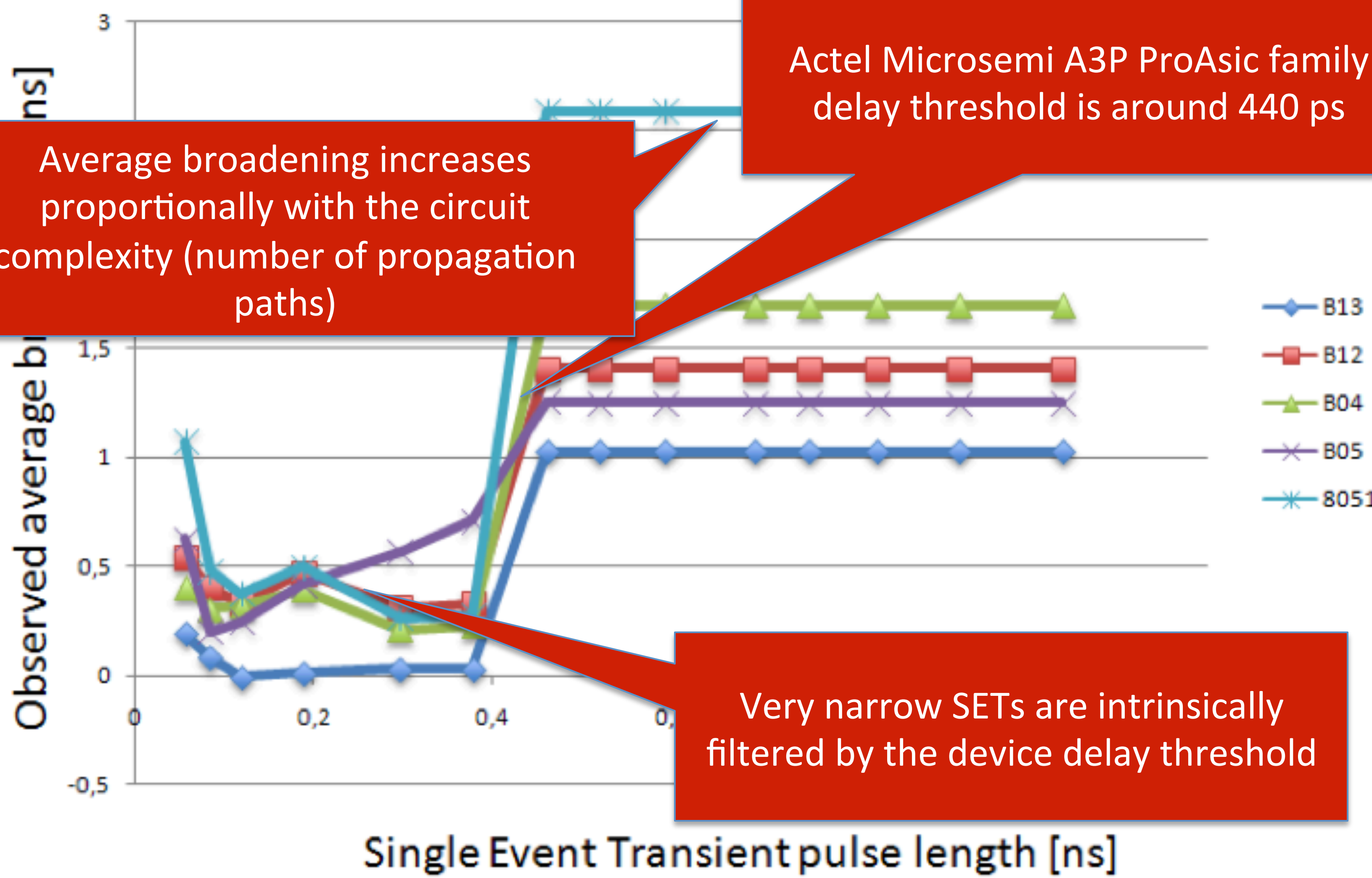
Circuit characteristics

Circuit Name	Device Type	Sensitive Nodes [#]	FFs [#]	Propagation Path [#]	SETA elaboration time [min]
B04	A3P600	493	67	49,512	54
B05	A3P600	415	66	19,820	12
B12	A3P600	565	123	5,717	4
B13	A3P250	162	50	518	0.3
8051	A3P1000	3,414	249	1,772,044	642

SETA analysis data

Circuit Name	SET pulses evaluated [#]	SET pulse masked [#]	SET pulse observed [#]	SET pulse observed [%]
B04	6,902	6,747	155	2.25
B05	5,810	5,711	99	1.70
B12	7,910	7,601	309	3.91
B13	2,268	2,057	211	9.30
8051	47,796	47,557	239	0.50

Average broadening

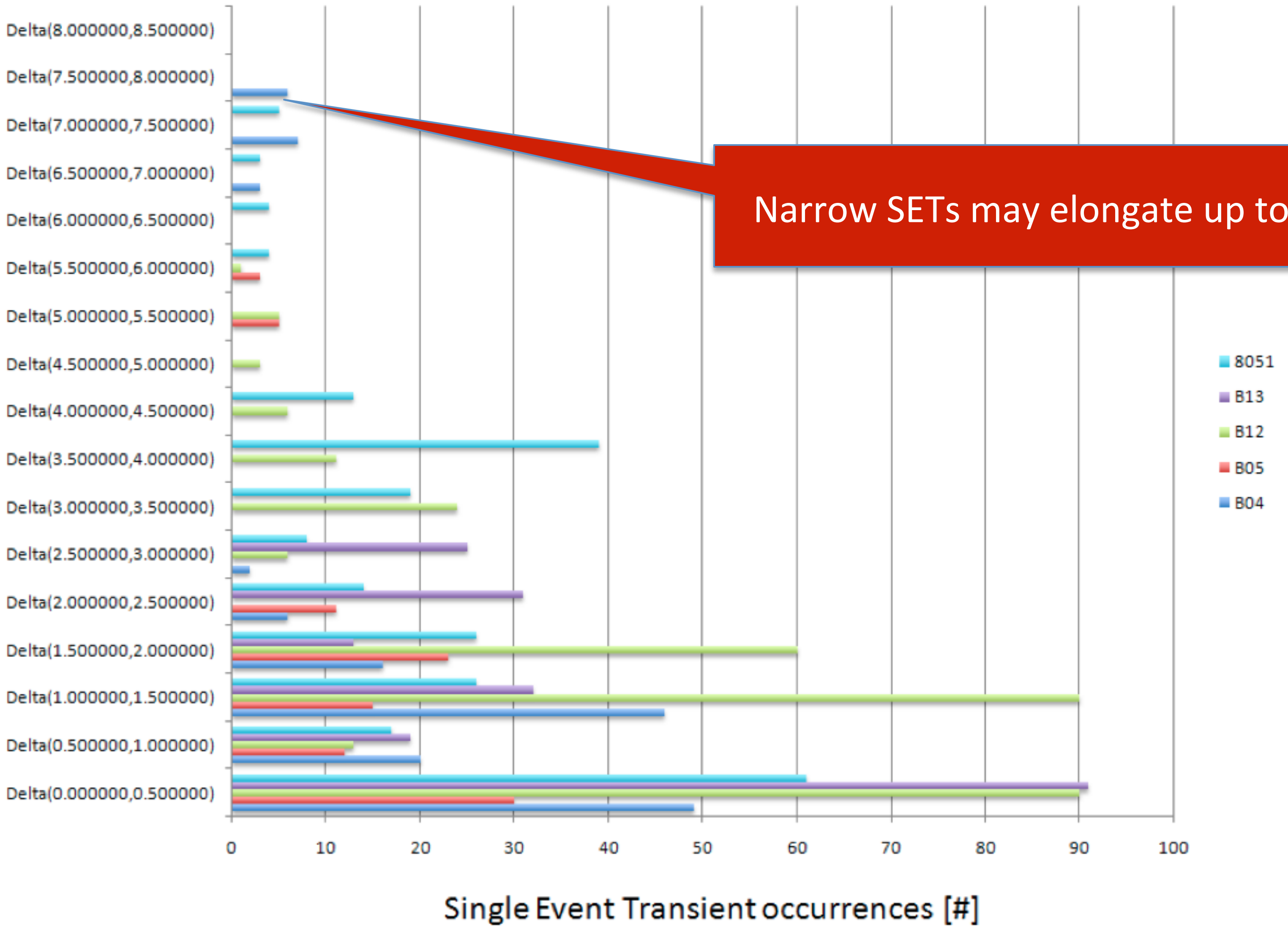


Actel Microsemi A3P ProAsic family delay threshold is around 440 ps

Average broadening increases proportionally with the circuit complexity (number of propagation paths)

Very narrow SETs are intrinsically filtered by the device delay threshold

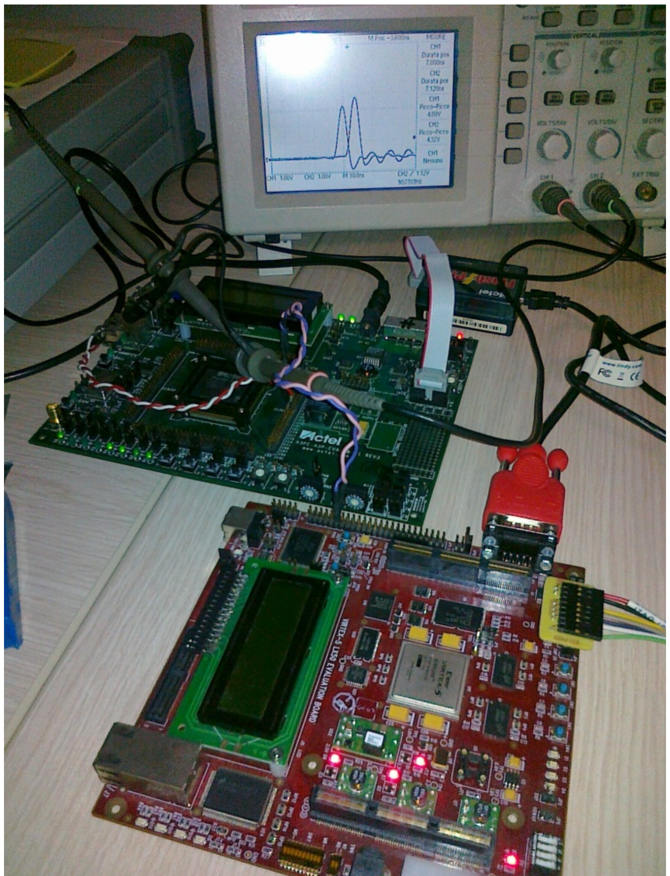
SET occurrences



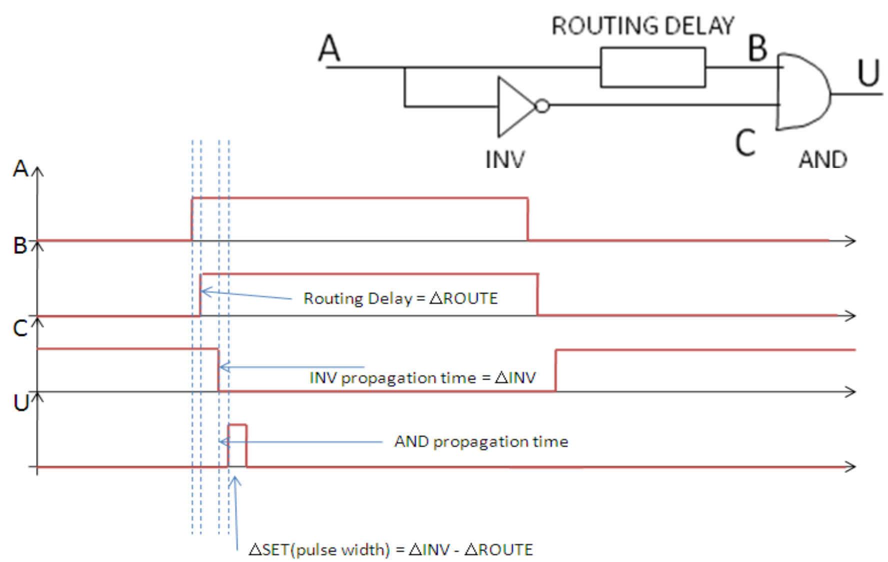
Luca Sterpone, SET project, ESA final presentation days

Results validation

- Results have been validated through electrical fault injection



- Selective injection of SET pulses
- SETs counted by a sampler circuit on a Virtex-5 FPGA
- Injection is performed instrumenting the circuits



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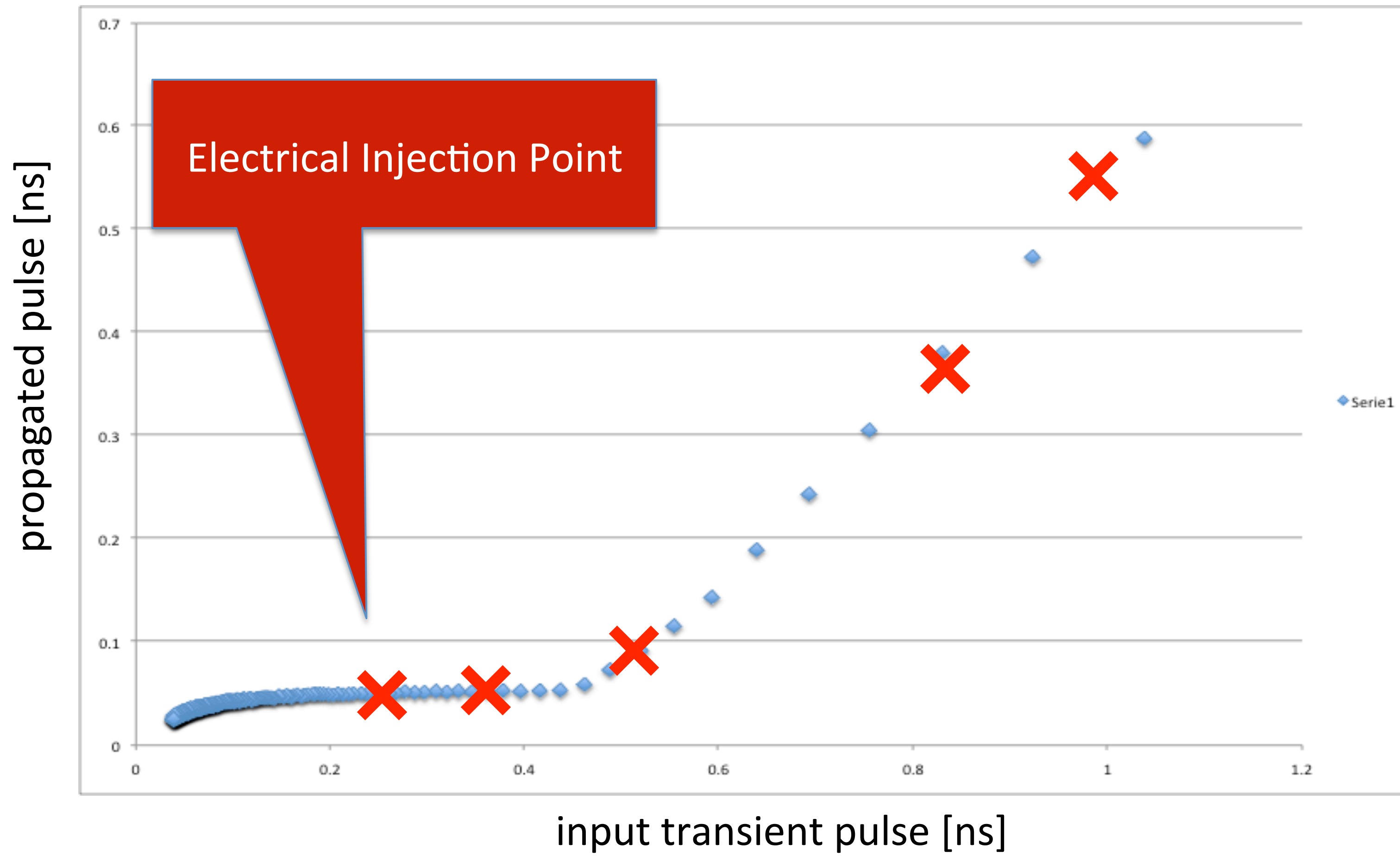


RISC hardening analysis

- Circuits characteristics

RISC version	Logic Gates	FFs
Unhardened	1,401	1,156
Full TMR+ GG	20,808	3,468
TMR + FF	4,203	3,468
PDT CAD tool	5,514	3,468

RISC hardening analysis

- SET analysis results by means of fault simulation

RISC version	SETs	SEUs
Unhardened	1,401	1,839
Full TMR+ GG	1,562	0
TMR + FF	2,302	0
PDT CAD tool	2	0

Conclusions

- A CAD tool – SETA – is available and able to automatically evaluate the SET sensitivity of complex circuits
  - Applied on Flash-based FPGAs
  - Embedding the PIPB effect characterization
- The SETA tool allows to
  - Investigate the behavior of individual FFs
  - Selectively apply mitigation solutions (guard-gates, selective TMR, others…)
- SETA results embedded into P&R flow
  - **Completely DONE for the placement**

Future works

- Compare the SETA analysis with laser and radiation testing
- Creating an IDE user interface and web-user access
- Extend the SETA flow to ASIC gate library

Thank you..

- For your attention

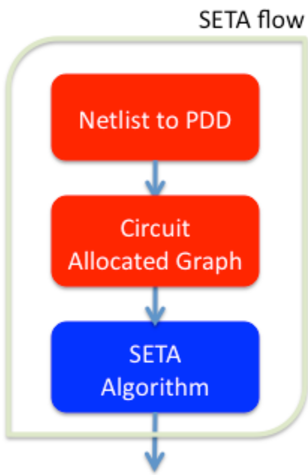
  Question and comments:

  Luca Sterpone

  luca.sterpone@polito.it

Spare slide

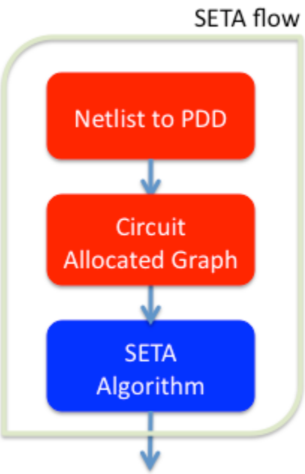
Crossing-PIPB calculation

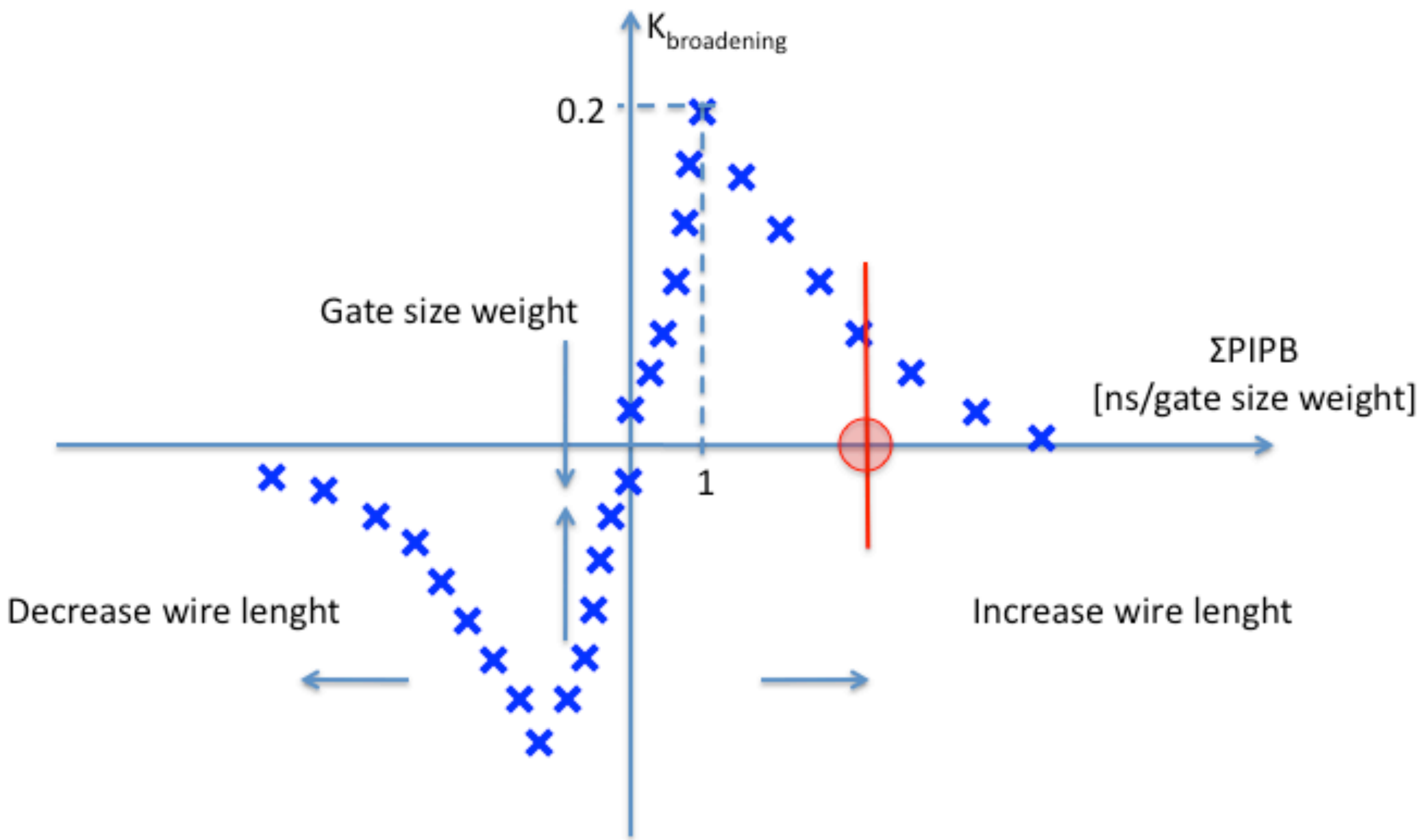


- The crossing-PIPB is calculated on the basis of the following routing parameter
  - $\tau =$ RC (sum of all the fan-out and fan-in contributions)
  - Logic gates manhattan distance
  - Size weight associated to destination gates

$$\text{Output Pulse Width }(x) = \text{Input Pulse Width }(x) \times K(x)_{\text{broadening}}$$

Computing $K_{broadening}$





SET sensitivity report: an example

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-- 332(70,4)	0.487994	0.000206	-0.487788	0.000206	99.957863
-- 388(57,31)	0.487994	0.000000	-0.487994	0.000000	100.000000
-- 458(69,10)	0.487994	0.938037	0.450043	0.938037	-92.223206
-- 1953(35,15)	0.487994	0.038000	-0.449994	0.038000	92.213112
-- 2052(60,36)	0.487994	0.000610	-0.487384	0.000610	99.875076
-- 2375(86,37)	0.487994	0.038000	-0.449994	0.038000	92.213112
-- 2406(82,30)	0.487994	0.045002	-0.442992	0.045002	90.778137

FF id and position (X,Y)

Destination SET

Destination SET / Clock period

Source SET

Broadening

% filtering gain

Circuit characteristics

Circuit Name	Device Type	Sensitive Nodes [#]	FFs [#]	Propagation Path [#]	SETA elaboration time [min]
B04	A3P600	493	67	49,512	54
B05	A3P600	415	66	19,820	12
B12	A3P600	565	123	5,717	4
B13	A3P250	162	50	518	0.3
8051	A3P1000	3,414	249	1,772,044	642

SETA analysis data

Circuit Name	SET pulses evaluated [#]	SET pulse masked [#]	SET pulse observed [#]	SET pulse observed [%]
B04	6,902	6,747	155	2.25
B05	5,810	5,711	99	1.70
B12	7,910	7,601	309	3.91
B13	2,268	2,057	211	9.30
8051	47,796	47,557	239	0.50