SCOC3
A brand-new heart for space missions

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Agenda

1. SCOC3 Features
2. Development History
3. Validation results
4. Radiation test results
5. Development Kit
6. Commercialization support
1. SCOC3 Features
Introduction to the SCOC3 ASIC

**SCOC3** is the **S**pacecraft **C**ontroller **O**n a **C**hip based on **LEON3FT**

- Tailored for **platform OBC** (spacecraft control, AOCS)
- Also very well suited for **payload computers**
SCOC3 Key Features (1/2)

All the core functions of a platform computer on a single chip

- **LEON3FT + GRFPU** (with large caches and MMU) provide **97 MIPS @ 80MHz**
- **CCSDS TM/TC interface:** direct coupling with transponders
  - 7 x **SpaceWire-RMAP**
  - 2 x **1553**
  - 2 x **CAN**
  - 4 x **UART**
- **CCSDS Time Management**
- Compatibility with both **SDRAM** and **SRAM**
  - Can address up to 20 Gbits
- **Security module** as an option
  - (authentication, deciphering)
- **Debug facilities** (IP Monitor, LEON DSU)
SCOC3 Key Features (2/2)

All the core functions of a platform computer on a single chip

▶ ATC18RHA **ASIC**
▶ Typical power consumption:
  ▶ 1W @32MHz
  ▶ 1.9W @80MHz
▶ Very good radiation performance
  ▶ 300 krad total dose
  ▶ SEU < 10^{-5} / day
  ▶ Latchup free
SCOC3 therefore groups **all the digital functions of a platform OBC on a single chip:**

- **Processing resources** for the flight mission SW
- **TM/TC services** & interfaces with the RF communication chain
- **General communication services** with the avionics and payload equipments through an on-board communication bus
- **Time synchronization** and distribution
- **Failure tolerant architecture** based on redundancy & reconfiguration

SCOC3 enables **significant gains** in **size, mass** and **power** at OBC level (enabled to shrink Astrium OBC from 3 boards to 2 smaller boards)
SCOC3 Architecture

CPU subsystem
SCOC3 Architecture

CPU + IO + TMTC subsystems
SCOC3 key competitive advantages

➢ **Processing performance** depends on:
  ➢ core performance
    • SCOC3 uses LEON3FT core
  ➢ cache size
    • SCOC3 has larger caches (2x to 4x more than competitors)
  ➢ memory throughput & latency
    • SCOC3 has 2x memory throughput thanks to the 2 memory buses
  ➢ clock frequency
    • SCOC3 runs at 80MHz over full spatial range, with SRAM as well as SDRAM
SCOC3 key competitive advantages

- Additional **advantages** of 2 AHB buses:
  - IO traffic does not impact CPU
    - Application validation eased (WCET calculation in particular)
  - IO bus can operate at lower frequency than CPU to reduce power
    - when CPU runs at 80MHz, TM/TC is slowed down to 40MHz
    - power gain of 25% at 80MHz (1.9W instead of 2.5W)

- **Autonomous** and **SW-friendly** modules
SCOC3 key competitive advantages

▶ All the modules and IOs are available simultaneously (except multiplexing on each of the 2 CAN/1553 ports)

▶ SDRAM Scrubbing is performed automatically in HW

▶ SCOC3 is **Flight-proven**

▶ **Complete ecosystem** (Qualified Simulator and Basic SW in particular)
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2. SCOC3 Development History
Development History

2001-2003: SCOC prototype design, SCOC1

› Selection of functions
› Preliminary architecture definition (based on LEON1)
› Development of a HW demonstrator (BLADE board)
› Development of a SpW IP Core
› Supported by ESA contract #13345/99/NL/FM “Building Blocks for System On-a-Chip” and Astrium internal funding

Spot 6 launch
Sep. 2012

Development History


SCOC1 SCOC2 SCOC3

TRL 9 — TRL 8 — TRL 7 — TRL 6 — TRL 5 — TRL 4 — TRL 3 — TRL 2 — TRL 1
2003-2006: Refinement of SCOC1 into **SCOC2**

- Upgrade to LEON2FT
- Evaluation of several IP Cores
- Performance assessment of different architectures
- Supported by Astrium internal funding
**Development History**

**2006-2009:** Development of the **SCOC3** System-on-Chip (1/2)

- Upgrade to LEON3FT
- Development of new IP Cores
- Architectural design and verification (simulation and FPGA prototyping)
- Supported by ESA contract #20167/06/NL/FM “Further Development of the Spacecraft Controller on a Chip” and Astrium internal funding
2006-2009: Development of the **SCOC3** System-on-Chip (2/2)

- Gate-level design and Layout
- Manufacturing
- ASIC Validation
- Dev. of a Demonstration Basic SW
- Radiation test
- Supported by ESA contract #22358/09/NL/JK “SCOC3 ASIC Manufacturing, Test and Validation”, and Astrium internal funding
SCOC3 Development Process

Kick-off (Sept 2006)

Feasibility (incl. architecture)

Development of New IPs
coding, synthesis, IP-level verification

SoC Integration

SoC Verification

RTL simulations
HW verif. on FPGA
SW verif. on FPGA breadboard

Gate-level simulations

Gate-level design
Layout

Foundry

Prototype
validation

Prototype approval (Oct 2009)

Prototype Board (July 2007)

Logic Review (Sept 2008)

Design Review (Dec 2008)

ASIC prototypes (May 2009)

Prototype Board (July 2007)

10 months

19 months

FPGA

Extensive verification phase

Flight Models (May 2010)

Flight Models

production

SW verif. on FPGA breadboard
HW verif. on FPGA

19 months

Flight Models

10 months
3. Validation Results
Verification results

SCOC3 Verification (before the foundry):

- IP-level simulations
- Top-level verification
  - RTL simulations
  - Gate-level simulations
  - HW verif. on FPGA breadboard
  - SW verif. on FPGA breadboard
- Verification reports
Validation results

▶ SCOC3 validation (on the ASIC prototype):
  ▶ hardware validation:
    • functional validation (numerous HW-oriented tests performed in various temperature and voltage conditions, with various clock frequencies)
    • electrical characterization (oscilloscope measurements of signals, memory accesses; power consumption measurements)
    • functional characterization (measurement of operating limits on clock frequencies, voltages, wait states)
  ▶ software validation:
    • validating the functionality from a software point of view (avionics-level tests defined in co-engineering between the SW team and the Data Handling architect, with performance measurements in representative and worst-case scenarii)
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4. Radiation Test Results
Objective of the Radiation Test

- The objective of the radiation test was to **confirm the existing radiation analysis** by validation of some experimental results
  - Using ATMEL data, test sensitivities were estimated
  - These predictions were compared to the actual test results

- Choice to have **multiple tests** focusing on **specific parts** of the design rather than a complex test activating all the functions at once
  - Data needs to be analyzable and exploitable

- 7 tests have been developed
SCOC3 Radiation Test

- SCOC3 radiation test took place at RADEF (Jyvaskyla, Finland) on 5-7 Sept. 2012
- Heavy Ions Testing
SpW Test Results

- The SpW test involved: 2 SpW + CPU + utilities.
- Results: 150x less sensitive than predicted.
The test of the caches involved: Inst. & Data caches + CPU + utilities.

Results: 15x less sensitive than predicted.
Radiation Test Results

Main results:

- **SEL:** SCOC3 is insensitive to SEL and to Electrical Failure (tested up to 65 Mev.cm²/mg)

- **SEU:** The observed SEU rates are less than the predicted SEU rates: from 5.6x less to much more.
  - One reason for this is logic masking: in modules involving DFFs and logic, some errors occurring in the logic will not generate a functional error
  - On the memory tests, the results are closer to the estimations

- **SET:** One test was run at both 32MHz and 80MHz to quantify the proportion of SEUs due to SETs sampled by DFFs.
  - No significant cross-section variation observed between the 2 frequencies, on the 5 comparison points.
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5. SCOC3 Development Kit
SW Development Environment

- The **SCOC3 LEON3 core** is readily usable by developers already working with **ERC32 or LEON2** based computers.

- The software development environment includes the compiler + debug tools and is available with an **Eclipse interface** (as well as in command line).

- SCOC3 is compatible with many OS (**RTEMS, VxWorks**, ...)

![SW Development Environment](image_url)
SCOC3 SW modules

Provided with SCOC3

BIOS and Drivers for I/O’s: SpW, 1553, CAN, TM/TC, UART...

Board Support Package for the RTEMS Operating System

Boot

Demonstration SW: test applications serving as SW examples

The first version (demonstration level) is already available

A Flight-Quality version is planned for beginning of 2013
The SCOC3 Starter Kit is a FPGA-based development platform & evaluation board

- Suitable for early SW development and rapid prototyping of applications using SCOC3

It is 100% representative of SCOC3 and its interfaces:

- SCOC3 VHDL design in a Xilinx on board memory
- all of SCOC3 interfaces (2x1553, 2xCAN, 4xUART, 7xSpW, TM/TC...)

It is scalable and can be adapted or extended through expansion boards
SCOC3 Simulator

SW development and qualification

- SCOC3 Simulator is **fully representative** of SCOC3 in current applications
  - It has been validated and calibrated with real HW to make it **suitable for flight software** development and qualification
- Used for **SW development, validation, qualification** and operations at spacecraft level
  - Ability to fully control execution time
  - Integrated with non intrusive debug functions
  - Failure injection capabilities to exercise SW error cases
- SCOC3 Simulator executes **as fast as real time**
  - Using JIT technology
- Test SW in Java
  - Eclipse plug-in
6. SCOC3
Commercialization
Development status & Availability

- SCOC3 ASIC is validated since 2009
- Flight models are available since 2010
- SCOC3 is commercially released since 2010

- **SCOC3 is already selected for** 8 satellites including SPOT6, SPOT7, KRS, SEOSAT, Sentinel ...

**FLIGHT PROVEN**

Since 9/09/2012 on SPOT6
ASSP & Commercialisation Plan

- SCOC3 is an **ASSP** (*Application Specific Standard Product*) available to the European space industry under fair and equal conditions
- Astrium is the single contact point to customers for providing components, support and additional services
- This is formalized with ESA through a *Commercialisation Plan*

![Diagram showing the flow of components and support for SCOC3](image)
Quality levels

- **3 Quality levels** are available
  - EM / Prototype
  - QML-Q
  - QML-V

- ATMEL MOQ (Minimum Order Quantity) apply, but discussions have started with ESA to waive this constraint by having a batch of components on stock (i.e. no MOQ for the final customer)
  - The idea is to put components on stock
  - Still under discussion (requires a budget)
The complete offer – summary

- SCOC3 ASIC (EM, QML-Q or QML-V)
- STARKIT (FPGA development kit)
- Simulator (qualified for flight SW development)
- Basic SW (demonstration version available, Flight-quality version for beg. of 2013)
- Application SW
- Technical support
Conclusion
Conclusion

- SCOC3 is a **powerful processor** and spacecraft controller
- SCOC3 is fully validated and already selected for 8 satellites
- SCOC3 is **flight-proven** since 9th September 2012
- SCOC3 is commercially available with a **complete ecosystem** for integration, use and SW development
Contacts

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