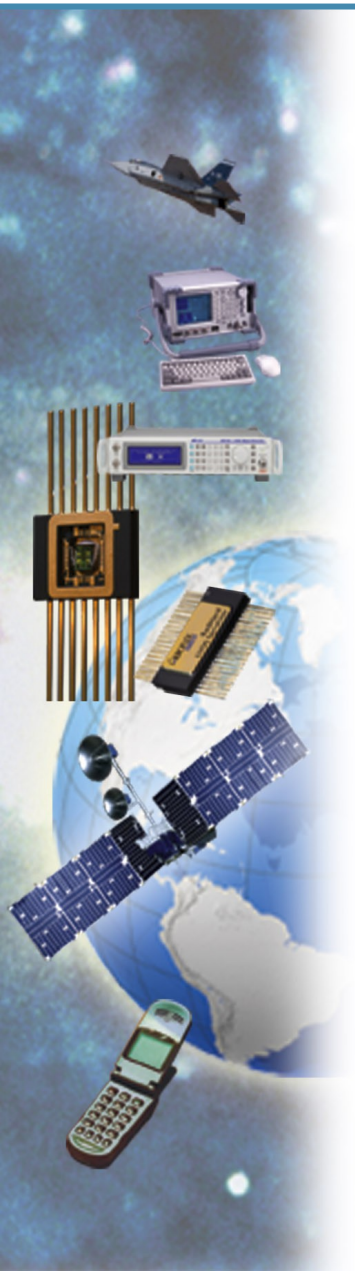


# Manufacture and Validation of the NGMP LEON4FT Multiprocessor Prototype Device

Final Presentation Days 2012

ESA/ESTEC December 5th, 2012

**www.aeroflex.com/gaisler**

# Introduction

- As background, Aeroflex Gaisler is developing system-on-chip design, named the Next Generation Microprocessor (NGMP), as part of a separate ESA contract, to be presented at a later time.
- NGMP is an ESA activity developing a multi-processor system with higher performance than earlier generations of European Space processors
- The NGMP is part of the ESA roadmap for standard microprocessor components
- Aeroflex Gaisler's assignment, together with various technology and service suppliers, consists of specification, the architectural (VHDL) design, verification, manufacturing, FM qualification and finally commercialisation of the NGMP.
- Aeroflex Gaisler has also been involved in support and validation of various ESA microprocessor developments under a frame contract. As a last call-off order of this contract, and the topic of this presentation, functional prototypes of the ESA Next Generation Microprocessor have been developed.

# Introduction

- Funding:
  - ESA within contract 18533/04/NL/JD
- Parties:
  - Aeroflex Gaisler AB (Sweden): Requirements, verification, synthesis, validation
  - eASIC Corporation (US, Romania): Layout, prototype implementation
  - Pender Electronic Design (Switzerland): Validation board development

# Outline of remaining slides

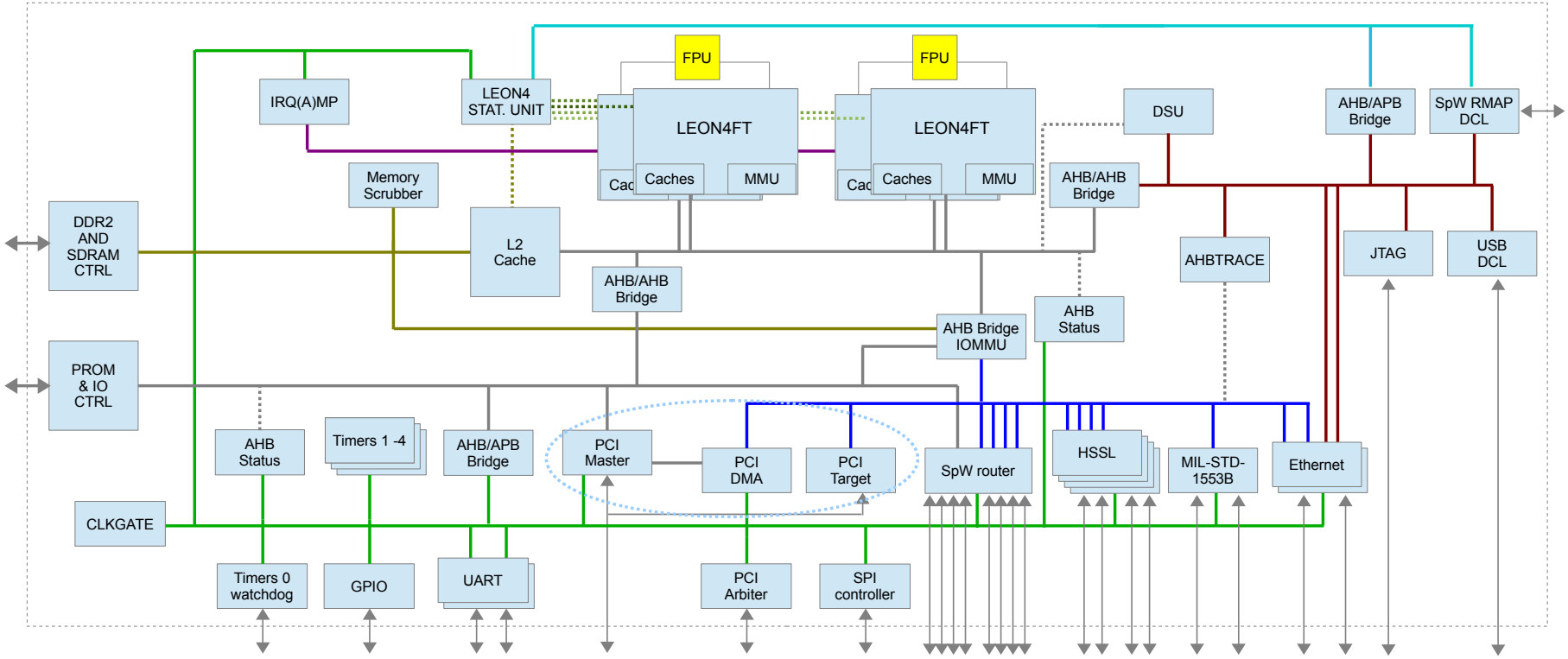
- Objectives
- Design description
- Target technology selection
- Work package descriptions
- Schedule
- Description of work performed
- Issues / Challenges
- Differences between NGMP baseline and NGFP
- Implementation results
- Benchmark results
- Validation board
- Lessons learned
- Remaining tasks
- Summary and outlook
- Conclusions

# Objectives

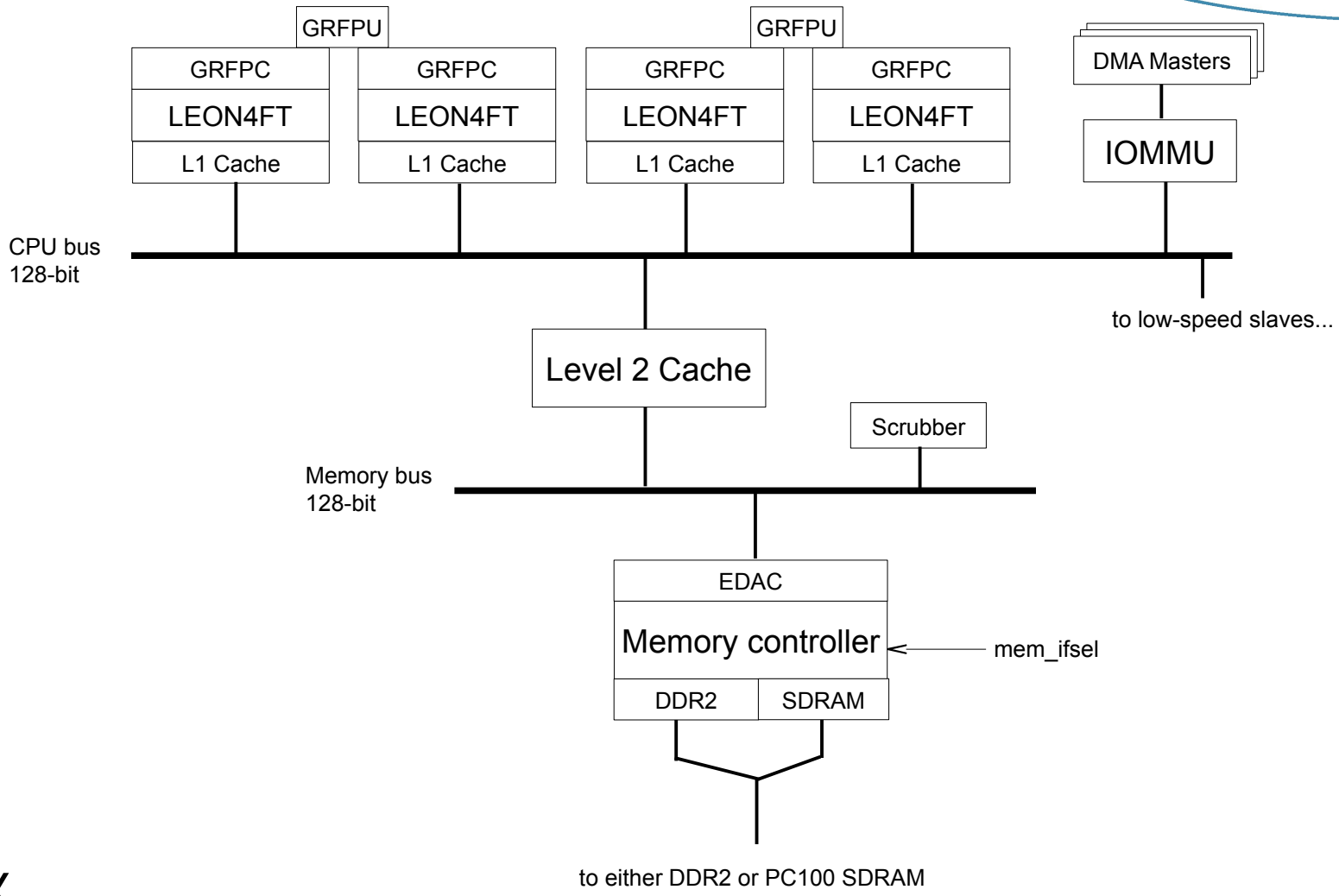
- Consolidate the previous prototyping on hardware at the target speed and allow real performance evaluation
- Make an early identification and investigation of potential problems related to the design and to implementation of the architecture on a deep sub-micron technology in order to prepare the development of the future processor device.
- Provide to the European space community the access to an evaluation board to allow users to asses the suitability of the offered at speed performances and the offered functions for their future applications and give feedback to consolidate the future ESA processor specification.

# Description of design: NGMP

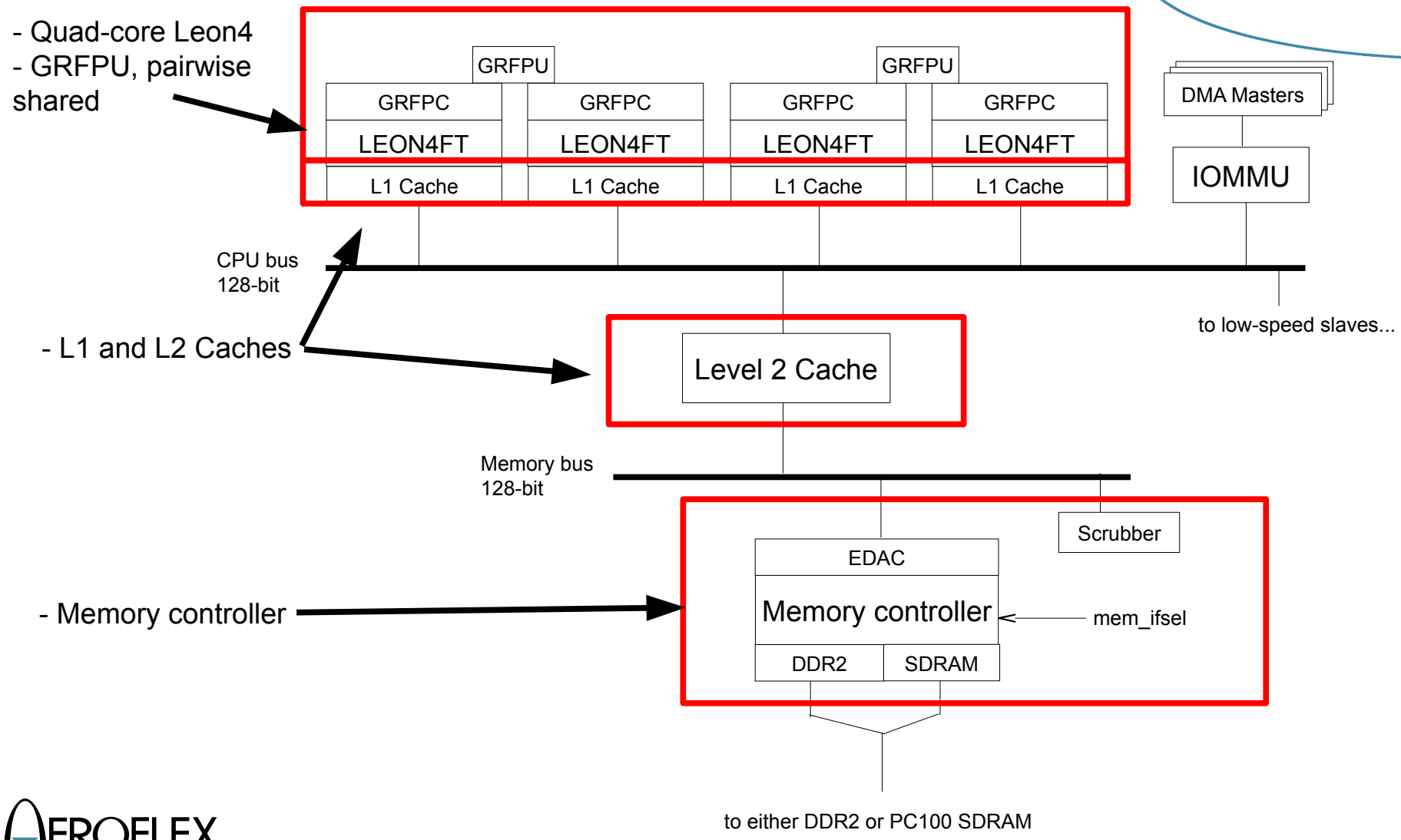
- Quad core LEON4FT connected to shared L2 cache



# NGMP Architecture Overview (1/2)



# NGMP Architecture Overview (2/2)



# NGMP Overview - Features

- 4x LEON4FT with 128-bit AHB bus interface
  - High-performance GRFPU, one FPU shared between two CPUs
  - 16 KiB I-cache, 16 KiB D-cache, write-through
- Level-2 cache, bridge in the bus topology
  - Configurable, copy-back operation, can be used as OC RAM
- External memory: DDR2 or SDRAM, 64 data-bit + 32 check-bit wide
  - Powerful interleaved 16/32+8-bit ECC giving 32 or 16 checkbits (SW selected, can be switched on the fly)
- Memory error handling (memory controller, scrubber, CPU together)
  - Hardware memory scrubber for initialization, background scrub, error reporting and statistics
  - Rapid regeneration of contents after SEFI
  - Graceful degradation of failed byte lane, regaining SEU tolerance
  - Example code for RTEMS available

# NGMP Overview – I/O Interfaces

- Large number of I/O interfaces:
  - 8-port SpaceWire router
  - 32-bit 33/66 MHz PCI Master/Target with DMA
  - 2x 10/100/1000 Mbit Ethernet
  - 4x High-Speed Serial Link (if available)
  - MIL-STD-1553B
  - 2xUART, SPI master/slave, 16 GPIO
- Debug interfaces:
  - Ethernet
  - USB
  - Spacewire (RMAP)
  - JTAG

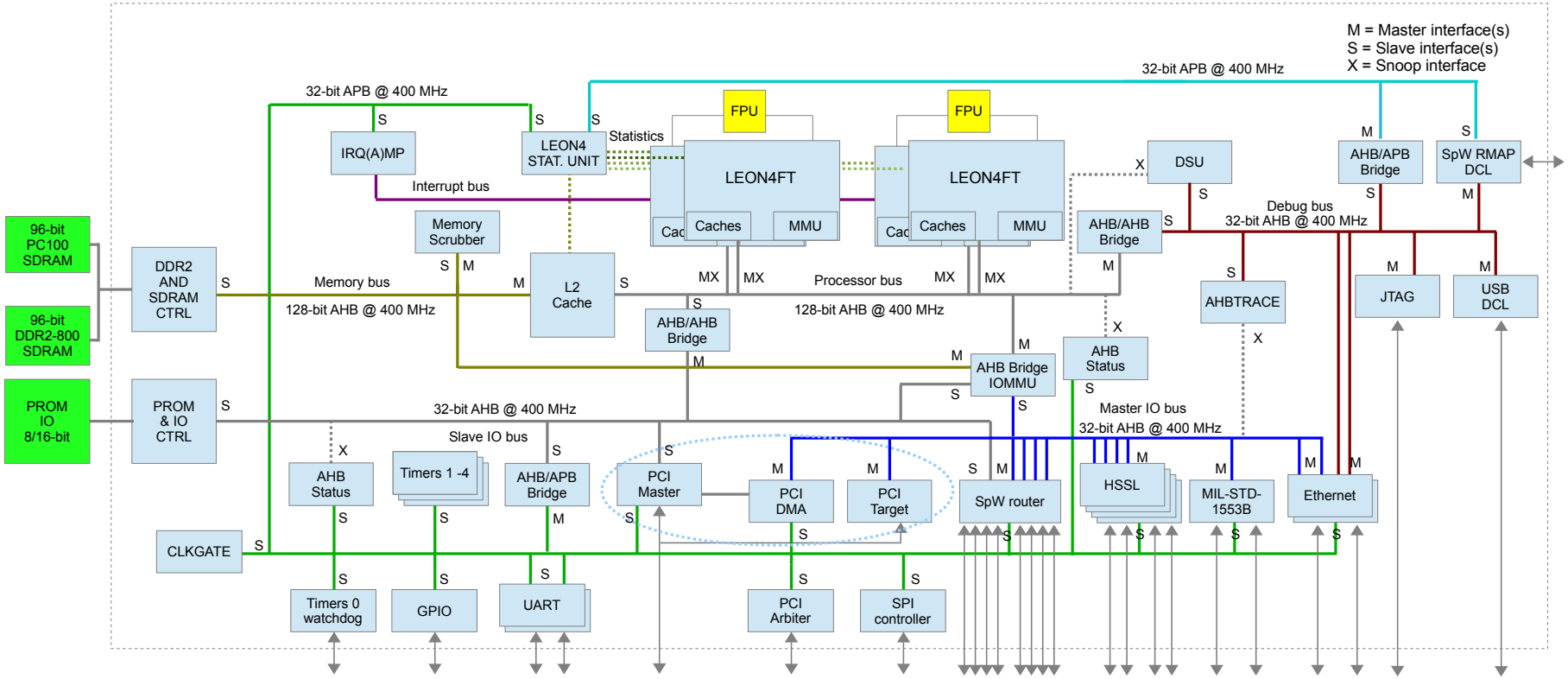
# NGMP Overview – Improvements

- Resource partitioning
  - The architecture has been designed to support both SMP, AMP and mixtures (examples: 3 CPU:s running Linux SMP and one running RTEMS, 4 separate RTEMS instances, 2x Linux/1x RTEMS/1x VxWorks, etc.)
  - The L2 cache can be set to 1 way/CPU mode
  - Each CPU can get one dedicated interrupt controller and timer unit, or share with other CPU
  - Peripheral register interfaces are located at separate 4K pages to allow restricting (via MMU) user-level software from accessing the wrong IP in case of software malfunction.
  - IOMMU
- Improved debugging
  - Dedicated debug bus allows for non-intrusive debugging
  - Performance counters, AHB and instruction trace buffers with filtering, interrupt time stamping

# NGMP - PROM-less / SpW applications

- Extended support for PROM-less boot
- PROM-less booting possible via SpaceWire
  - Connect via RMAP
  - Configure main memory controller
  - Use HW memory scrubber to initialize memory
  - Enable L2 cache (optional)
  - Upload software
  - Assign processor start address(es)
  - Start processor(s)
- SpaceWire router, with eight external ports, is fully functional without processor intervention
- Device can also act as a software/processor-free bridge between SpW and PCI/SPI/1553 etc.
  - IOMMU can be used to restrict RMAP access

# NGMP Overview – Block Diagram



# Target technology selection

- Trade-off was made between
  - MPW on commercial ASIC (e.g. TSMC/UMC 90)
  - eASIC Nextreme2
  - High-end FPGA
- The selected target technology was eASIC Nextreme2
  - Quicker turn-around than MPW
  - More (tested and functional!) devices compared to MPW
  - Less cost compared to high-end FPGA
  - Preliminary analysis (pre-layout synthesis) showed that roughly 300 MHz could be obtained on AMBA system

# Work package descriptions

- W.P. No: 100 – Definition phase T0 → T0+2
- W.P. No: 200 – Architectural design T0+2 → T0+4
- W.P. No: 300 – Detailed design T0+4 → T0+6
- W.P. No: 410 – Layout generation T0+6 → T0+8
- W.P. No: 420 – Layout verification T0+6 → T0+8
- W.P. No: 500 – Prototype implementation T0+8 → T0+10
- W.P. No: 610 – Validation board development T0+6 → T0+10
- W.P. No: 620 – Design validation T0+10 → T0+12

# Schedule

- Contract signed in May 2011
- Schedule, planned vs. actual:

| Milestone | Planned date | Actual date | Slip |
|---|---|---|---|
| KOM | T0 | T0 | 0 |
| SRR | T0+2m | T0+2m | 0 |
| PDR/DDR | T0+6m | T0+9m | +3m |
| CDR | T0+8m | T0+11m / T0+13m | +5m |
| QR/AR/FR | T0+12m | T0+20m (?) | +8m |

- Delay incurred at before PDR/DDR partly due to missing eASIC tools. Tape-out initially planned for December 2011. Got access to updated tool-flow during November 2011 → Tape-out postponed to mid 1Q2012.
- Tape-out subsequently postponed to March, April (timing problems, DDR2 PHY issues), and then May (to allow time for back-annotated sim). Tape-out occurred May 18 2012.

# Difficulties faced during the work (0)

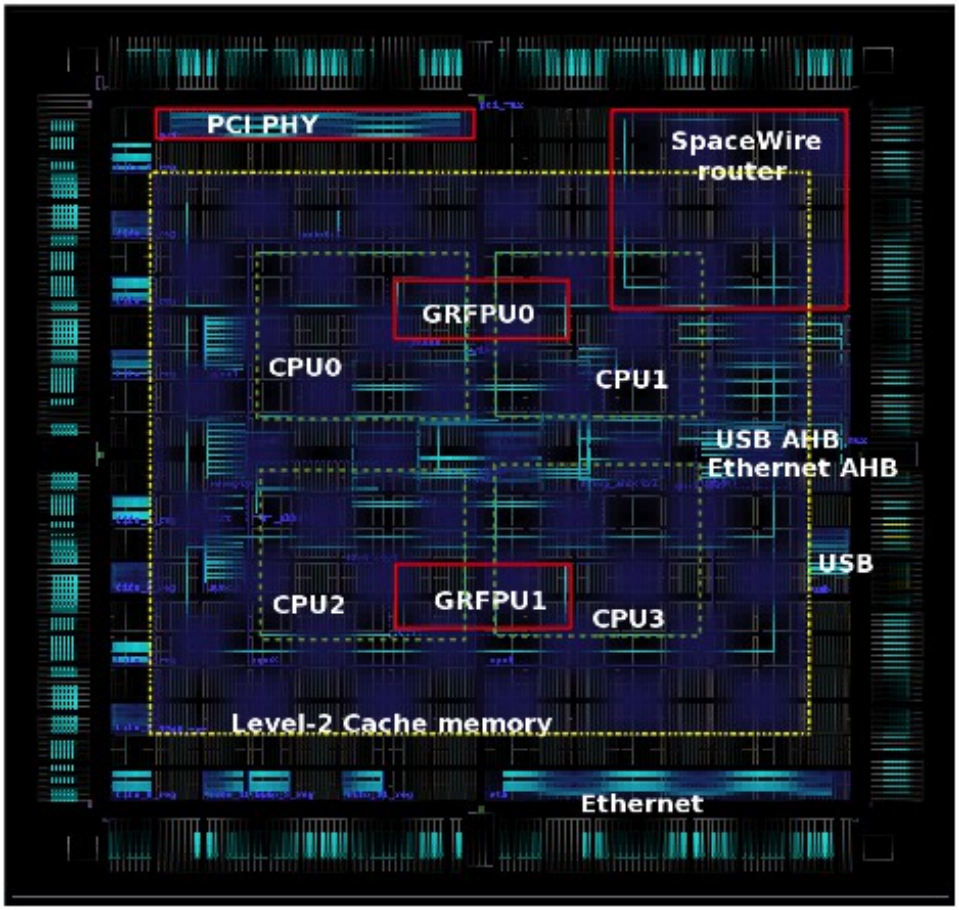
- Trade-off on features to implement
  - Upgraded to larger device to accommodate all I/Os (N2X550 in FC896 package). Plenty of logic resources to fit design.
  - No SerDes available on target device → HSSL not implemented
- Map of technology specific parts to Nextreme2 technology was overall straightforward.
  - Aim was to re-use as much as possible of eASIC's pad and memory generators
  - Difficulties with the integration of eASIC's DDR2 PHY. Delays due to wait on new tool versions. Bugs found at late stages both in DDR2 controller and in DDR2 PHY
- Difficulties to meet timing. No support for physical synthesis. No proper wire-load model available.
- Iterations with eASIC to improve AMBA system timing while eASIC focused on memory interface layout.

# Difficulties faced during the work (1)

- Problems with I/O timing on PCI, Ethernet and SDRAM required much effort
- Netlist verification successful after much work spent on reducing 'X'-propagation
- Tape-out delayed on several occasions due to layout verification issues
  - Very pessimistic simulation models of PLLs
  - Several upgrades required for simulation models used for back-annotated simulations.
  - Very long simulation time
- Device tape out on: May 18 2012
- Validation board with devices received in September 2012
- Most of validation board work has been spent on memory interfaces. Issues faced with DDR2, all other interfaces appear functional.

# Example of layout issue

- Fixed RAM positions vs. Level-2 cache



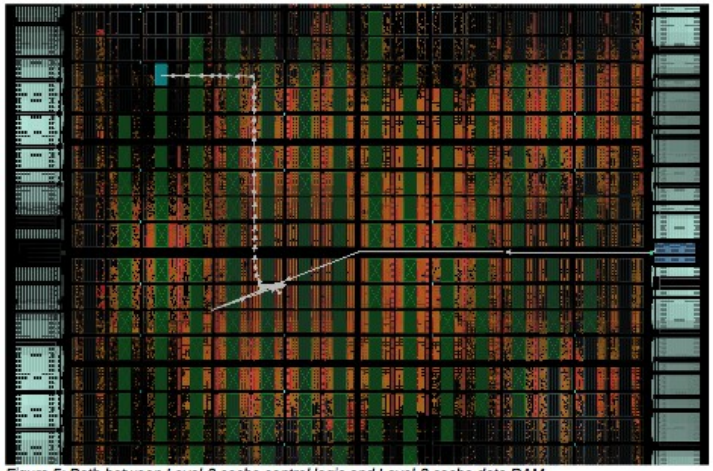



Figure 5: Path between Level-2 cache control logic and Level-2 cache data RAM

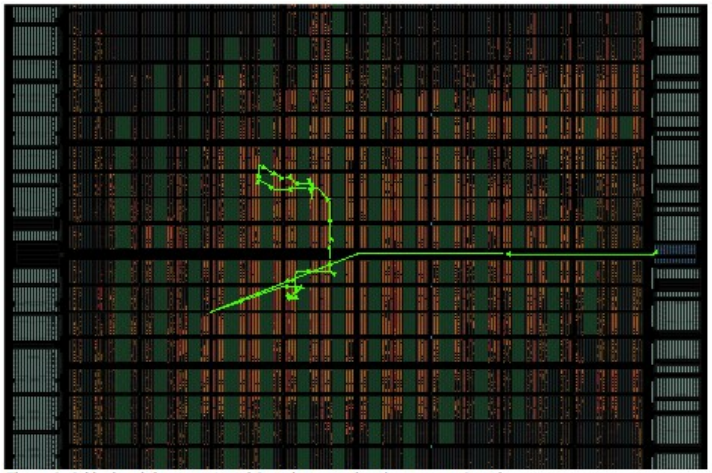


Figure 6: Critical path between Level-2 cache control and processor 0 cache

# NGFP and baseline NGMP differences

- Lower operating frequency (150 MHz, also affects selectable modes)
- No high-speed serial links
- DDR2 and SDRAM memory interfaces on separate pins
- No fault-tolerance for LEON4, Level-2 cache, Ethernet core buffers, SpaceWire router
- Dynamic PLL and pad control
- Soft-configurable L1 cache replacement policy is not implemented.

# Implementation results

- Memory interfaces: DDR2 SDRAM: 300 MHz, SDRAM: 100 MHz
- AMBA:
  - 150 MHz in all corners
  - 200 MHz not met in slow-slow corner – but appears stable in lab
- Area (N2X550 device):

| Resource | Used | Available | Utilization |
|---|---|---|---|
| I/O Pads | 600 | 615 | 97.56% |
| eDFFs | 89396 | 368640 | 24.25% |
| eCells (estimated) | 237169 | 552960 | 42.89% |
| Total number of LUTs | 313796 | | |
| Logical | 308520 | | |
| 2-input LUT | 72280 | | |
| 3-input LUT | 234227 | | |
| 4-input LUT | 2013 | | |
| Arithmetic eCells | 5276 | | |
| Buffers | 42448 | | |
| bRAMs | 196 | 240 | 81.67% |
| bRAMs (18K) | 107 | | |
| bRAMs (36K) | 142 | | |
| ViaROMs | 0 | 4 | 0.00% |
| RegFiles | 293 | 480 | 61.04% |
| Global clocks | 9 | 32 | 28.12% |
| PLLs | 8 | 16 | 50.00% |
| DLLs | 12 | 52 | 23.08% |

# Benchmark results

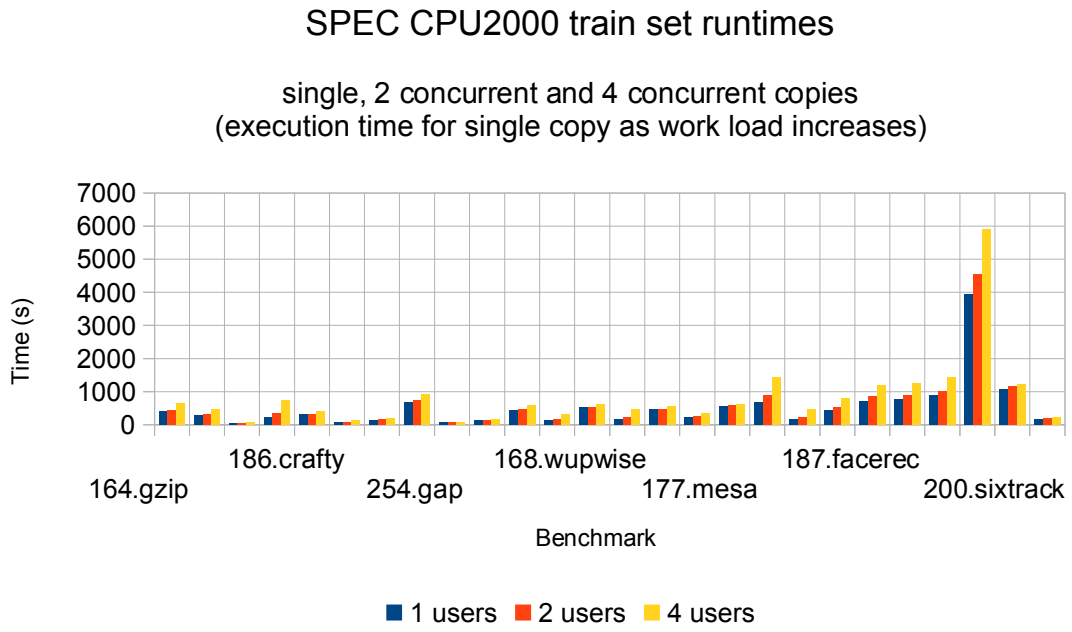
- CoreMark 1.0:

| AMBA Frequency | SDRAM | | DDR2 SDRAM | |
|---|---|---|---|---|
| | L2C disabled | L2C enabled | L2C disabled | L2C enabled |
| 150 MHz | 185 CoreMarks | 308 CoreMarks | 215 CoreMarks | 308 CoreMarks |
| 200 MHz | 247 CoreMarks | 410 CoreMarks | 244 CoreMarks | 410 CoreMarks |

- SDRAM frequency is half of AMBA frequency
- DDR2 SDRAM I/F is DDR2-600
- Benchmark compiled with GCC 4.4.2

- **Device can deliver: 410 CoreMarks (2.05 CoreMark/MHz)**

# Multi-Core Benchmark results



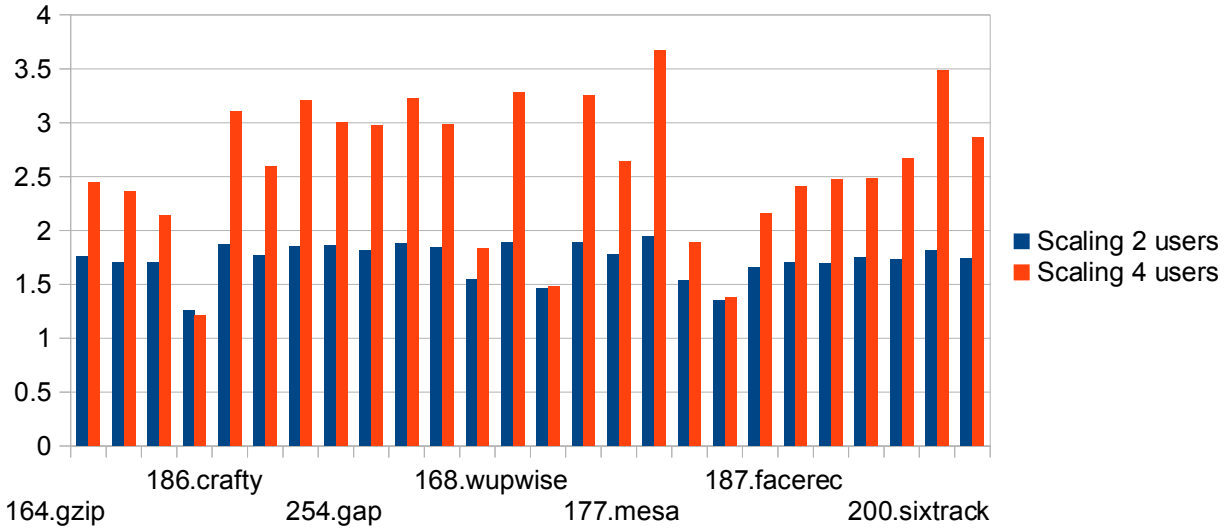

**(Pessimistic) Average of scaling measurements:**

Activating one additional core gives speed-up of 1.6 (range 1.3 – 1.94)

Activating three additional cores gives speed-up of 2.4 (range 1.2 - 3).

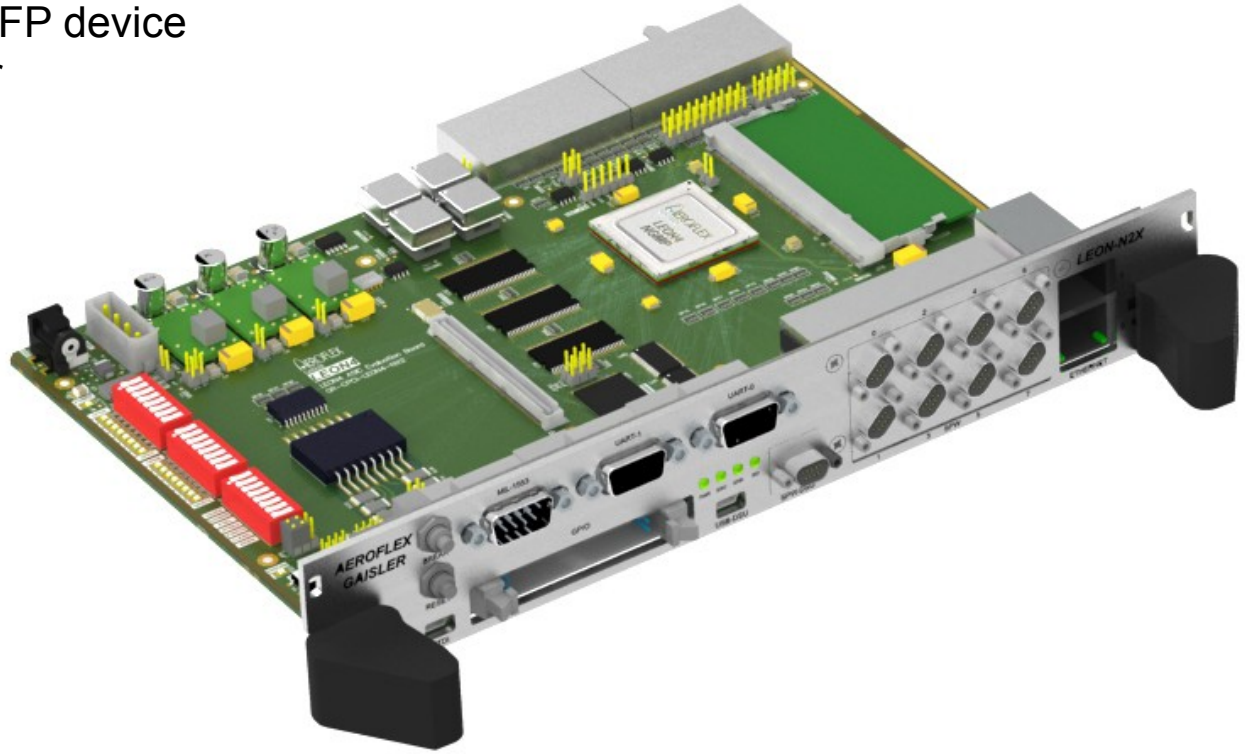
.. in tests where workload is multiplied with number of cores!

Test is pessimistic as all (sequences) of accesses to shared resources will occur simultaneously.



# NGFP Evaluation Board

Evaluation board providing
interfaces of the NGFP device
6U CPCI form factor



# Lessons learned

- Fixed sea of small RAMs and large Level-2 cache is a bad mix
  - FPGA tools appear to handle this surprisingly well
  - eASIC is an FPGA-like architecture, but with limited tool capabilities
- Beware of the pre-/post-layout derating factor, it was 2 in this technology
- 96-bit wide external DDR2 memory interfaces can bring timing trouble
- Integrating a DDR2 PHY can be a challenge
- Do not assume that tools are able to move registers close to pads
- Trace buffers on all buses can save time
- Two months allocated for board validation was too little time for a design and board of this complexity

# Remaining tasks

- Validation board investigations
- IO performance evaluation
- Demonstration of multi-core debugging support
- Additional benchmarking

# Summary and outlook

Initial goals of the activity are mostly fulfilled:

- Consolidate the previous prototyping on hardware at the target speed and allow real performance evaluation
  - Full speed target not met, still large improvement compared to existing FPGA prototypes.
- Make an early identification and investigation of potential problems related to the design and to implementation of the architecture on a deep sub-micron technology in order to prepare the development of the future processor device
  - Valuable lessons learned, although many specific to the target technology.
- Provide to the European space community the access to an evaluation board to allow users to asses the suitability of the offered at speed performances and the offered functions for their future applications and give feedback to consolidate the future ESA processor specification.
  - Validation board is up and running. Some debugging remains.
  - The validation board is commercially available

# Conclusions

- Lessons learned considered valuable for future implementations of the architecture.
- Functional prototype device and validation board successfully implemented and we can now provide a representative prototype of the NGMP to the European space community.
- The board is on display at the bottom of this room,
  and it is commercially available from Aeroflex Gaisler

Thank you for listening!

Questions?

Specifications and NGMP status available from:

http://microelectronics.esa.int/ngmp/