FT-Unshades2: High Speed, High Capacity Fault Tolerance Emulation System

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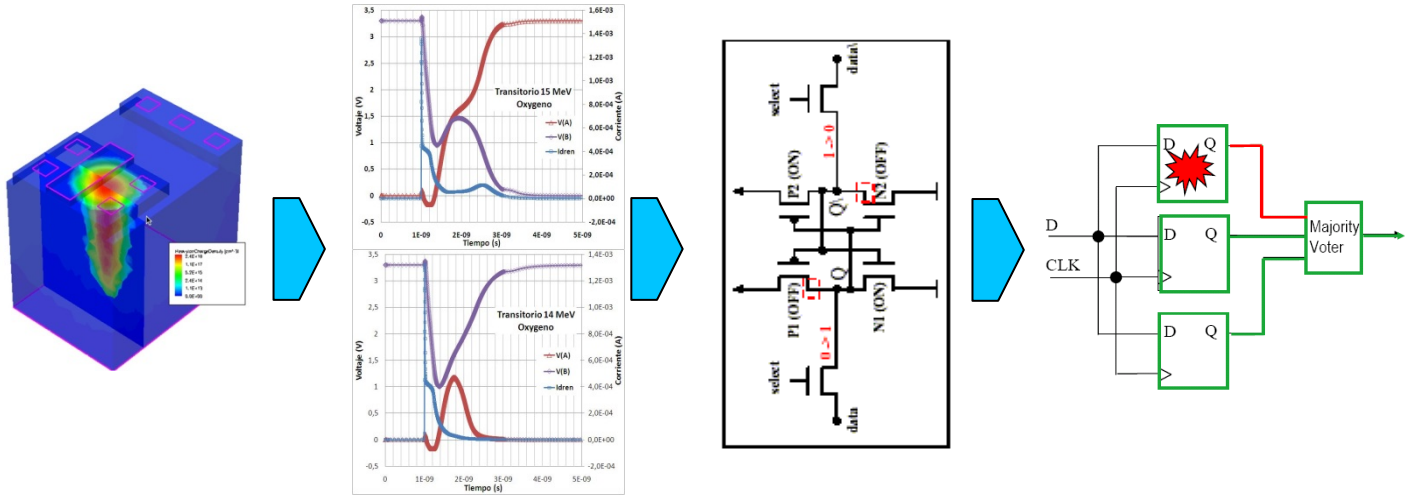
FTU2 Purpose



- Determine the best protection level of your design
- Check if the protections has not been collapsed by synthesis
- Check if the workload is enough for your radiation tests
- Functional design tests are recommended
- Initialization policy of your design.

Outline

- FT-UNSHADES concept
- The Hardware & Software subsystems
- Highlights of the project
- Examples

What is FT-Unshades2?

- **FT-Unshades2 is a tool for FAST PREDICTION of radiation effects in digital designs**

- At the HDL description stage of the design flow
- Easy and non-intrusive set-up
- Uses a proprietary FPGA emulation technology
- Change te current value of any USER REGISTER (bit-flip)
- Fast and Flexible environment
- Over a custom-made hardware system

What can FT-Unshades2 do?

- Massive SEE emulation in the netlist to obtain an estimation of MTBF
- Detailed analysis of fault propagation through the netlist
- Several SEE models (SEU, SET, MBU, …)
- Internal protection checking (TMR, EDAC, …)
- Hierarchical analysis of circuit sensitivity for selective protections
- Initialization policy checking

DESIGN

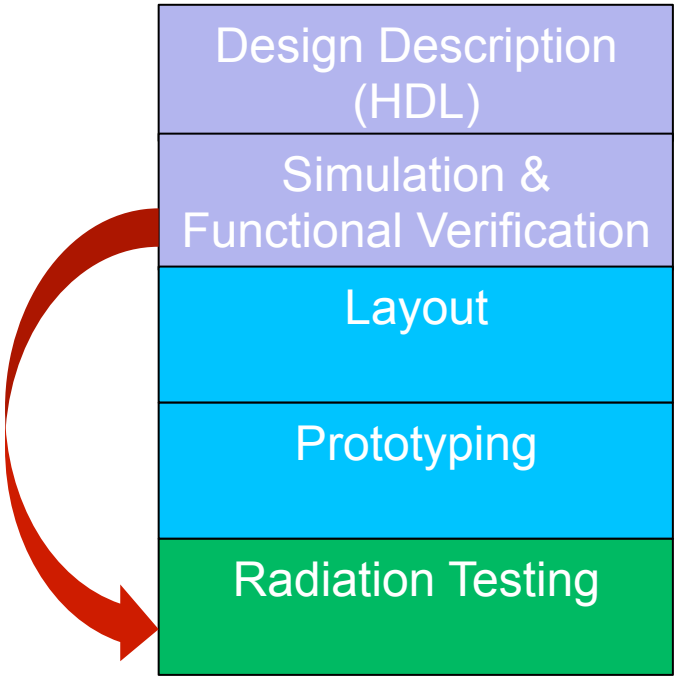
- Test vector quality assessment
- Fault diagnosis

BEAM

What can FT-Unshades2 do?

For You

- Typical Digital Design Flow:



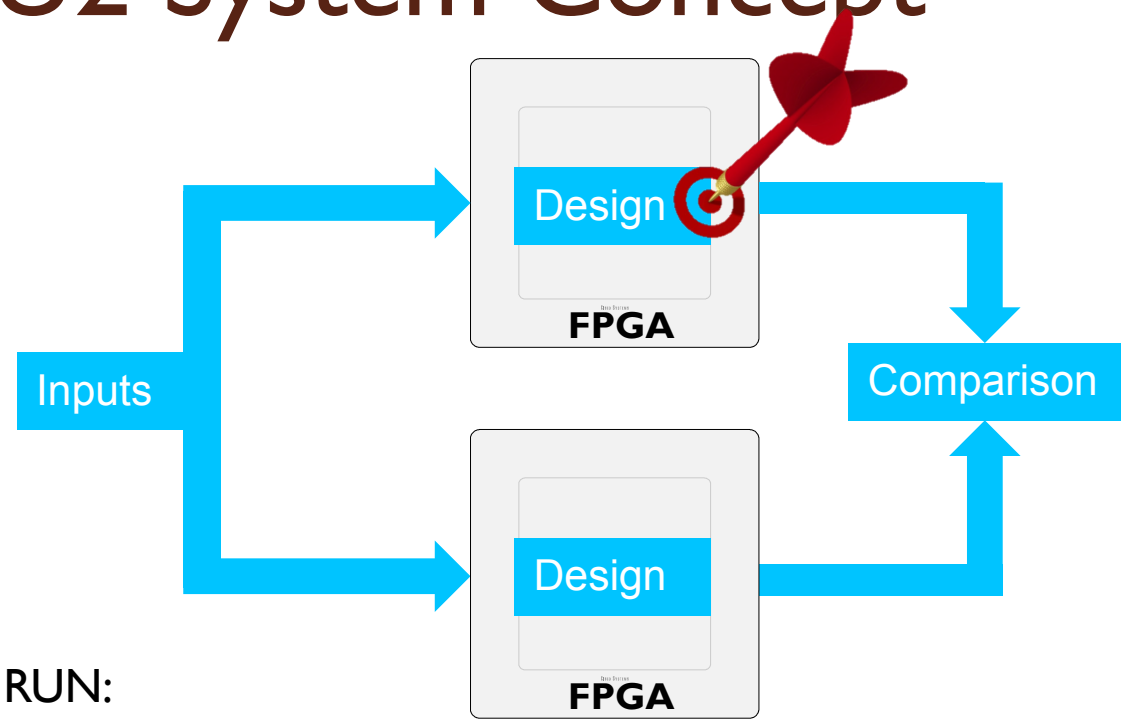
FTU2 Procedure

- Simple procedure:

1. Write a small I/O declaration file (design.pin)
2. Implement for Xilinx FPGA (design.bit and .ll)
3. Simulate your testbench and dump a vcd file (design.vcd)
4. Use the *User Friendly Interface* to perform the Fault Tolerance Analysis

- That's all!

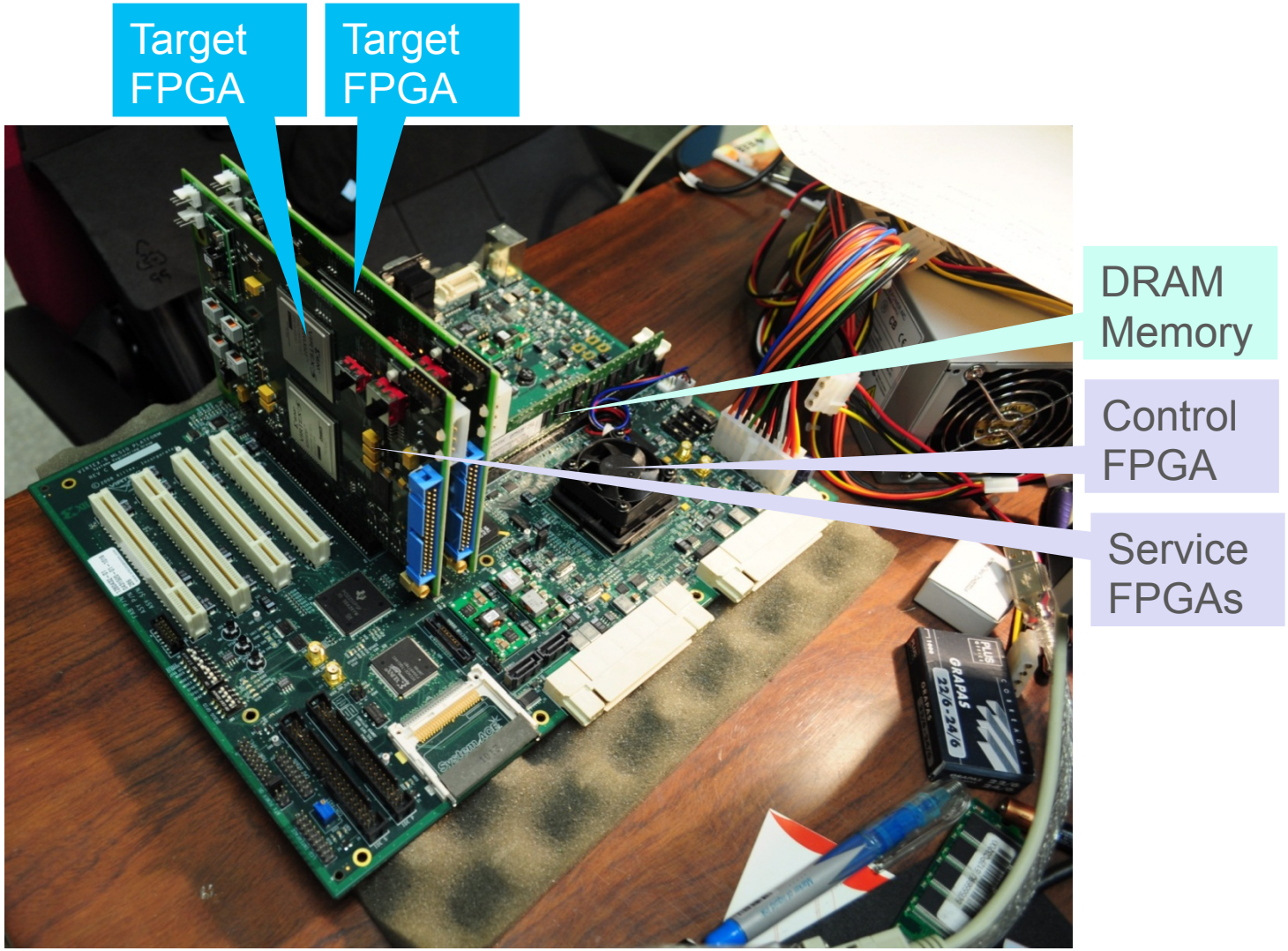
FTU2 System Concept



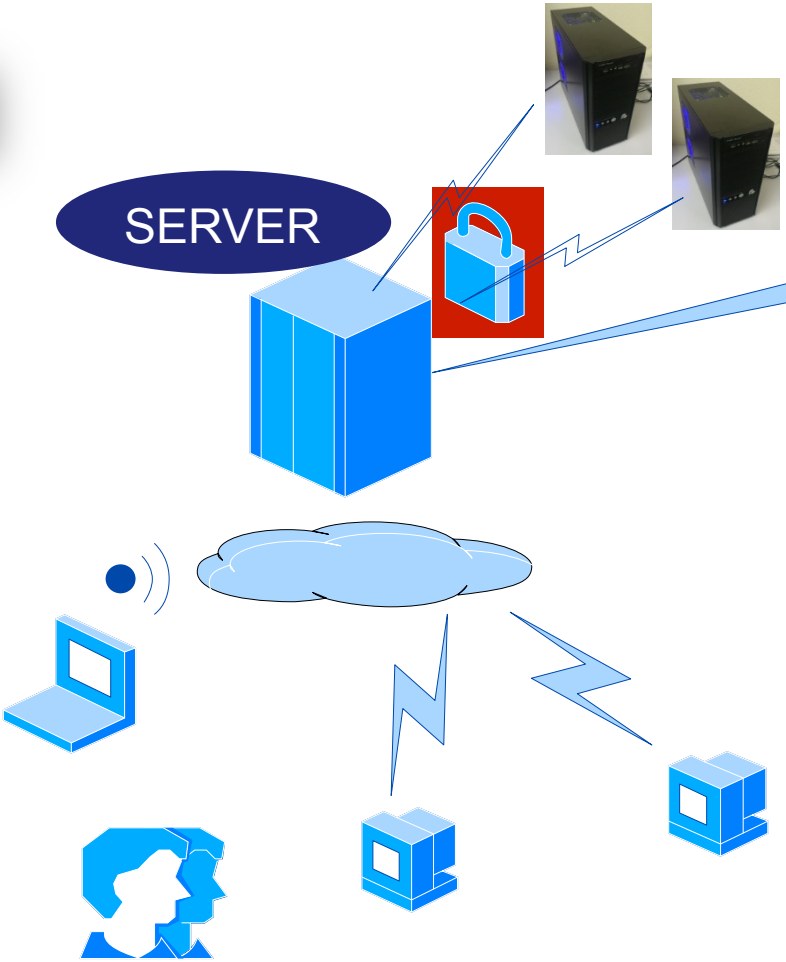
A single RUN:

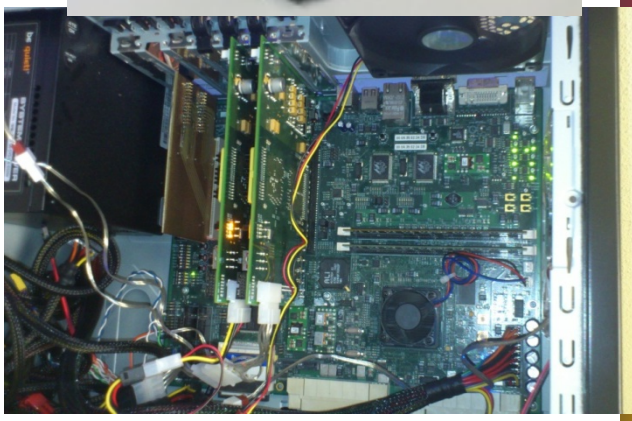
- Select a target register
- Define the injection cycle

FT-UNSHADES2 in a nutshell: hardware structure



FTU2 Remote Access





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FTU2 User Interface

- FT-UNSHADES concept
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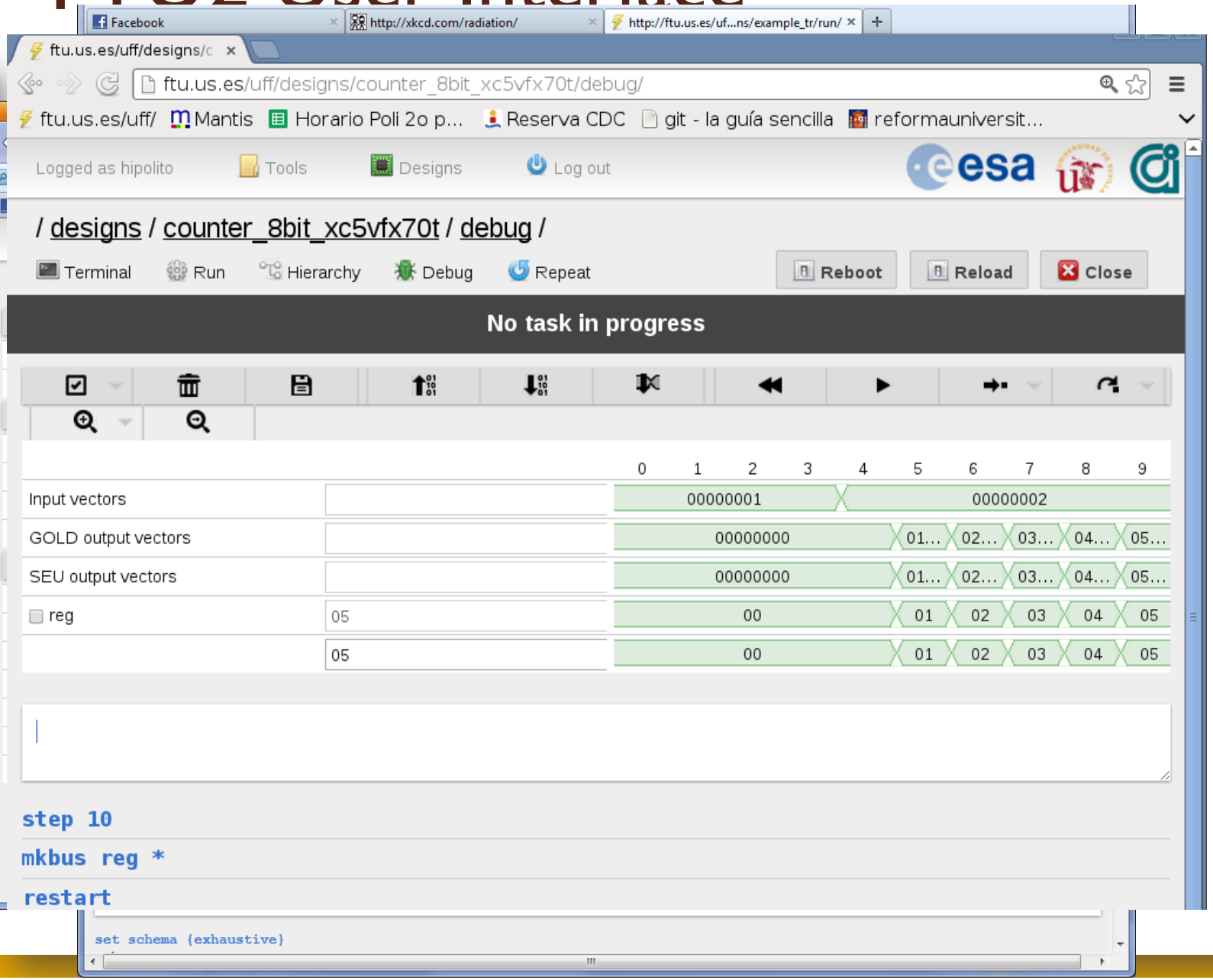


FTU2 highlights

- FT-UNSHADES is a tool for SEE EMULATION, at netlist level.
- Emulation is the use of programmable hardware structures to perturb the design under test.
- It is a highly flexible and simple solution for the designer.
- Represents ANY fault model represented by bit-flips
- The goal is to perform the injections in a deterministic manner.
- Combines Massive Injections with cycle accurate analysis, in the same tool
- Exploits the mechanisms of Xilinx FPGA, named Partial Reconfiguration, Snapshot and Readback

Other features:

- Remote access
- Internal analysis
- Test in the beam
- Targeting FPGAs for analysis

FTU2 in numbers

1. Fault rate achieved: 10.000 faults/sec (this figure will be improved in new versions)
2. 512 I/Os, the capacity depends on the model of the target device.
3. Current configurations Virtex 5, LX50T and FX70T (FF1136 package)

Access to FTU2

- For public institutions and research purposes:
  - We offer the on-line access to our University
  - For in-situ systems contact with “Foundation of the University of Sevilla (FIUS)”
- For private companies:
  - Contact with our private transference office “AICIA”.

More FTU2…

- FPGA mode
  - Injections over the configuration memory
  - Using a configuration bit map
  - Checking propagation of faults to user logic
  - Scrubbing technique testing
- Radiation testbed adaptation
  - Run-time analysis of a device exposed to the beam
  - Failure diagnosis based on fault dictionary
  - Workload quality assessment
- SET diagnostic
  - Connect with SETA tool (Politecnico di Torino)
  - Integration with CADENCE injection tool FTU-Analog

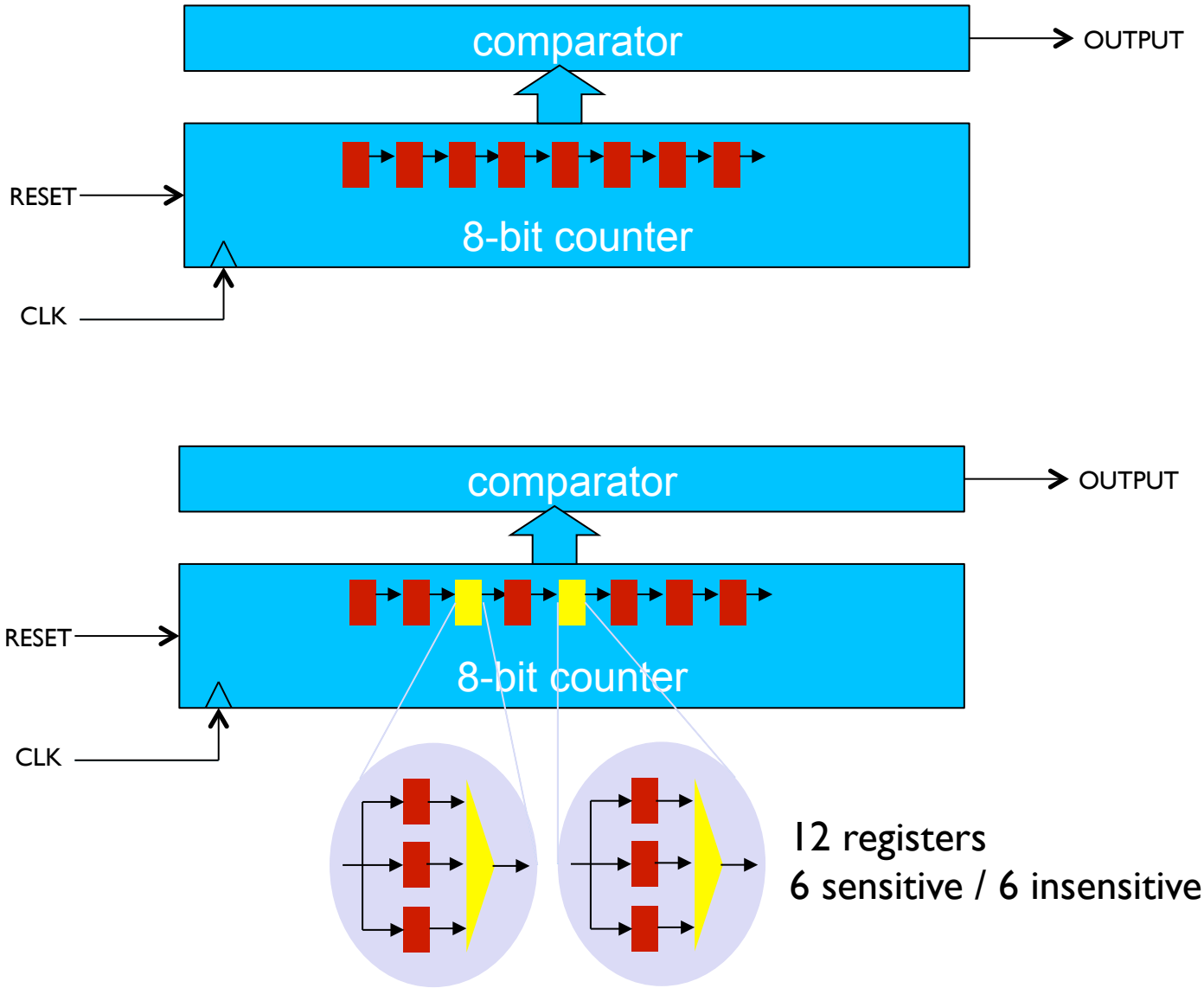
Live demo!

- Connection to the system @ Universidad de Sevilla (us.es)

- Three designs will be presented:

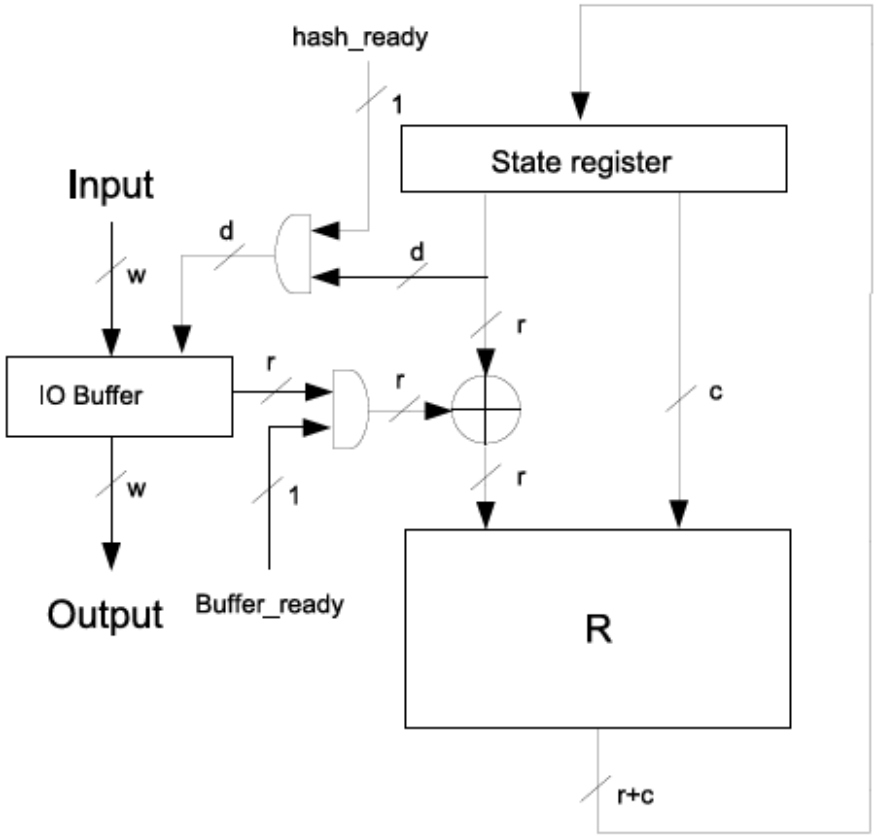
1. Simple counter with two tripled stages
2. KECCAK Cryptcodec
3. R-vex microprocessor

Simple counter



Keccak Cryptcode

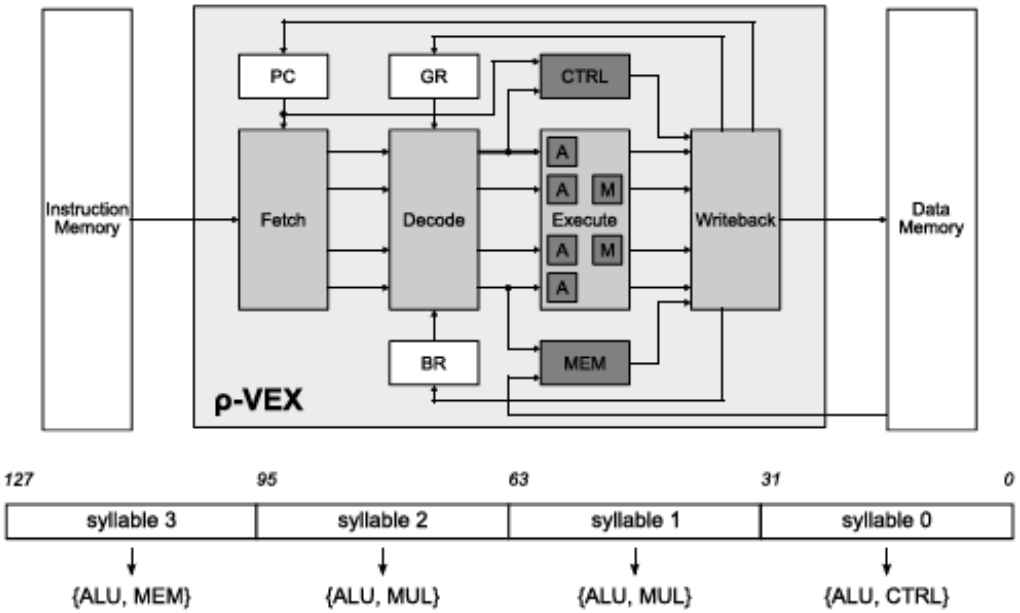
http://keccak.noekeon.org/



Completely third party design, without hierarchy structure

ρ-VEX processor

ORGANIZATION



- This example is taken from internet.
- We didn't make any modification. It is not protected.
- The example is a *LZW data compressor*. .
- There is a problem with the initialization.
- The data memory block is not initialized.

FTU2 in FPGA mode

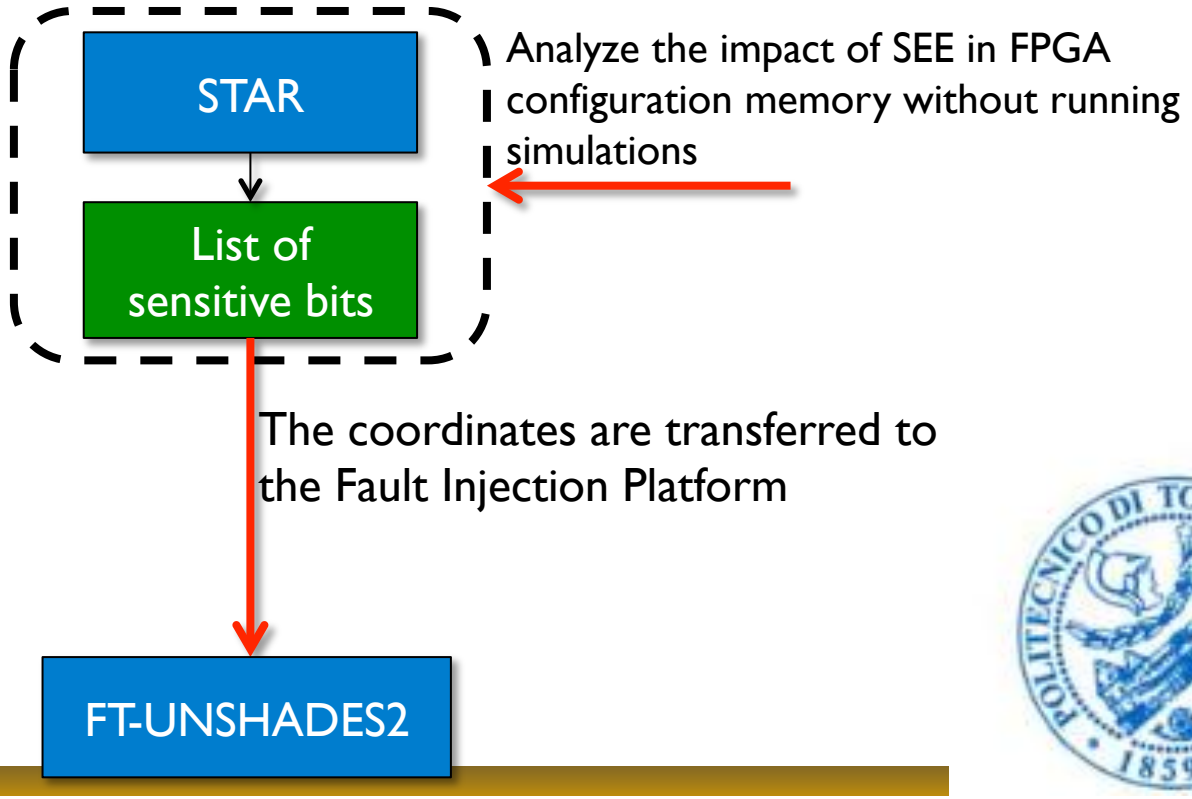
Originally FTU was thought trough the assessment of ASIC netlist. FTU2 has been extended to inject on SRAM-FPGAs configuration.

- The basic mechanism to inject over the FPGA CONFIGURATION is the same than USER REGISTERS.
- It is not constrained to a specific FPGA
- Analyzes in detail the propagation of a fault in the configuration, and the possible corruption of the user logic.
- The study of techniques for scrubbing policy

FT-UNSHADES2 and STAR, SETA

1. STAR analyzes the allocation of the design in the FPGA.
2. Determines the most critical configuration bits.
3. Generates the coordinates of those critical bits.

```
Bit  96615 0x000c0400  199 Block=PIP_Conf  Net=/.config/Frame199/ISPFIFO/mem3(3)
```



Thank you for your attention
Q &A

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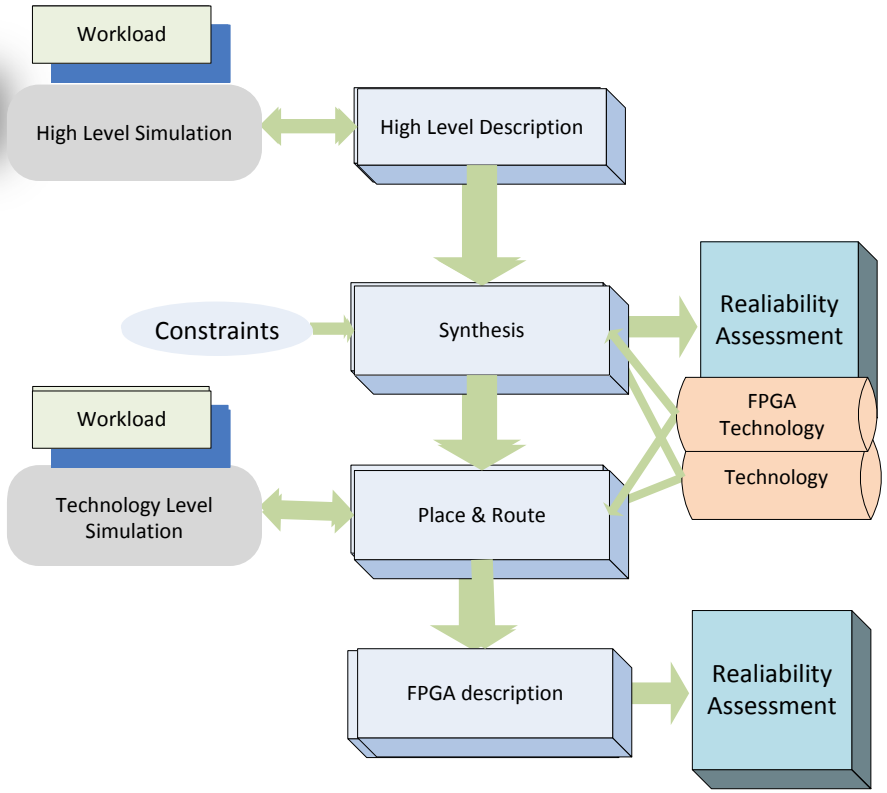
FT-UNSHADES2 in a nutshell: the design preparation flow



- Bitstream (.bit)
- Bit allocation file (.ll)
- Port location (.pin)
- VCD stimuli (*.vcd)

For FPGA flow

- **Configuration allocation (*.cl)**

1. Fit your design in the target FPGA
2. Allocate I/Os
3. Simulate and extract inputs
4. Finish the standard flow