

OVERVIEW

- Project Objective
- Work Package Descriptions
- Contract Change Notices
- Milestones
- ► DAREI80
- ► DARE90
- DARE180 CIS
- DAREI80 Support
- Future Work

PROJECT OBJECTIVE

▶ 180nm

- Provide a ready-to-use DARE180 library including all the views for the complete design flow
- Provide the necessary documentation including a data book

▶ 90nm

- Porting of DARE180 library to 90nm

WORK PACKAGES

► WPI	DAREI80 Library Maintenance and
	Data Book
► WP2.I	DARE90 Test Vehicle Design
► WP2.2	DARE90 Test Vehicle Manufacturing
► WP2.3	DARE90 Test Structure Characterization and Irradiation
► WP2.4	DARE90 Test Results Analysis and Library Definition
► WP2.5	DARE90 Library Porting
► WP2.6	DARE90 Documentation
► WP3	Further Consolidation of DARE ASIC's procurement for space

CONTRACT CHANGE NOTICES

- CCNI Work Planning Update
- CCN2 DAREI80 Porting to CIS (Sun Sensor)
 - WP CMI Preparing CIS Port
 - WP CM2 Digital I/O Port
 - WP CM3a LVDS Port
 - WP CM3b LVDS Power Optimization
 - WP CM4 Analog I/O Port
 - WP CM5 Digital Core Port
- CCN3 Budgetary Update for SEE Testing (increase of radiation time needed to obtain enough hits)

MILESTONES

▶ 21 December 2007

► 6 May 2008

► May 2008

26 September 2008

5 November 2008

March 2009

▶ 17 July 2009

28 October 2009

January 2010

July 2010

October 2010

October 2011

Kick Off Meeting

Architectural Design Review

CCNI (WPI)

DIE HARDER Tape-Out

CDR

TID test at UCL

KNUT2 Tape-Out

CCN2 (CIS)

DAREI80 Release V4.I

DAREI 80 CIS Release VI.0

SSOC Tape-Out

SEE test at INFN

CCN3 (SEE)

Final Presentation

WPI: DAREI80 LIBRARY MAINTENANCE AND DATA BOOK

- Updated DAREI80 design kit
 - Naming: DARE180_* iso RadHardUMC18_*
 - Small layout updates in DARE180_CORE
 - Characterization flow based on ELC (previously SignalStorm)
 - Fully scripted layout verification (DRC, LVS, ANT, LPE)
 - Additional RAD check
 - Encounter based back-end flow (previously Astro)
- DAREI80 Data Book
 - HTML generated with ELC (Encounter Library Characterizer)
- RAM simulation report
 - "DARE90_WPI_SRAM_simulation_report.pdf"
 - "LEONDARE SRAM simulation report.pdf"

DAREI 80 VIRTUOSO DATABASE

Schematic Update:

- CORE, IO, IOa, PLL, LVDS, (SRAM)
- Conversion script from old to new database for schematics and symbols

Layout Update:

- Conversion script based on GDSII layer remapping
- PG tracks set to lum
- top metal 20kA (MM-RF processing)
- SAB layer (DRC)
- MMSYMBOL layer added (LVS)
- new bondpad (oxide studs)
- minimum area rules (DRC e.g. polysilicon, metal, ..)

DAREI80 DATABASE VERIFICATION

DRC

- Automated verification scripts for complete library
- LVS
 - Include extraction for ELT
 - Automated verification scripts for complete library
- ► LPE
 - Based on LVS verification scripts
 - Extraction of parasitic capacitors and resistors
 - Reduction of complex RC circuits (trade-off between accuracy and simulation speed)

DAREI80 CHARACTERIZATION

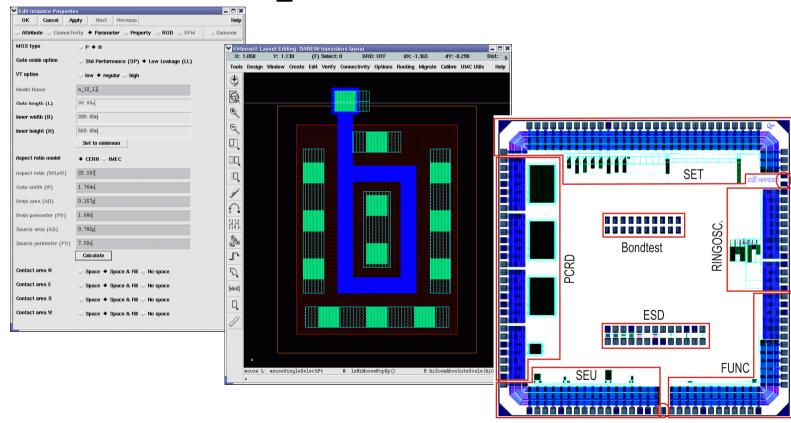
- SignalStorm -> ELC
 - CORE and IO
 - Fully scripted approach
 - HIT cells are included in the flow
 - Automated generation of databook (html)
 - Verilog, Vital, lib/db
- Ocean (spectre)
 - LVDS and PLL
 - A lot of scripting to generate the views
 - Verilog, Vital, lib/db, html

DAREI80 SRAM COMPILER

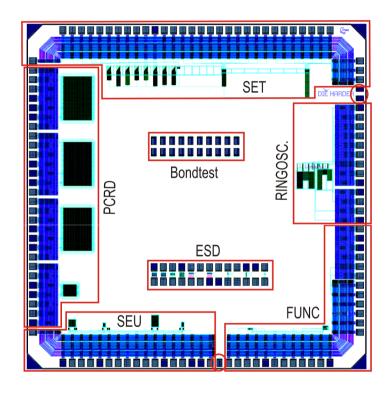
- Single Port Compiler
- Non functional medium and big size sram instances
- Simulation
 - High capacity spice simulator used (Ultrasim)
 - Based on schematic -> all OK
 - Based on layout with parasitic C extraction -> all OK
 - Based on layout with full RC networks -> timing problem in medium sized and big SRAMs
- Solution is being implemented in DARE+ contract (KO June 2011)

WP2.1: DARE90 TEST VEHICLE DESIGN (1/3)

- Detailed design and layout database
 - Cadence IC 5.1.41
 - UMC PDK C01_PB



WP2.1: DARE90 TEST VEHICLE DESIGN (2/3)



DIE_HARDER

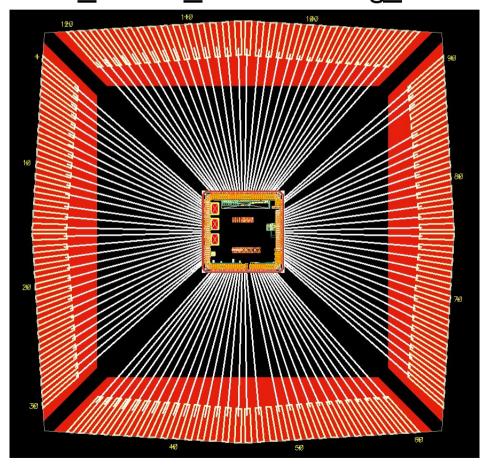
- Functional test structures (combinatorial & sequential)
- Ring oscillators (TID)
- 1024 bits shift registers with different (ELT, GB) physical countermeasures against radiation defects (TID)
- 64 bits shift registers based on flip-flops or latches using either DARE90 (ELT, GB, HIT) or commercial implementation (SEU)
- Test structures for sensitivity measurements on RESET, DATA and CLOCK input of DARE90 flip-flop (SET)
- Test structures for measuring drive strength impact (SET)
- ESD, bonding pads

WP2.1: DARE90 TEST VEHICLE DESIGN (3/3)

- ► Test structures detailed design report:
 - "DARE90_WP2.I_DDR.pdf"
- ► Test structures characterization test plan:
 - "DARE90_WP2.I_TestPlan_version1.8.pdf"
- ► Test structures irradiation test plan:
 - "DARE90_WP2.I_TestPlan_version1.8.pdf"

WP2.2: DARE90 TEST VEHICLE MANUFACTURING

► Approximate 50 dies (40 packaged in CPGA120) "DARE90_WP2.2_Manufacturing_version1.0.pdf"



WP2.3: DARE90 TEST STRUCTURE CHARACTERIZATION AND IRRADIATION

Microtest

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"DARE90_TestReport_v1.13_12May2009.pdf"

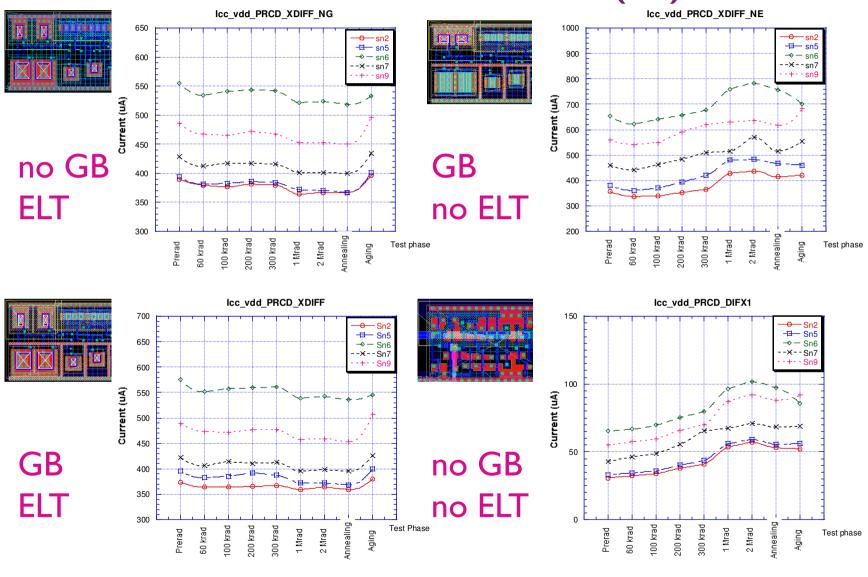
"DARE90_IrradiationTestReport_v1.2.pdf"

"dare90_RAD_drift_30apr09.xls"
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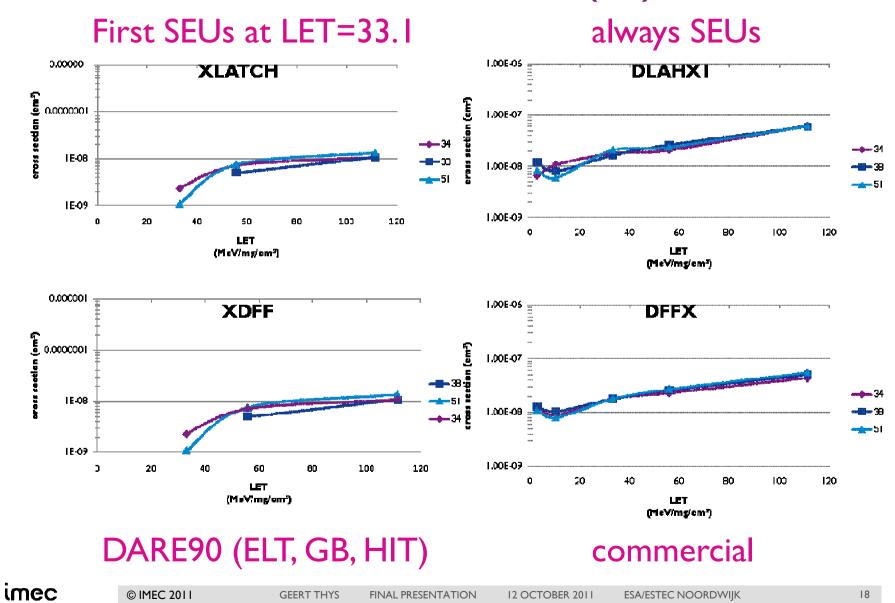
- Maprad
 - "TID-DARE990v10.pdf"
 - "Addendumv I 3.doc"
- Imec

"P-61287-IM-10-TR-01.pdf"

WP2.4 DARE90 TEST RESULTS ANALYSIS AND LIBRARY DEFINITION (1/3)



WP2.4 DARE90 TEST RESULTS ANALYSIS AND LIBRARY DEFINITION (2/3)

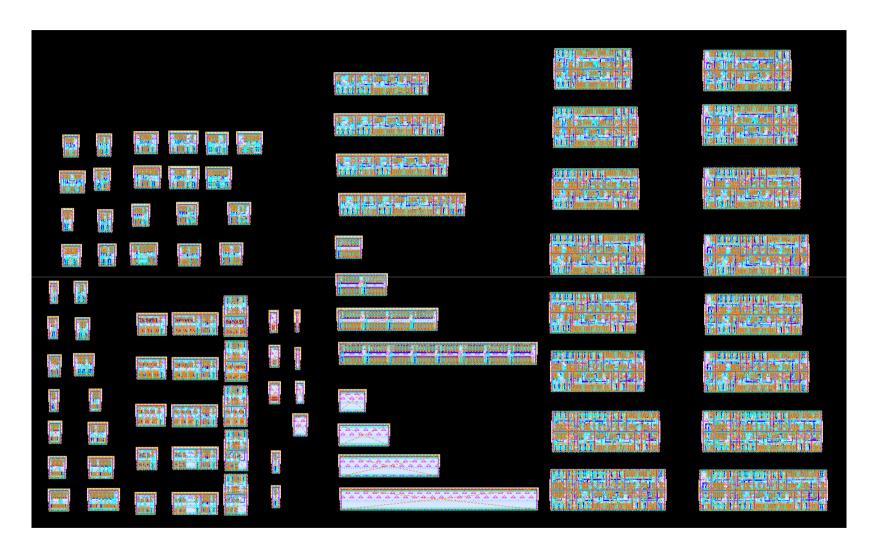


WP2.4 DARE90 TEST RESULTS ANALYSIS AND LIBRARY DEFINITION (2/3)

► TID:

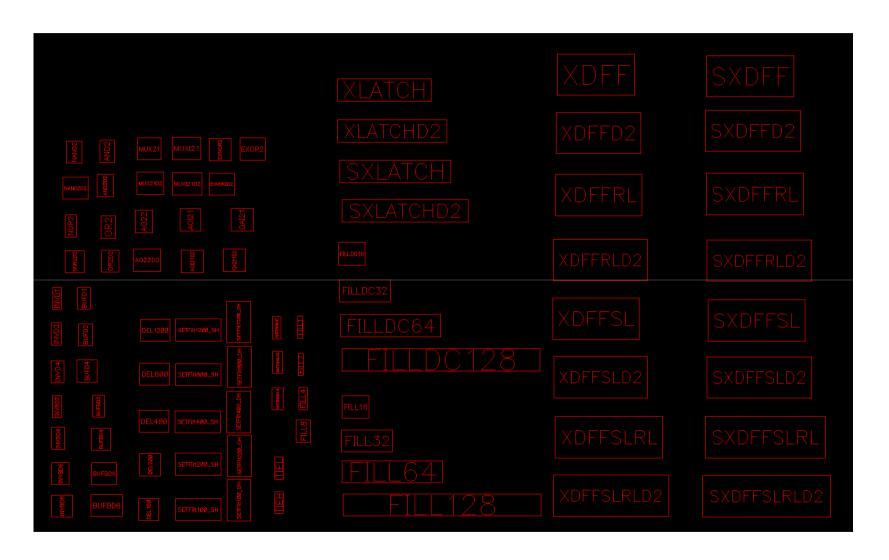
- I.2V SP transistor: no ELT
- 3.3V IO transistor: ELT
- Guard bands
- ► SEU:
 - HIT cell
- ► SET:
 - UMC 90nm = (very) sensitive
 - Limited drive strength hardening (power)
 - Pulse filtering (area)
- ► SEL:
 - Guard bands

WP2.5 DARE90 LIBRARY PORTING (1/9)





WP2.5 DARE90 LIBRARY PORTING (2/9)





WP2.5 DARE90 LIBRARY PORTING (3/9)

Combinatorial (40)

NAND2 NAND2D2 AND2 AND2D2

- NOR2 NOR2D2 OR2 OR2D2

- EXNOR2 EXNOR2D2 EXOR2

- AOI21 AOI21 D2 OAI21 OAI21 D2

- AO22 AO22D2

- BUFDI BUFD2 BUFD4

- INVDI INVD2 INVD4
- BUFBD2 BUFBD4 BUFBD6 BUFBD8
- INVBD2 INVBD4 INVBD6 INVBD8
- DEL100 DEL200 DEL400 DEL800 DEL1200
- MUX21 MUX21D2 MUXI21 MUXI21D2

WP2.5 DARE90 LIBRARY PORTING (4/9)

Sequential (18)

- XDFF XDFFD2 SXDFF SXDFFD2

- XDFFRL XDFFRLD2 SXDFFRL SXDFFRLD2

XDFFSL XDFFSLD2
 SXDFFSL SXDFFSLD2

- XDFFSLRL XDFFSLRLD2 SXDFFSLRL SXDFFSLRLD2 (*)

- XLATCH XLATCHD2 SXLATCH SXLATCHD2

► SET Filters (10)

- SETFilt100 DH SETFilt100 SH

- SETFilt200_DH SETFilt200_SH

- SETFilt400_DH SETFilt400_SH

- SETFilt800_DH SETFilt800_SH

- SETFilt1200_DH SETFilt1200_SH

^{*} Not released due to functional error in some process corners after post-layout simulation

WP2.5 DARE90 LIBRARY PORTING (5/9)

- Place & Route (15)
 - Filler cells:

FILL1 FILL2 FILL4 FILL8 FILL16 FILL32 FILL64 FILL128

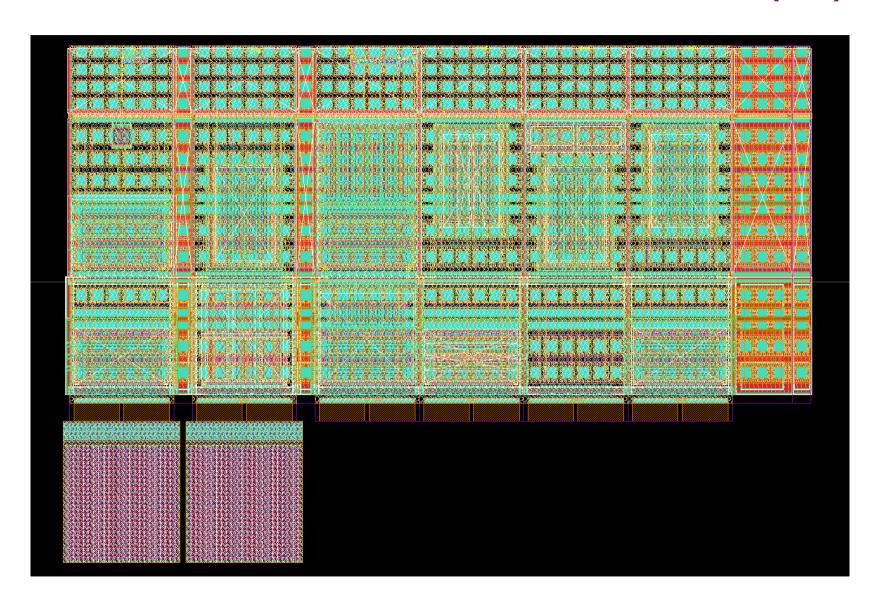
- Filler cells with decoupling:
 FILLDC16 FILLDC32 FILLDC64 FILLDC128
- Tie cells:

TIEH TIEL

- Antennafix cells:

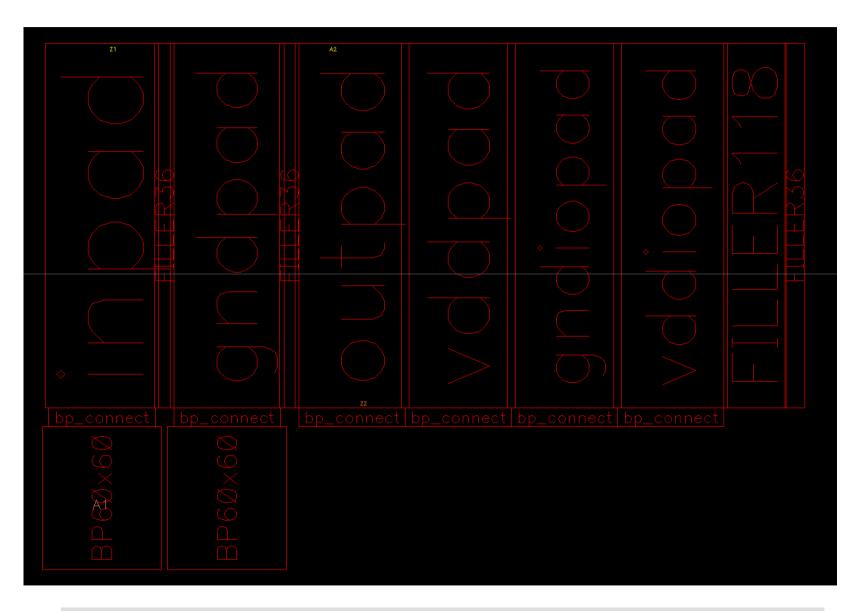
ANTENNAXI

WP2.5 DARE90 LIBRARY PORTING (6/9)





WP2.5 DARE90 LIBRARY PORTING (7/9)



WP2.5 DARE90 LIBRARY PORTING (8/9)

- Power & Ground (4)
 - Vddpad Gndpad
 - Vddiopad Gndiopad
- ► Input & Output (2)
 - Inpad
 - Outpad
- Place & Route (5)
 - FILLER36
 - FILLER 118
 - CORNER
 - BP60x60
 - bp_connect

WP2.5 DARE90 LIBRARY PORTING (9/9)

- ► UMC L90N IP9M2TIF Low K Logic
- # CORE cells = 83
- ▶ # I/O cells = I I
- CORE voltage = 1.2V
- ► I/O voltage = 3.3V
- I/O compatible with Mixed-Mode options
- I/O functional with only 4 metal layers
- Layout, schematic, symbol, cdl, spectre, liberty, verilog, vital, html, lef
- Fully scripted layout verification flow
- ELC based characterization flow

WP2.6 DARE90 DOCUMENTATION

- ► ELC based flow generates HTML style data book
- User manuals available for
 - DARE90_CORE
 - DARE90_IO



WP3 FURTHER CONSOLIDATION OF DARE ASIC'S PROCUREMENT FOR SPACE

- Document available "DARE90_WP3_Consolidation.doc"
- Continuous DARE support
- Continuous additions
- New requests every month



WP CMI PREPARING CIS PORT

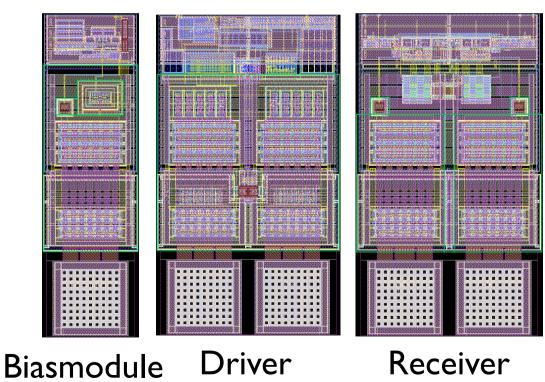
- No change to schematics
- No change to layout of CORE cells
- Big impact on layout of I/O cells
 - 4 metal layers
 - Extra cells
 - ESD issues
- Conversion script to remove VIA4, METAL5, VIA5 and METAL6
- Manual fix of 'lost' functionality
- Reuse of layout verification scripts from DARE180
- Reuse of ELC scripts for characterization

WP CM2 DIGITAL I/O PORT

- Limited set of DARE180 10 ported
- Only 110x110 bondpad available
- Optimization of metal4 use (IR drop, ESD)
- Addition of ESD_NOBP (full set of PG protections, but without bondpad)
- Addition of ESD_APD (anti-parallel diodes to be placed between grounds of different domains)

WP CM3A LVDS PORT

- DAREI80_LVDS ported
 - LVDS_Driver
 - LVDS_Receiver
 - LVDS_Biasmodule





WP CM3B LVDS POWER OPTIMIZATION

- Power down input added
- Exploratory simulations done
 - Stability
 - Power
 - Speed
 - LVDS standard
- Implementation not part of the contract

WP CM4 ANALOG I/O PORT

- DARE180_IOa ported, except GNDA18PAD and VDDA18PAD
 - IANALOG
 - OANALOG
 - VDDA33PAD
 - GNDA33PAD
- Addition of IANALOG_NOESD (low capacitance)
- Addition of VDDREG18PAD, VDDREG33PAD,
 VDD50PAD and GND50PAD (voltage regulators)
- Addition of 5V ESD clamp

WP CM5 DIGITAL CORE PORT

- Direct import of DARE180_CORE layouts
- ► LPE with CIS specific rules file
- Recharacterization with CIS models
- Addition of 'metall reprogrammable' SetReset HIT-FF



DAREI80 SUPPORT (1/2)

- ► TESAT-KNUT2
 - ESD update
 - Large bondpads
- ► ETCA-LEONDARE
 - LVDS power
 - Radiation test results

DAREI80 SUPPORT (2/2)

► ARQUIMEA-REDSAT2

- TESAT-LARSI
 - Double I/O row:TUNNEL,TCORNER
 - DAREI80_DAC and DAREI80_ADC
 - Vital models
 - SDF generation

FUTURE WORK (1/2)

- Update layout of HIT based cells
- DICE iso HIT
- Triple well
- Simulate SEE
- Implement lower power flow (90nm)
 - Clock gating cells
 - Level shifters
 - Isolation cells
 - Power switches
 - Transistor flavour (RVT/HVT/LVT)
 - Process flavour (SP/LL)
- Implement methodology for pulse filter insertion into digital flow

FUTURE WORK (2/2)

- Expand I/O library (90nm)
 - 2.5V
 - Output drive strength
 - Slew rate control (SSO)
 - Schmitt
- ► SRAM (90nm)
- Characterization with ECSM (90nm)
- Follow EDA tools evolution:
 - ALTOS iso Encounter Library Characterizer
 - PDK version C02_PB is available (DARE+)
 - Cadence IC6 (DARE+)



