DAC2401
Very High Resolution DAC
for Space Applications

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Outline

- System overview
- Features
- Architecture
- Radiation hardening
- Static performance specifications
- Dynamic performance specifications
- Low frequency noise characterization
- Conclusions
- Next steps
Product highlights

- **Features**
  - Architecture: multi-bit ΣΔ modulator
  - Output stage: differential current steering
  - Digital input interface: Synchronous serial data format (Clock, Data, Valid)
  - Bandwidth: DC to 330kHz
  - Selectable oversampling ratio: selectable x256, x128, x64, x32
  - Sampling frequency up to 2MSa/s
  - 1.2V digital power supply & 3.3V analog power supply
  - Radiation tolerant design: >100kRad Total Dose immunity verified

- **Operating modes**
  - Normal
  - Bypass
  - Test
  - Power down

- **Applications**
  - High accuracy instrumentation, measurement and actuator drive for aerospace systems.
System Overview

DAC2401

1.2V

- Input interface
- I²C interface
- Clock Distribution network
- DFT

- Interpolation stage
- 3rd order \( \Sigma \Delta \) modulator
- DWA

3.3V

- Level Shifters (1.2 - 3.3V)
- DAC 1 (Main)
- Reference block
- DAC 2 (Redundant)

- SDIN
- SCLK
- SYNC
- SDA
- SCL
- MCLK
- Test signals
- OUTP1
- OUTM1
- Ref. Voltage
- OUTP2
- OUTM2

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DAC2401 - Company confidential
**Architecture: Digital part (2/2)**

- **Modulator design**
  - 3rd order feed-forward $\Sigma\Delta$ modulator
  - 5-bit quantizer
  - Idle Tone avoidance by introduction of dither

- **Dynamic Element Matching (DEM)**
  - The output element mismatch error is minimized by the use of a DEM algorithm.
  - Data Weighted Averaging (DWA) as an efficient DEM algorithm.
  - Algorithm's objective → **achieve an equal use of elements in long-term by rotating the output elements (current sources) in a cyclic fashion.**
  - DWA uses only one index, which is updated with the addition of the input every clock cycle.
Bandgap cell provides an accurate reference voltage (1.2V) with a low temperature coefficient.
First order RC filter reduces any noise from the bandgap block.
Low noise Op-Amp along with M1 and current setting resistor (R_{ref} or R_{ext}) implements the reference current source for generating the reference current I_{ref}.
I_{Ref} can be set by selecting the internal resistor R_{Ref} or connecting an external resistor R_{ext}.
32x differential elementary current sources built around the regulated cascode topology.
Use of PMOS transistors for lower flicker noise(1/f) and high linearity.
Radiation hardening techniques

- **Technology level:** ST Microelectronics HCMOS9 0.13 um is a rad-hard proven technology.

- **Library level:** For the digital part the most oversized and robust standard cells were used (including latches and flip-flops).

- **Digital design level**
  - Fault masking by TMR (e.g. FSMs)
  - Synchronous reset
  - Reset assertion in the SINC block every 32 clock cycles

- **Analogue design level**
  - Current source transistors with increased W/L ratio for increased capacitance and driving power.

- **Layout level**
  - Deep N-well isolation (NISO): The entire digital part and all the NMOS devices of the analogue part are placed inside a deep n-well to minimize digital feed-through and latch-up susceptibility (see slide 10).
  - P+ guard rings surround the n-channel devices to cut any possible radiation induced parasitic paths.
  - Increased distance between the p+ diffusion in the well and the n+ in the substrate.
  - Increased number of substrate and well contacts.
Deep N-Well isolation (NISO)
- Minimizes the digital feed-through to the sensitive analog nodes
- Improves the latch-up immunity

Layout and polarization scheme (ST's rules)

Diagram of layout showing N-Well, P-Well, NMOS, and PMOS components with deep N-Well isolation.
Floorplan and fabrication highlights – Prototype

- **Technology**: 0.13um HCMOS9-GP ST-Microelectronics™ 6 metal layers
- **Dimensions**: ~ 1840 x 1840 um
- **Total area**: 3.42mm²
- **No of I/O pads**: 43
- **Minimum pad-to-pad spacing**: 90um
Static electrical parameters outline

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value (TYP)</th>
<th>Unit</th>
<th>Condition - remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDa</td>
<td>Digital current consumption</td>
<td>0.97</td>
<td>mA</td>
<td>Normal mode, no clk</td>
</tr>
<tr>
<td>IDb</td>
<td>Digital current consumption</td>
<td>1.33</td>
<td>mA</td>
<td>Normal mode, with input</td>
</tr>
<tr>
<td>PD</td>
<td>Digital power consumption</td>
<td>1.6 (typ)</td>
<td>mW</td>
<td>Normal mode, with input</td>
</tr>
<tr>
<td>IAa</td>
<td>Analog current consumption</td>
<td>4.22</td>
<td>mA</td>
<td>Normal mode, BG ON, with input, Internal RREF=219Ω</td>
</tr>
<tr>
<td>IAb</td>
<td>Analog current consumption</td>
<td>20.3</td>
<td>mA</td>
<td>Normal mode, BG OFF</td>
</tr>
<tr>
<td>PA</td>
<td>Analog power consumption</td>
<td>66.8 (typ)</td>
<td>mW</td>
<td>Normal mode, with input</td>
</tr>
<tr>
<td>Pt</td>
<td>Total power consumption (PD+PA)</td>
<td>68.4 (typ)</td>
<td>mW</td>
<td>Normal mode, with input</td>
</tr>
<tr>
<td>I_{CM}</td>
<td>Common mode current</td>
<td>2.85</td>
<td>mA</td>
<td>Per DAC polarity</td>
</tr>
<tr>
<td>I_{diff(FS)}</td>
<td>Full-scale output differential current</td>
<td>± 3.6</td>
<td>mA</td>
<td>Normal mode</td>
</tr>
<tr>
<td>Vbg</td>
<td>Internal bandgap voltage</td>
<td>1.192</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>e(offset)</td>
<td>Offset error</td>
<td>&lt; 1</td>
<td>uA</td>
<td></td>
</tr>
<tr>
<td>INL/DNL</td>
<td>Differential / Integral non-linearity</td>
<td>&lt; 0.5 LSB</td>
<td>LSB</td>
<td>@ 13 bit resolution</td>
</tr>
</tbody>
</table>

→ The analog current/power consumption can be reduced by using an external resistor of higher value.
Dynamic performance – Time domain

Sine 1.33kHz, -1dBFS, MCLK=20.48MHz, Fs=80kSa/s

Sine 13.3kHz, -1dBFS, MCLK=20.48MHz, Fs=80kSa/s
Dynamic performance FFT

- Differential measurement
- Sine 100Hz/ -10dBFS
- MCLK = 1.536MHz
- FFT BW 22Hz to 22kHz
- Blackman – Harris
- 32768 FFT points

⇒ THD+N better than 100dB
Low frequency noise DC – 0.1Hz
Low frequency noise DC – 0.1Hz
Conclusions

- A monolithic, radiation hardened 24-bit DAC targeting space applications has been designed, fabricated in 0.13um CMOS and validated in terms of electrical performance and radiation tolerance.
- At low frequencies the DAC exhibits an SNR of 118dB and a THD+N figure >100dB, with a total power consumption of less than 70mW.
- The device is capable of operating in sampling frequencies exceeding the 1MSa/s
- Total Dose characterized up to 100 krad without any sign of performance degradation or functional interrupt.
Modifications to be done

- Eliminate the 1.2V
- Change the output to voltage-differential
- Put a standard SPI interface
- Change the return-zero strategy
Thank you for your attention!