Agenda – 11th of September 2013

14:00 Introduction
14:15 CWICOM Description & Architecture
14:45 CWICOM Packaging, Technology & Status
15:00 CWICOM Commercialization
15:15 CWICOM Validation
15:45 Coffee Break
16:15 CWICOM Hardware Demonstration
16:45 Conclusion & Questions
17:00 End of Meeting

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Introduction

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Introduction

- Space applications are **more and more demanding** in terms of **image compression performances** : instrument resolution, data rate, agility and swath are continuously increasing
- This concerns both **Earth observation** and **scientific missions**
- It multiplies by 10 the volume of picture acquired on one orbit
- In parallel, the satellites size and mass are decreasing, requiring innovative electronic technologies reducing size, mass and power consumption

- In this context and **in the frame of an ESA contract**, Astrium has developed a new image compression ASIC : the **CWICOM**

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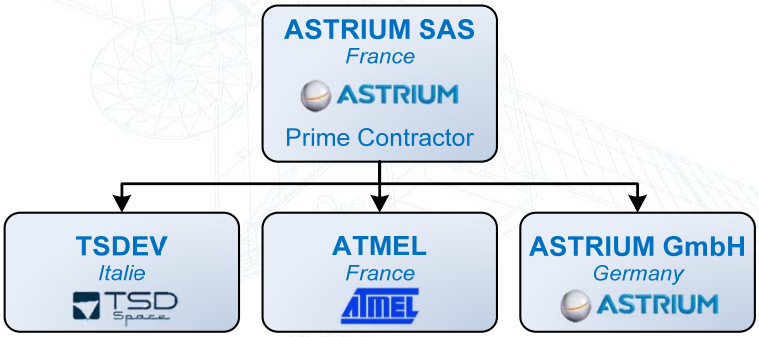
Industrial Organization

- The CWICOM project consortium is constituted by :
  - **Astrium Satellites SAS** (France)
  - **Astrium Satellites GmbH** (Germany)
  - **Techno System Development** (Italy)
  - **Atmel** (selected as foundry for the CWICOM ASIC)



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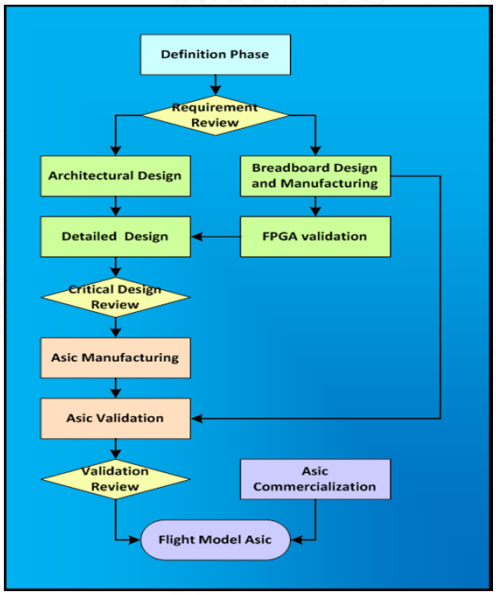
Development Flow



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CWICOM Description

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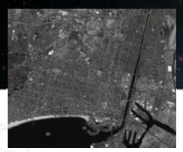
Objectives

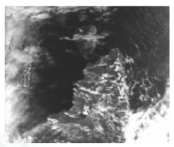
Develop a high-performance image compression ASIC :

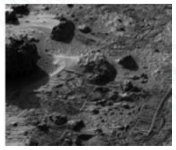
- Compressing with CCSDS image compression standard
- Delivering data with CCSDS packet protocol standard
- Reaching a high data rate of 60 Mpix/s
- Processing pixels up to 16 bits
- Supporting image width up to 2600 pixels (S2)

This is what achieved the **CWICOM** development

CWICOM stands for **C**CSDS **W**avelet **I**mage **COM**pression ASIC, and is developed in the frame of an ESA contract







CCSDS The Consultative Committee for Space Data Systems

esa

CWICOM

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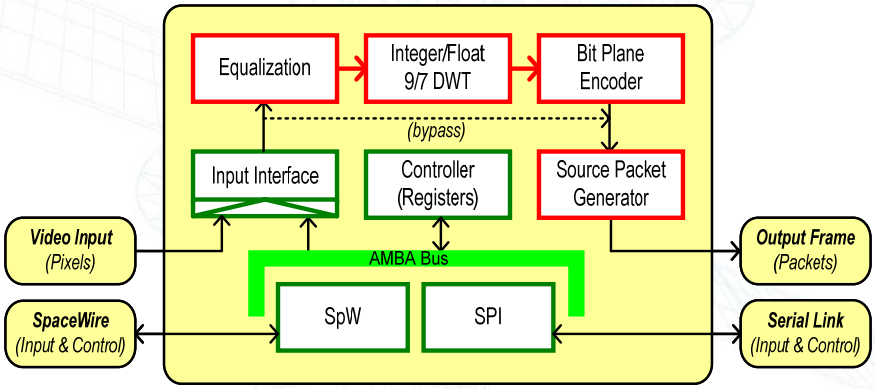
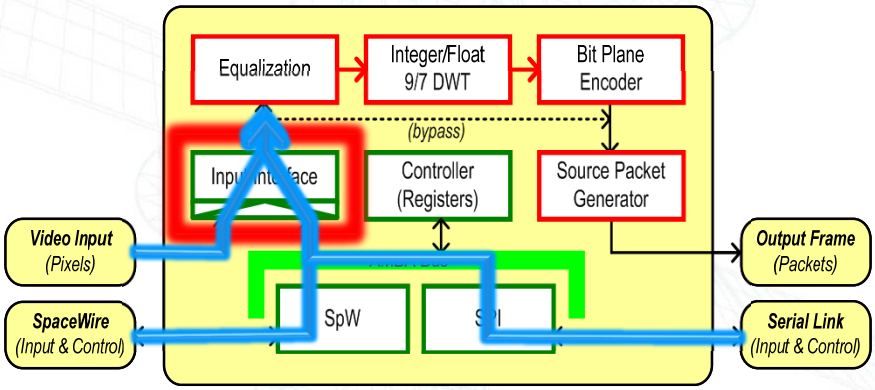
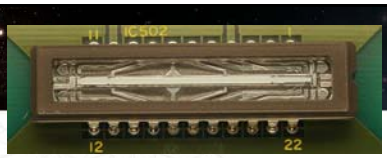
CWICOM General Block Diagram



CWICOM Input Interfaces

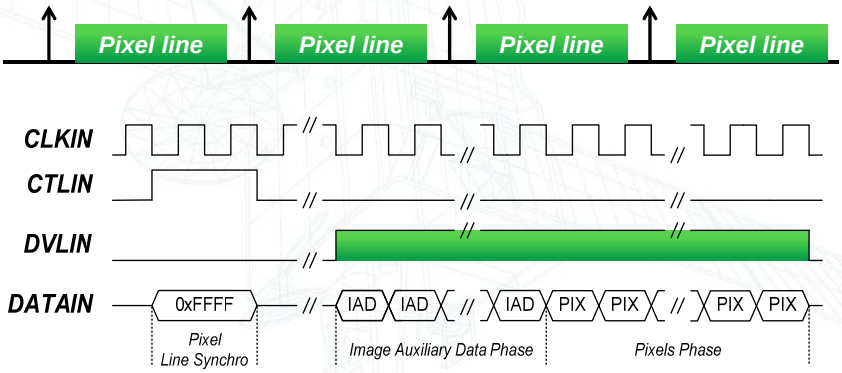


Input Interfaces

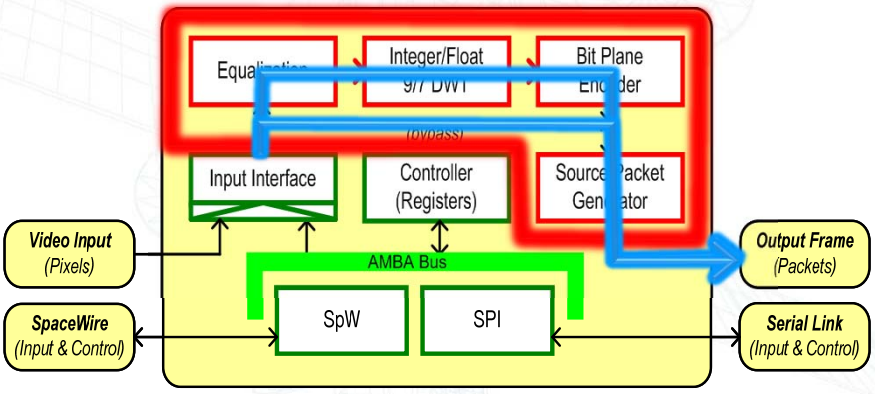


- Parallel Input Interface, SPW or SPI
- Up to 16 bits pixels
- Up to 3496 pixels per line

Line-CCD

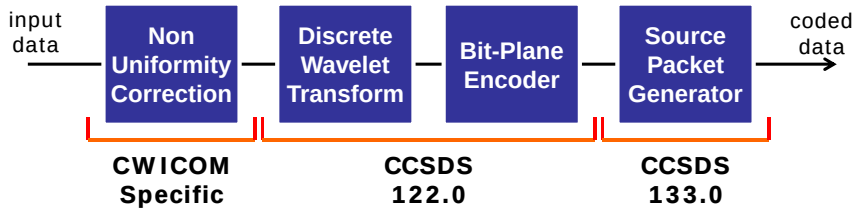


CWICOM Compression Core



CWICOM Compression Core

- CCSDS Standard for Data Compression → **CCSDS 122.0-B-1**
- CCSDS Space Packet Protocol → **CCSDS 133.0-B-1**



CCSDS WAVELET IMAGE COMPRESSION MODULE

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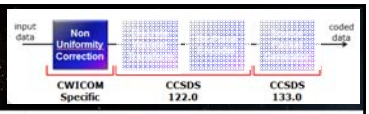
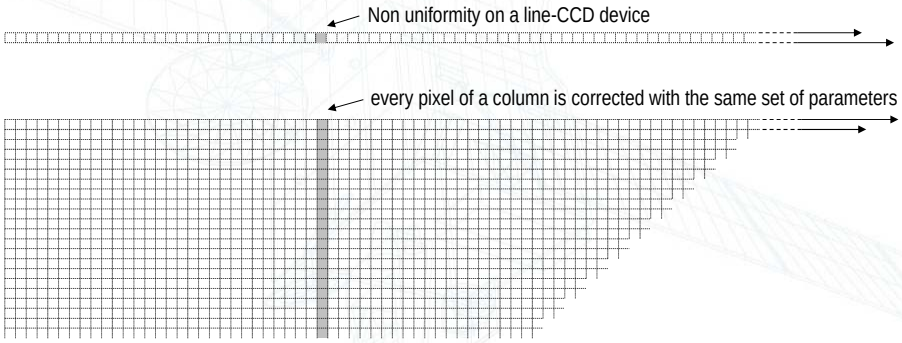
Pixel Equalization



- The equalization consists in a Non-Uniformity Correction (NUC) applied to correct the **non uniform response**/sensitivity of the line-CCD device
- It performs a bi-linear **correction** on each pixel in a image line
- Equalization can be **bypassed** to keep the input pixels unchanged



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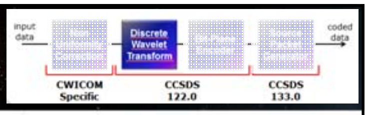
Wavelet Transform

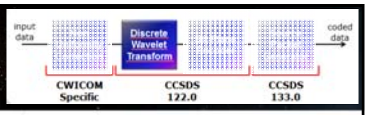


PIX1 | PIX2 → LF | HF

- Example of a very simple 2-tap filtering :
  - ***LF* = (*PIX1* + *PIX2*) / 2**
    → Low-pass Filter
    → Takes information from the average value of the two pixels
  - ***HF* = (*PIX1* – *PIX2*) / 2**
    → High-pass Filter
    → Takes information from the gap between the two pixels
- This mathematical operation is **fully reversible**

CWICOM ASTRIUM

Wavelet Transform



- 1D DWT (Discrete Wavelet Transform) of one line (one row) of pixels

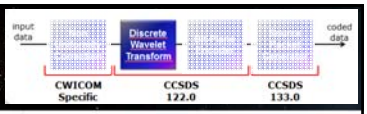
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF

- 2D DWT Level 1: First step → DWT on rows

B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF
B0	B0	B0	B0	B0	B0	B0	B0	→	LF	HF	LF	HF	LF	HF	LF	HF

CWICOM ASTRIUM

Wavelet Transform



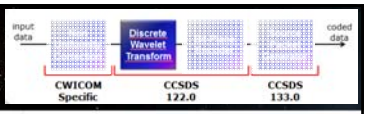
- 2D DWT Level 1 : Second step
  → DWT on columns

LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF
LF	HF	LF	HF	LF	HF	LF	HF

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

B1	V1	B1	V1	B1	V1	B1	V1
H1	D1	H1	D1	H1	D1	H1	D1
B1	V1	B1	V1	B1	V1	B1	V1
H1	D1	H1	D1	H1	D1	H1	D1
B1	V1	B1	V1	B1	V1	B1	V1
H1	D1	H1	D1	H1	D1	H1	D1
B1	V1	B1	V1	B1	V1	B1	V1
H1	D1	H1	D1	H1	D1	H1	D1

Wavelet Transform

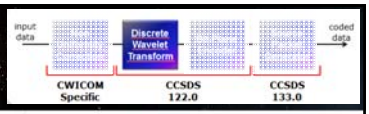


- Low-pass and High-pass filters generate different sub-bands B, V, H, D

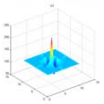
B1	V1	B1	V1	B1	V1	B1	V1	→	B1	B1	B1	B1	V1	V1	V1	V1
H1	D1	H1	D1	H1	D1	H1	D1	→	B1	B1	B1	B1	V1	V1	V1	V1
B1	V1	B1	V1	B1	V1	B1	V1	→	B1	B1	B1	B1	V1	V1	V1	V1
H1	D1	H1	D1	H1	D1	H1	D1	→	B1	B1	B1	B1	V1	V1	V1	V1
B1	V1	B1	V1	B1	V1	B1	V1	→	H1	H1	H1	H1	D1	D1	D1	D1
H1	D1	H1	D1	H1	D1	H1	D1	→	H1	H1	H1	H1	D1	D1	D1	D1
B1	V1	B1	V1	B1	V1	B1	V1	→	H1	H1	H1	H1	D1	D1	D1	D1
H1	D1	H1	D1	H1	D1	H1	D1	→	H1	H1	H1	H1	D1	D1	D1	D1

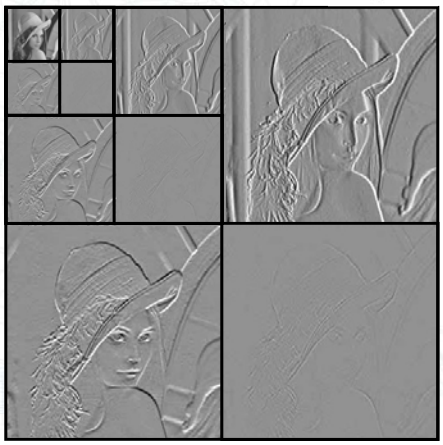
- After a first 2D DWT, the elements of the B sub-band are grouped and used as input for a second DWT filtering
- After this second DWT, once again the resulting B sub-band is used as input for a third DWT filtering

Wavelet Transform

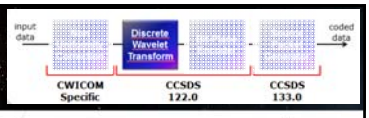


- This means that DWT is applied 3 times
  → 3 levels of decomposition

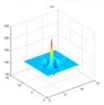


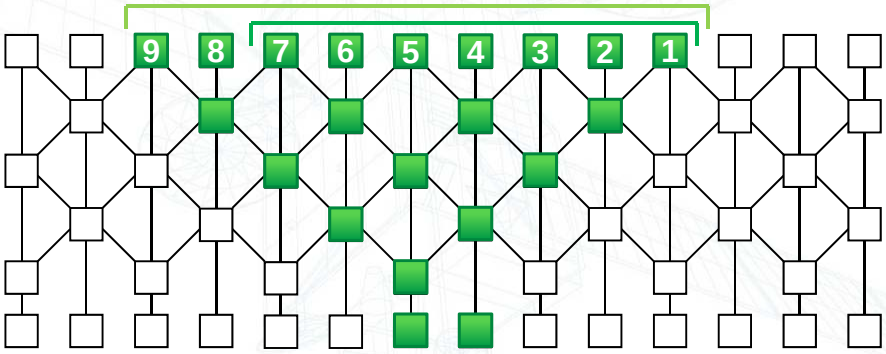


Wavelet Transform

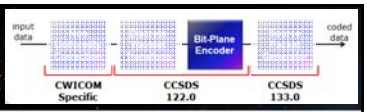


- CCSDS standard describes two DWT filters with 9 & 7 taps :
  a 9/7 float filter and a 9/7 integer filter
- Both are implemented inside the CWICOM

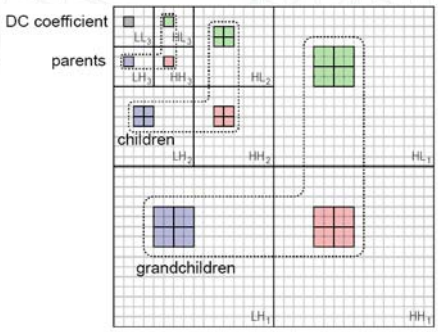




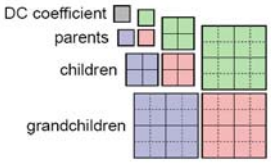
Bit plane encoder



- The coding is performed **bit plane after bit plane**, on groups of consecutive **blocks** called **segments**, with an **entropy coding** using variable-length codewords



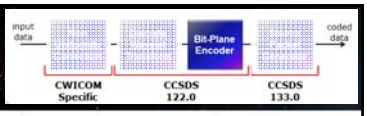
wavelet-transformed image



a single block

- Blocks are constituted by 64 coefficients

Bit plane encoder



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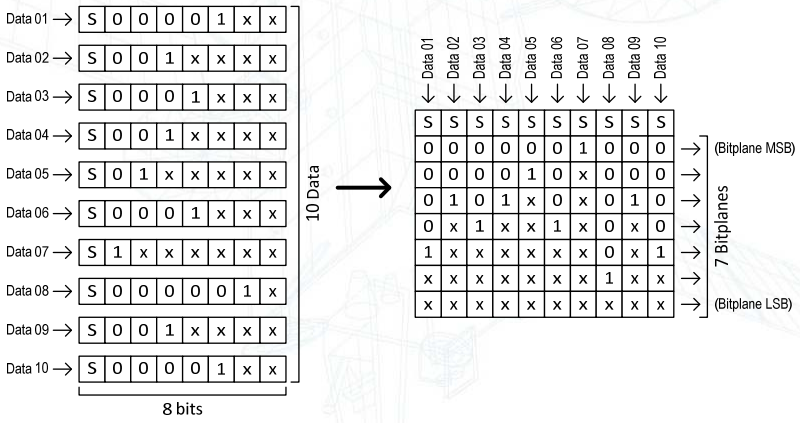
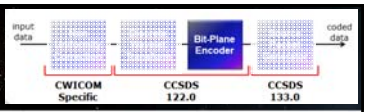


Bit plane encoder



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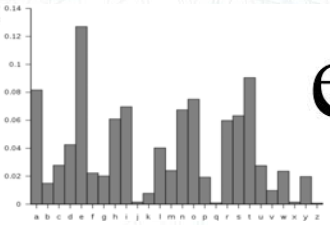
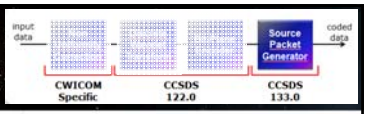
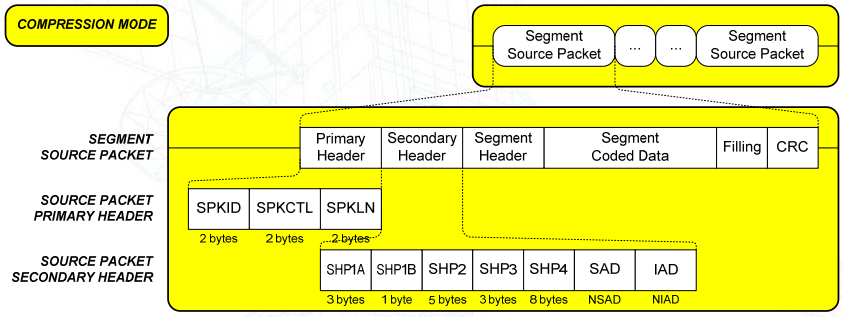
ASCII Alphabet			
A	1000001	N	1001110
B	1000010	O	1001111
C	1000011	P	1010000
D	1000100	Q	1010001
E	1000101	R	1010010
F	1000110	S	1010011
G	1000111	T	1010100
H	1001000	U	1010101
I	1001001	V	1010110
J	1001010	W	1010111
K	1001011	X	1011000
L	1001100	Y	1011001
M	1001101	Z	1011010



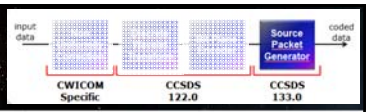
CCSDS Packets



- Data (compressed or bypassed) are embedded with insertion of standard headers in order to generate a CCSDS source packet



CCSDS Packets



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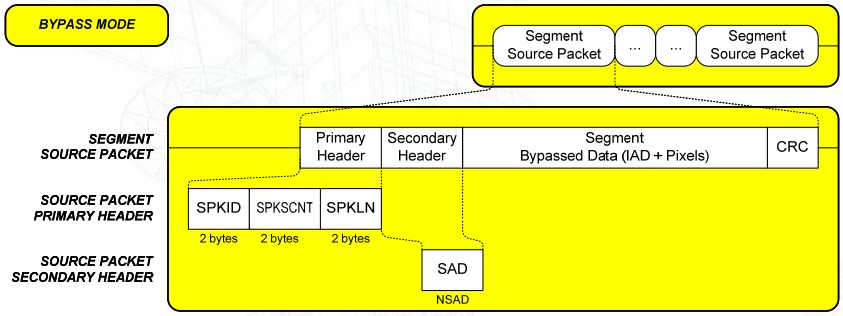
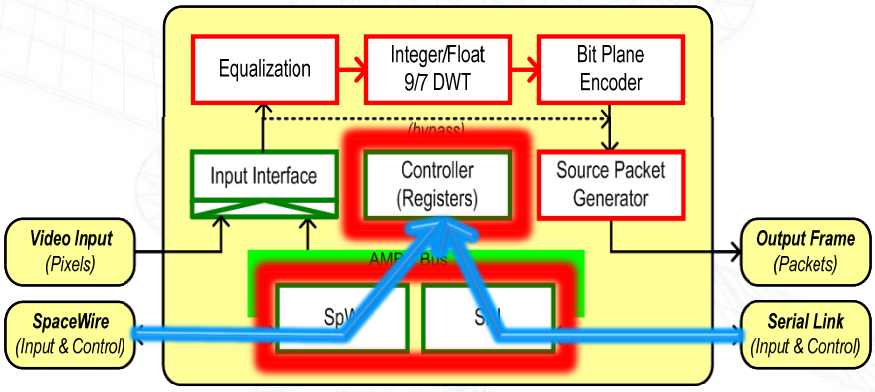


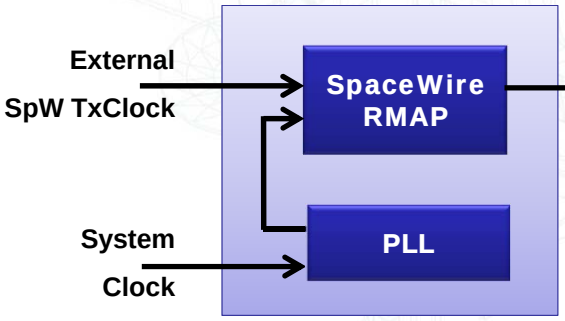
CWICOM Control



CWICOM Control - Links

- CWICOM is easily configurable and can be controlled through a standard serial link interface, either **SPI** or **SPW** link:
  - **SPW-RMAP** (Remote Memory Access Protocol → ECSS-E-50-11)
  - **SPI serial link**

→Both links give access to all of the **CWICOM internal registers**



SpW TxClock source is either external or internal

if source is internal, it is generated from the System Clock by an internal PLL

CWICOM Control - Commands

- The configuration consists in the programming of some registers to define image size, pixel dynamic, CCSDS output header…, in the load of equalization parameters and finally in a single command
  - **CONF command**

    To configure the quality mode by a truncation at a specified point (bit plane number and coding stage)

    To configure if we are in compression or bypass mode

    To define the DWT filter type (9/7 Integer or 9/7 Float)

- After configuration, the CWICOM is able to perform image compression with only two commands → **ease of use**
  - **START command**

    To start the compression
  - **STOP command**

    To stop the compression

CWICOM Architecture

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CWICOM Breakthrough

60 Mpix/s

Classical TVHD image 720p = 1280 x 720 = 921 600 pixels

So CWICOM Data Rate is equivalent to 60 TVHD images per second

CWICOM

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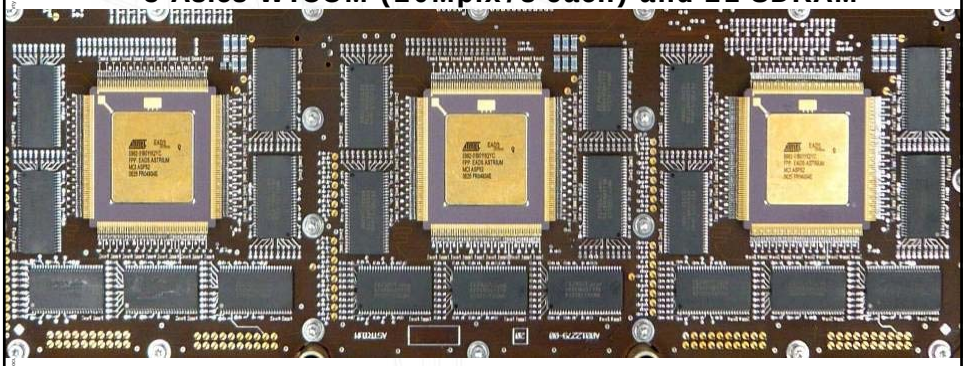
CWICOM Breakthrough

60 Mpix/s

3 Asics WICOM (20Mpix/s each) and 21 SDRAM



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CWICOM Breakthrough

60 Mpix/s

3 Asics WICOM (20Mpix/s each) and 21 SDRAM

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The 60Mpix/s challenge

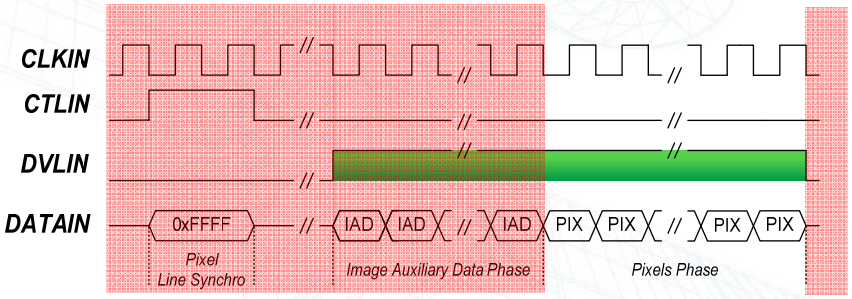
- First, CWICOM architecture implements **pipelined data flows**
- Then CWICOM architecture implements a very efficient **internal embedded memory** organization
- → It allows **higher data rate** performances because sharing an external memory between functional blocks is one of the main source of **bottleneck** in processing architectures

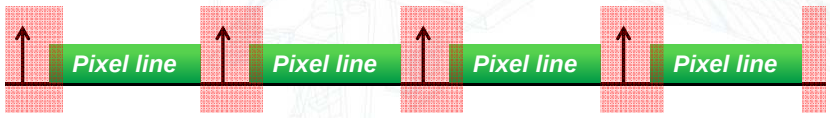
60 Mpix/s

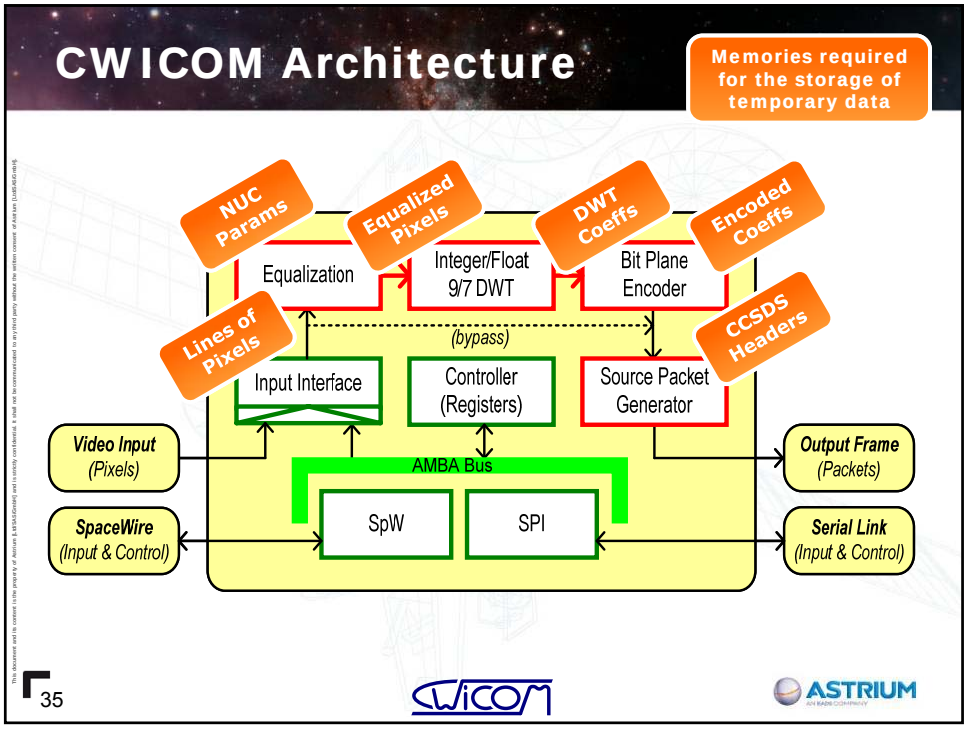
- → Moreover, it avoids the use of **external memory** with difficult **memory chip procurement** and potential **obsolescence** of any specific external memory interface
- → It leads to a **very simple stand-alone implementation** with a reduced number of I/Os and to **Standard Surface Mount Package**

CWICOM Performances

- Compression Core Processing performance = 1 pixel per cycle
- ASIC overall performance = almost 1 Mpixel / MHz






CWICOM Architecture
Memories required for the storage of temporary data
NUC Params
Equalized Pixels
DWT Coeffs
Encoded Coeffs
CCSDS Headers
Lines of Pixels
Equalization
Integer/Float 9/7 DWT
Bit Plane Encoder
(bypass)
Input Interface
Controller (Registers)
Source Packet Generator
AMBA Bus
SpW
SPI
Video Input (Pixels)
SpaceWire (Input & Control)
Output Frame (Packets)
Serial Link (Input & Control)
35
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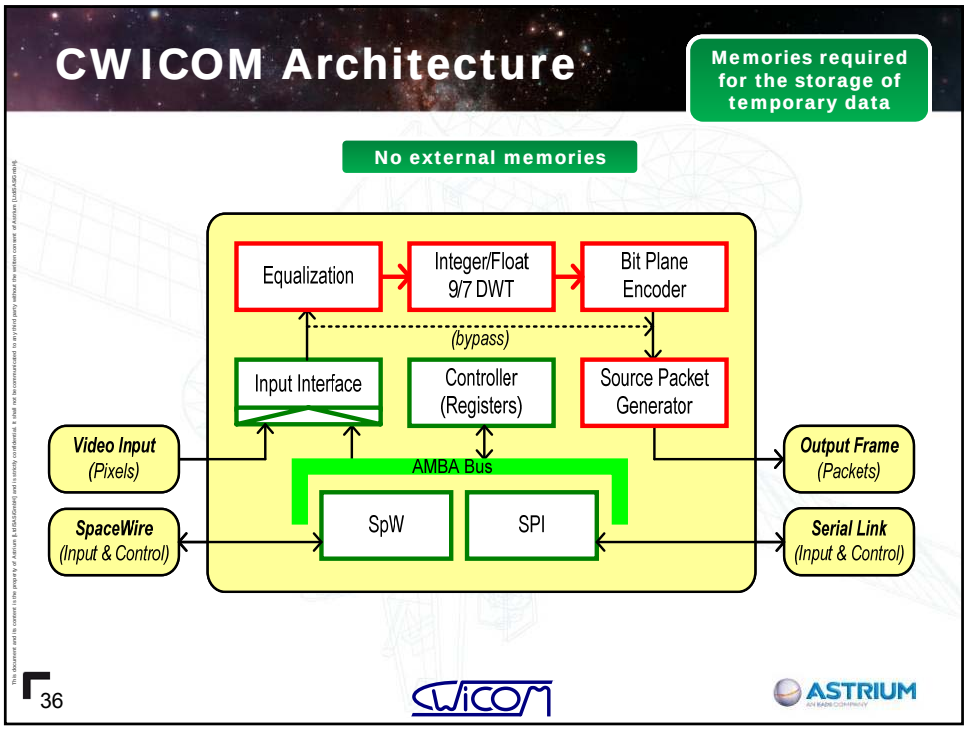
CWICOM Architecture
Memories required for the storage of temporary data
No external memories
Equalization
Integer/Float 9/7 DWT
Bit Plane Encoder
(bypass)
Input Interface
Controller (Registers)
Source Packet Generator
AMBA Bus
SpW
SPI
Video Input (Pixels)
SpaceWire (Input & Control)
Output Frame (Packets)
Serial Link (Input & Control)
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Technology & Packaging

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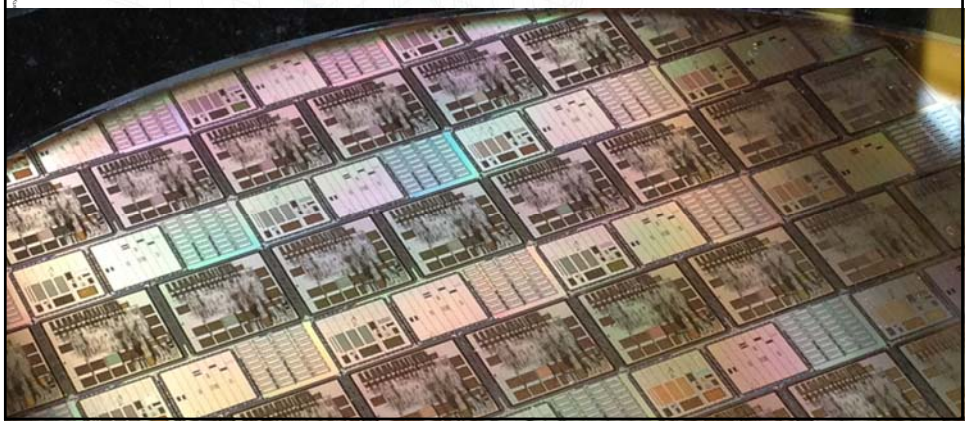
Technology

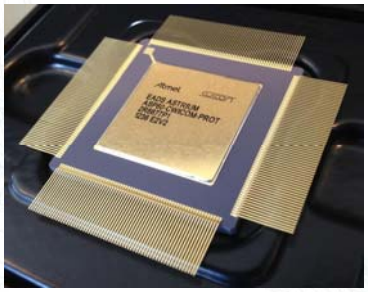
- CWICOM target is the **ATMEL ATC18RHA rad-tolerant technology**
- CWICOM has embarked on the **Multiple Project Wafer** MPW #5
- It will be available in different **quality grades** : QML-Q & QML-V
- Foundry (prototypes) has been done **end 2012**



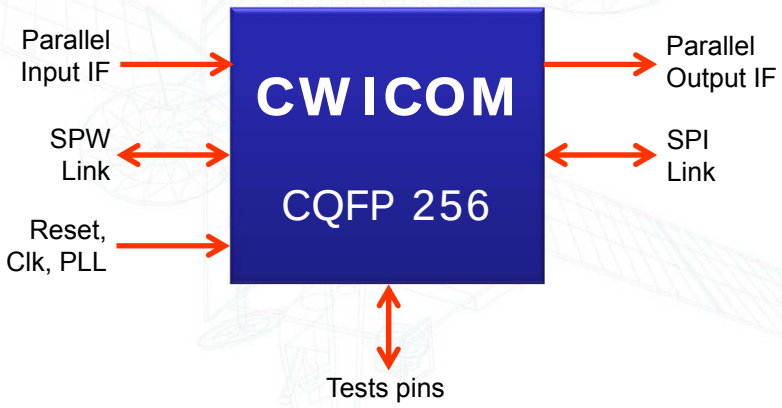
CWICOM Package & Pinout

- CQFP 256
- Standard Surface Mount Package

- Pinout :
  - 76 functional pins
    - Input Interface: 19 pins
    - Output Interface: 19 pins
    - SpaceWire Link: 4 pins
    - SPI Serial Link: 4 pins
    - Clock & Reset: 2 pins
    - IDLE Flag: 1 pin
    - PLL: 9 pins
    - Test: 18 pins
  - 52 power pins
- Total 128 used pins / 256 pins



CWICOM Pinout Topology



Commercialization

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Commercialization

- CWICOM will be available to the European space industry as an **ASSP** (**Application Specific Standard Product**) under fair and equal conditions
- The commercialization plan covers the CWICOM itself in various quality levels, but also related **technical support and documentation**

CWICOM

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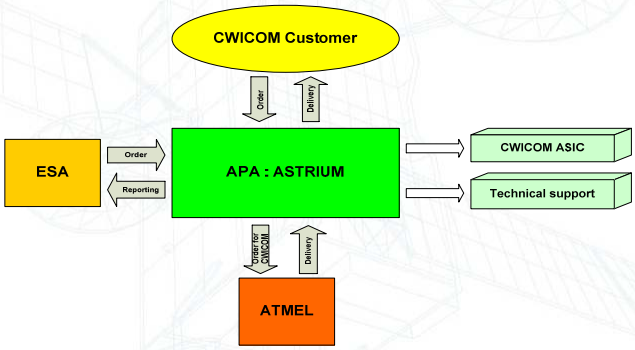
Commercialization

- A comprehensive **framework** has been set up to support the CWICOM commercialization



- CWICOM commercialization is organized by ASTRIUM, acting as the **ASSP Procurement Agency** (APA)

Commercialization

- ASTRIUM SAS proposes a **commercialization scenario** with "Full initial procurement and industrial NRE covered by ASTRIUM"
- In that case, ASTRIUM SAS would propose to any customer an access to the ASIC **with a mitigated MOQ** (Minimum Of Quantity) instead of the MOQ requested by the ASIC manufacturer

Validation

Validation Strategy

- Driver : reach a "**good at first run**" ASIC design

→ CWICOM validation steps:

- **Algorithmic simulations** → to define HW implementation
- **Bit-accurate emulator** in C → SW Reference Model
- **VHDL simulations** in a representative testbench → results compared to the SW Reference Model output
- **HW Prototyping** on a Compressor Board with FPGA
- **Compressor Board** tests with the first ASIC samples

TSD contribution to CWICOM

- TSD has contributed to the ASIC design and developed the Bit-accurate SW model and the CWICOM Validation & Evaluation Platform.
- Contribution to ASIC design:
  - Development of the VHDL Input Interface block of CWICOM
  - Integration of the CWICOM VHDL logic
  - System level simulation

TSD contribution to CWICOM

- The CWICOM Validation & Evaluation platform provides all the data handling and interface resources to prototype the CWICOM RTL code with FPGA and to test the ASIC samples both in a representative H/W environment.

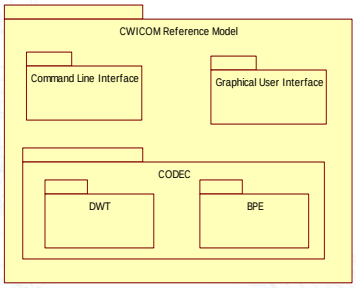
The CWICOM Validation & Evaluation Platform

SW Reference Model Development

- The following activities have been performed
  - Market survey
  - Identification of potential applications
  - Requirement assessment
  - Data compression algorithm analysis
  - Design of the software reference model

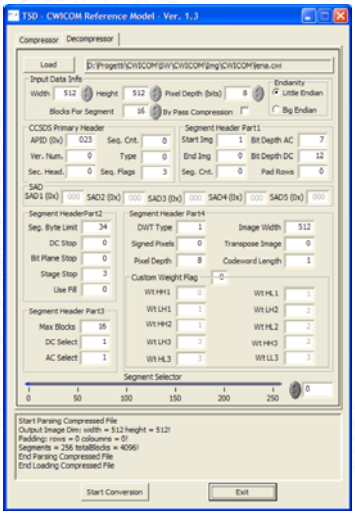
SW Reference Model
A Bit-accurate SW C_Model

- The Reference Model Software consists of three main packages:
  - Command Line Interface
  - Graphical User Interface
  - Codec Package
- The Codec is based on:
  - The Discrete Wavelet (DWT)
  - The Bit Plane Encoder (BPE)



SW Reference Model
A Bit-accurate SW C_Model

- Using the GUI it's possible to select the following parameters:
  - Input image file
  - Width, height, pixel depth
  - Compression factor or bpp
  - Filter type (9/7 integer or float)
  - Code word length
  - Blocks for segment
  - DC Stop
  - Bit Plane Stop
  - Stage Stop
  - Custom Weight
  - Equalization Parameters



SW Reference Model
A Bit-accurate SW C_Model

- The Command Line Interface is able to receive all the parameters, by using 2 xml files:
  - A Configuration File
  - An Input file

CWICOM VHDL Test (TSDev)

The following activities have been performed:

- Development of the Evaluation and Validation platform based on Xilinx FPGA (design, production and assembly)
- Prototyping of the ASIC design with FPGA by the Evaluation and Validation platform; the CWICOM netlist has been mapped in a Virtex-5LX Fpga by Xilinx.
- Validation of the ASIC design

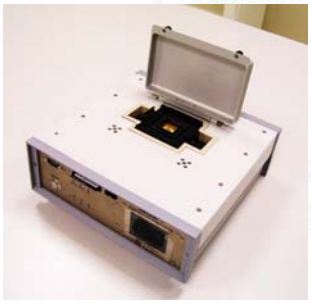
→ All the test procedure foreseen in the validation plan have been run successfully

Evaluation & Validation Board Usage

- How the Evaluation & Validation board could support the activities of CWICOM potential users
- The Evaluation and Validation electronic platform developed by TSDev allows a CWICOM potential user:
  - the evaluation of ASIC functionalities for test & development purpose
  - an easy and economic way for the development of a bread-board which includes a CWICOM equivalent hardware (implemented by Virtex-5 FPGA). The electronic platform could be also customized by TSDev including other interfaces or features.

CWICOM Evaluation Platform

- The CWICOM samples have been validated using the Validation & Evaluation Platform designed by TSD which provides all the interfaces for both:
  - prototyping of the RTL code with FPGA
  - test of all the functions of the ASIC
- It can be used also as a demo platform.



The interfaces include:

- Standard socket to host CWICOM samples
- Camera-Link video input
- Gigabit Ethernet Port
- Compact-flash Card connector
- SpaceWire Interface
- Analog Video Output Interface
- RS232 Ctrl/Cfg and Debug UART line

SW Utilities developed for the Evaluation Platform

- **CWICOM Serial Commander**: to send, via RS232, the configuration command to the CWICOM Evaluation platform
- **PktAssembler**: to receive via Ethernet (UDP protocol) the compressed stream and store it on host PC
- **CWICOM Image Splitter**: to split, decompress and display the stored compressed stream in a sequence of single frame

Verification Test
Stand-alone configuration

Stand-alone configuration (Test Mode Configuration) is meant for RTL code prototyping and ASIC validation according to the verification plan

- The full verification database is pre-loaded on CF card.
- Test data (image data, configuration files, equalization parameters…) are read from CF
- The user send the ID of the Image test to use for validation via UART line using the Serial Commander utility
- The platform configures CWICOM via SPI interface
- The selected image is sent via Parallel Input Interface
- Compressed data are received via Parallel Output Interface
- Compressed stream is checked against reference file
- Test's results are sent via UART line and displayed by Serial Commander utility

The Stand-Alone Configuration

SpaceWire Interface Test

- The CWICOM SpaceWire RMAP interface has been tested by using the TSD Ethernet-to-SpaceWire Bridge.
- The SpaceWire RMAP interface on the Bridge is based on the ESA IP core. This provides an independent tool to validate the CWICOM implementation.

TSD Ethernet-to-Spacewire Bridge

The TSD I/F Bridge is based on a proprietary FPGA based board; it can provide a configurable number and type of communication interfaces (Spacewire, Channel-Link, Camera-Link, GPIO, etc.).

The unit implements a bridge between on-board I/Fs and standard Gigabit Ethernet ports.

Verification Test
Live configuration

Live configuration is meant to evaluate CWICOM performances in a representative scenario

- Images are received from real camera
- Configuration parameters are set via UART line using the Serial Commander utility
- CWICOM is configured via SPI interface
- The images' stream are sent via Parallel Input Interface
- Compressed stream is received via Parallel Output Interface
- Compressed stream is sent via UDP to the Host PC
- Some utilities on the Host PC will be able to store, decompress and display the compressed video stream

Camera characteristics:

- CameraLink base configuration, dual-tap
- Gray-scale Image size of 1600 x 1200
- Pixel dynamics of 10 bit
- Frame rate up to 60 fps (with binning)

The Live Configuration

Verification Test Results

- For both stand alone and live configurations, **all the test procedures specified in the verification plan have been successfully run**
- Moreover, further measures and investigations have been carried out in order to acquire significant electrical and timing data relative to the ASIC itself and to estimate the upper limits of the achievable performances

Further tests & measures
Max SysCLK frequency

A subset of the test procedures have been used for an estimation of the limit frequency of the CWICOM itself. For this purpose, the CWICOM SysCLK frequency has been raised progressively up to the condition for which the ASIC output data packets start to contain errors.

The result has been a limit frequency of **72MHz** (for which all procedures run successfully); above 80MHz, all the procedures run with errors.

The last observation suggest that the errors have been due to sampling limits of the Evaluation platform instead of the CWICOM compression itself. This hypothesis has been confirmed by further investigations.

Further tests & measures
CWICOM Power supplies (1/3)

A subset of the test procedures have been carried out with the purpose to estimate the current absorption relating to the 1.8V Core and 3.3V I/O supplies. The results below show that the Core supply absorption is dominant.

Sys_Clk	Test Procedure	ON current	Peak current
32MHz	083	278 mA	471 mA
55MHz	083	410 mA	652 mA
	038		559 mA
	091		674 mA
	092		678 mA
	046		594 mA
65MHz	083	525 mA	796 mA
	038		708 mA
	091		845 mA
	092		818 mA
	046		739 mA
72MHz	083	580 mA	870 mA
	038		781 mA
	091		927 mA
	092		914 mA
	046		803 mA
80 MHz	091	650 mA	1007 mA
	083		935 mA

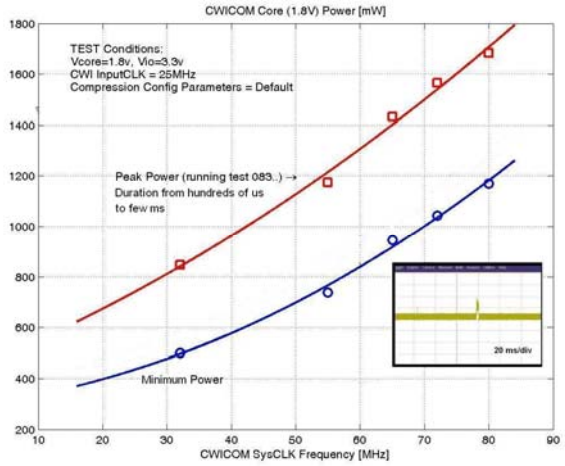
Measures on CWICOM 1.8V Core

Sys_CLK	Test Procedure	ON current	Peak current
55MHz	083	35 mA	110 mA
	038		115 mA
	091		115 mA
	092		75 mA
	046		115 mA
65MHz	083		128 mA
	038		124 mA
	091		124 mA
	092		75 mA
	046		128 mA
72MHz	083		128 mA
	038		133 mA
	091		137 mA
	092		75 mA
	046		133 mA

Measures on CWICOM 3.3V I/O

Further tests & measures
CWICOM Power supplies (2/3)

These measurements at 25C with some images shall be improved by additional tests to establish the real power consumption performance of the CWICOM



Further tests & measures
CWICOM Power supplies (3/3)

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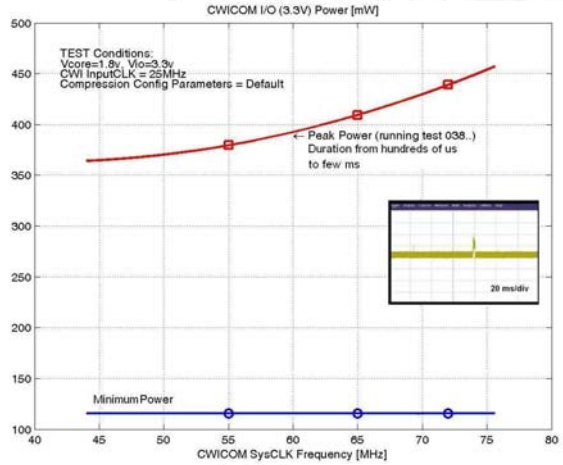

Hardware Demonstration

TSD Space

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CWICOM Live Demo (1/5)

A live demonstration using the ASIC will be carried out in ESTEC by the Validation & Evaluation Platform and the test setup showed in the figure which includes also the developed SW utilities which permit the control of the test.

TSD Space

CWICOM

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CWICOM Live Demo (2/5)

- In the live test configuration the FPGAs of the validation platform are programmed to grab images coming from the camera and to move these to CWICOM via the Parallel Input Interface.
- After power up, using the Serial Commander software, the user must specify the test configuration (that is, type of transform to use, if equalization is to be applied, the number of byte per segment etc.). All these parameters are sent via RS232 serial line to the Evaluation Platform which configures CWICOM via the SPI interface.
- The compressed data are sent back to the Host Computer via the Ethernet connection using the UDP protocol. Using the Packet Assembler software, it is possible to collect all the UDP packet and save it on the host PC.
- The saved file then is given in input to the Image Splitter software that reconstructs, decompresses and displays all the images included in the file.

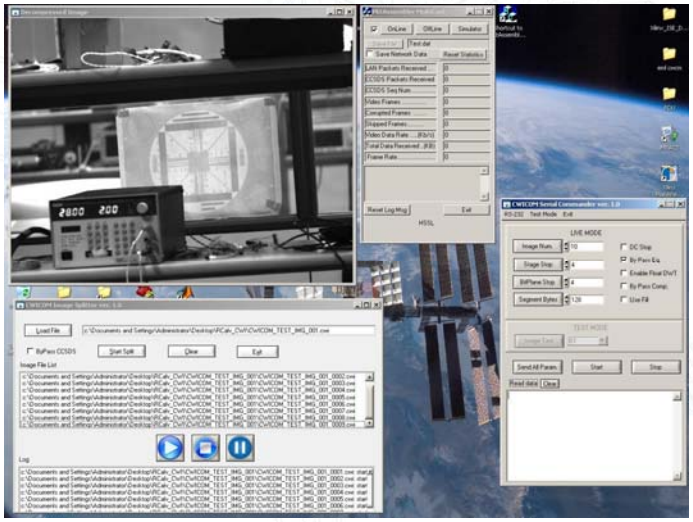
CWICOM Live Demo (3/5)

A typical test sequence consists of the actions listed below:

- Power-on of the CWICOM Evaluation & Validation Platform
- launch and configure the Packet_Assembler software (set the name and directory of the output file .CWI and other options); “arming” of the SW for waiting for incoming compressed video frames; the software must be placed in the “On Line” state pushing the “On line” button
- launch the Serial Commander SW, configure the parameters to send to CWICOM and start the execution of the operations
- wait for completion of the compression (the Packet_Assembler receives the compressed frames via Ethernet); at the end of the process (the state can be seen by the output of CWICOM on the UART interface) the Packet_Assembler must be stopped pushing the Off-Line button
- launch the Image_Splitter and select the .CWI file saved by the Packet_Assembler, then start the split process
- double click on a single image in the image file list to decompress and visualize the related image
- push the “Play” button, to start the decompression and visualization process.

CWICOM Live Demo (4/5)

The SW windows which permit the control of the Evaluation platform



CWICOM Live Demo (5/5)

Live demonstration of **CWICOM ASIC performing image compression**

- in **Stand-alone mode**, based on pre-defined CCSDS test images
- in **Live mode**, based on real time image capture from a digital camera

Conclusion

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CWICOM Key Features Summary

▪ High data rate	**60 Mpixels/s**
▪ Pixels dynamic	up to **16 bits**
▪ Image width	width up to **3496 columns**
▪ Image height	**unlimited** in push-broom
▪ Op frequency	~60 MHz
▪ Compression	0.5 bpp to 10 bpp
▪ Memory gates	~5 Mbits
▪ Logical gates	~1 Mgates
▪ Packaging	**CQFP 256**
▪ Size	37 x 37 x 3 mm
▪ Mass	~ 20 g
▪ Radiation	300 Krad total dose
▪ Power	~25 mW per Mpix/s (TBC)

CWICOM

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Conclusion

Status

- First foundry has been launched : ASIC prototypes have been **successfully validated** on a dedicated Compressor Board
- CWICOM results from a **fruitful ESA, Astrium & TSDEV** collaboration

Next step

- Consolidation with ESA of **Commercialization Plan** framework (MOQ, price, support…) in order to propose the CWICOM as an ASSP

Conclusion

Summary

- The **CWICOM ASIC** is a high performance image compression ASIC
- Fully compliant with the CCSDS image compression standard
- High data rate performance of 60 Mpix/s
- Radiation hardened
- Low power consumption
- Provided in a CQFP256 package easy to mount for SME
- No need for any additional external memory
- Easy to use, with possibility of control through SpW or SPI link
- The **CWICOM ASIC** has been developed to fulfill the needs of space applications more and more demanding in terms of image compression performances and integration constraints

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