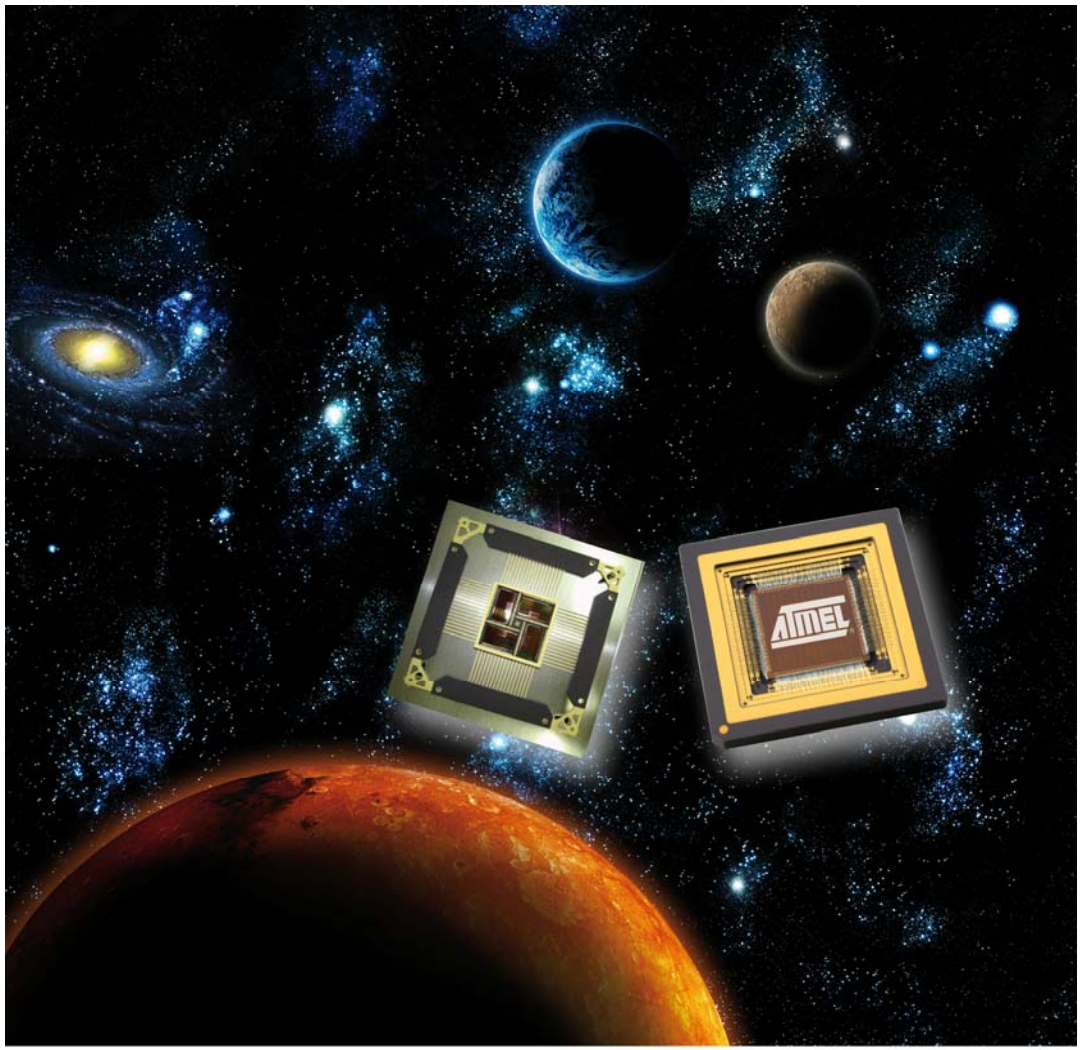
AT697F
SPARC V8



Final Presentation Day
ESTEC

April 25th, 2012

AGENDA

1. Why AT697
2. AT697E “Engineering Model”
3. AT697F
    1. Specification
    2. Design
    3. Characterisation
    4. Radiation test
    5. Application test
4. SPARC biz
5. Next Steps

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Sparc 32-bit Architecture

- Start in 1994
- SUN Microsystem agreement
- 3 Chips: 691 – 692 – 693
- 1 Chip TSC695
- Worlwide adoption of SPARC architecture for Space

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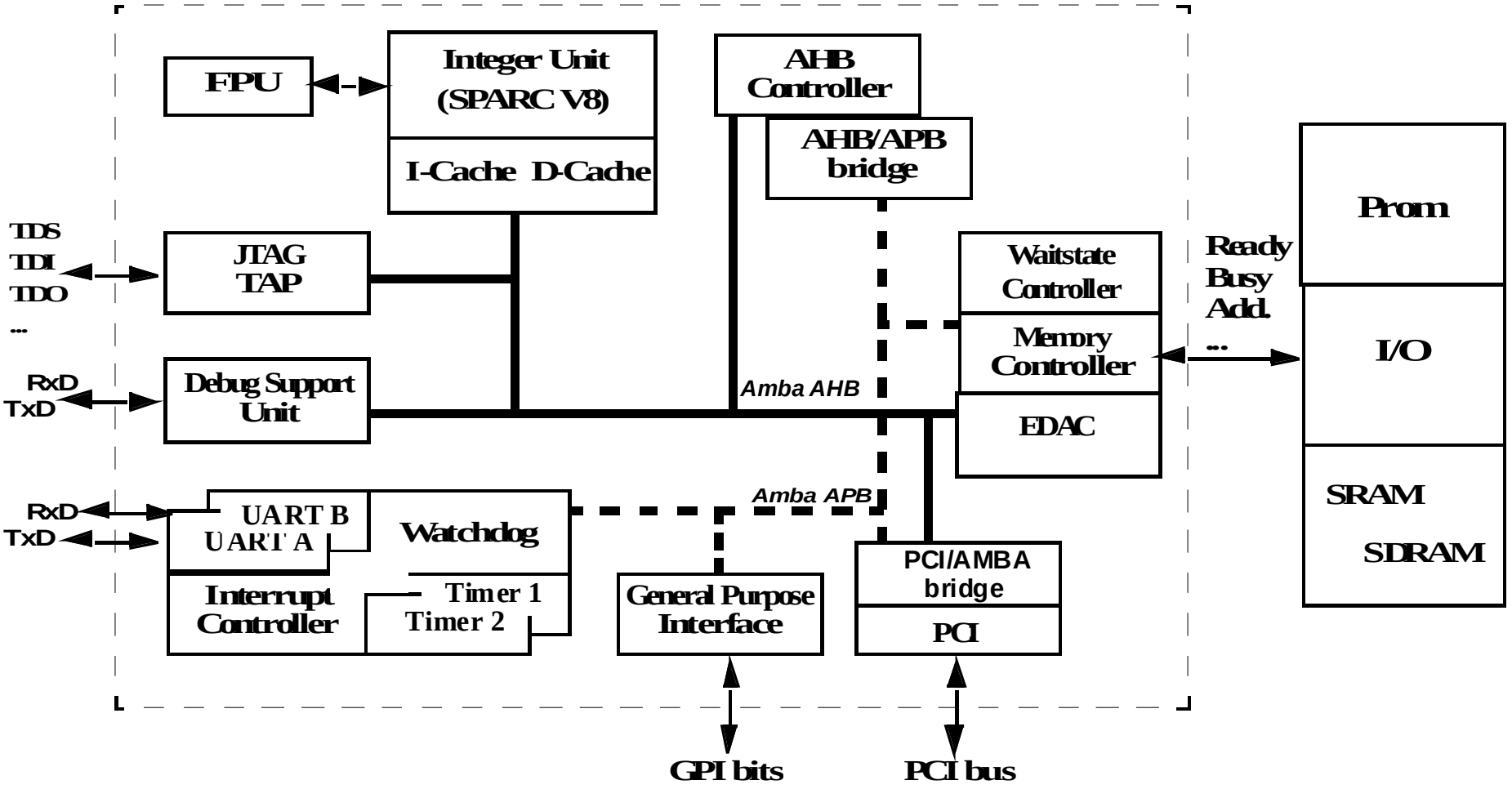
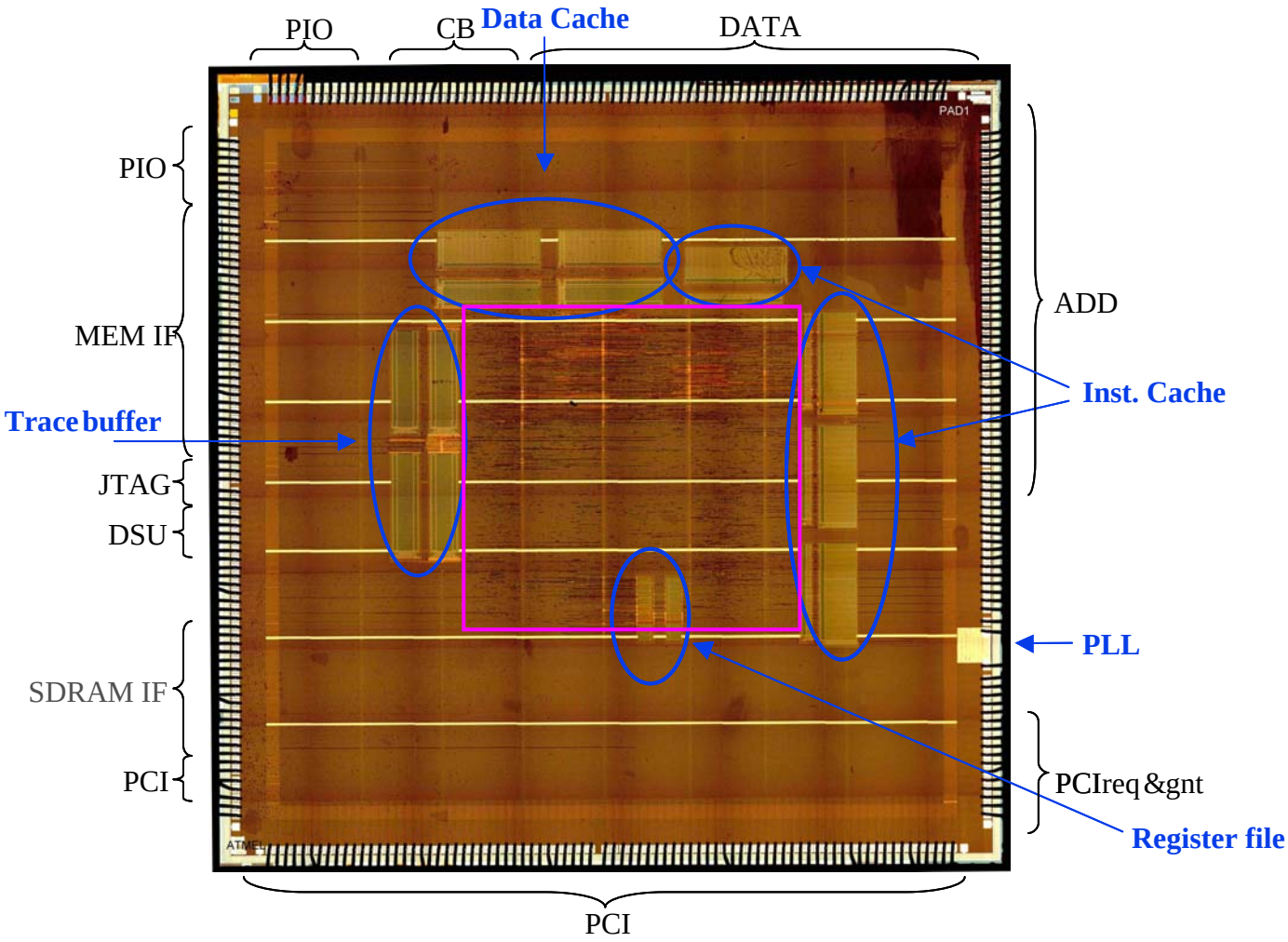
AT697 Sparc V8 32-bit Architecture

- SPARC V8 LEON2 with Integer and Floating Point Unit
- On chip Amba Bus
- Embedded Instruction and Data caches
  - 16Kbytes multi-sets Data cache
  - 32Kbytes multi-sets Instruction Cache
- Memories Interface for PROM, SRAM and SDRAM
- PCI 2.2 interface (33 MHz)
- Two Timers, two 8-bit UARTs and Interrupt Controller
- User friendly Debug Support Unit
  - Trace buffer 512 lines of 16 bytes

AT697 block diagram



AT697 Die View



AT697E performance

- Performance at 100MHz
  - 86 MIPS (Dhrystone 2.1)
  - 23 MFLOPs (Whetstone)
  - SDRAM interface speed impacted by the bus load
    - On AT697-EVAB (2 SRAM and 1 SDRAM banks) : 65 MHz maximum
- Power consumption

150 MIPs/W

  - 7 mW / MHz
    - At 100 MHz and for high activity : core at 0.5 W, I/O at 0.2 W

AT697E radiation performance

- Total Ionizing Dose
  - Parts fully functional at 200 krad (Si)
  - 3.3V I/O standby current increases after 100 krad (Si), and recovers after high temperature annealing
  - These results allow to use these AT697E parts for space mission requiring a maximum of 60 krad (Si)

- Single Event Effects
  - No Single Event Latchup (SEL) at 95 MeV/mg/cm2 – max voltage – 125°C for a fluence of 1 E7 particles/cm2
  - Very good Single Event Upset/Transient (SEU/SET) protection

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AT697F rationales

- Prototype devices: AT697E and Flight devices: AT697F
- ATC18RHA library
  - To allow successful total dose test up to 300 krad (Si)
  - To ensure appropriate process reliability monitoring (through SEC test vehicle)
- Bug removal
  - All known bugs has been corrected (see AT697E errata sheet)
- Removal of existing functions
  - 16-bit mode PROM/RAM interface (no EDAC support)
  - PCI single transaction mode
- Addition of new functions
  - Addition of Two Memory Block Protection Units (TSC695F compatible)
- Pin out compatible with AT697E

AT697F improvements of existing functions

- Many feedbacks from customers during AT697E validation phase and first designs
- Improvements
  - Asynchronous assertion of BRDYN
  - Use of the BRDYN for PROM area
  - Extending the timers to 32-bits
  - Addition of four external interrupts
  - AHB trace buffer halt
  - New 8-bit memory EDAC scheme
  - Write to 8-bit PROM with EDAC enabled
  - PCI device configuration boot pin made readable
  - PCI configuration registers made AHB readable in satellite mode
  - Higher capacitive load capability.
  - Higher ESD protection 2000V (250V for AT697E)
- SDRAM interface speed

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Design Considerations

- ATC18RHA CMOS 0.18 micron; 1.8 V core; 3.3V I/Os
- Fault tolerance by design
  - Triple Modular Redundancy with skew
    - SEU and SET protection
  - EDAC on register file and external memories
  - Parity on the caches
- Available package
  - MCGA 349 (extended last delivery Q2_2013)
  - LGA 349
  - MQFPF 256
- First Silicon is Last silicon

Design Considerations

- *Difficulties*
  - *A fight against the natural TMR dissolution*
    - *Set don't touch all along the flow*
    - *Each TMR is a sublock, as a consequence*
    - *It slows down drastically the netlist loading before simulation*
  - *"Hold correction step" leads to*
    - *Component number inflation (up to 50%)*
    - *A trade off between clock skew value and hold delay buffers*
  - *SDRAM painful Read/Write optimisation/adjustment*
    - *Dedicated clock tree for SDRAM interface*
  - *NTL simulations : Stuck at initialisation*
    - *Due to DFFs "X" propagation*
    - *The Work around was to patch the simulation DFF models*

Simulations and STA Considerations

- *Logical Simulations done*
  - *At corner : Typical, Worst and Best (skew 00,01,10)*
    - *tbfunc32(50Mhz,95Mhz-sk00),tbfunc8(50Mhz),tbfuncsd(50Mhz),*
    - *tbmsp(50Mhz),tbpci(10Mhz)*
    - *tbBist,tbJtag,tbscan*
    - *PLL(80Mz,100Mhz,120Mhz)*
- *Static Timing analysis*
  - *Max frequency*
    - *95MHZ (skew 00 corner slow)*
    - *92MHZ (skew 01 corner slow)*
    - *87MHZ (skew 10 corner slow)*

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3.1 Functional Tests

- TBFULL (Natural, Medium and Max skews)
- PCIMASTER (Natural, Medium and Max skews)
- PCISLAVE (Natural, Medium and Max skews)
- USPARC (Natural, Medium and Max skews)
- SRAM
  - 50MHz ,83MHz and 100MHz (Natural skew)
  - 20MHz (Natural , Medium and Max skew)
- APPLAB 10MHz (Natural , Medium and Max skew)
- APPLAB 10MHz , CLK shift (Natural , Medium and Max skew)
- TBFUNCSD (Natural , Medium and Max skew)
- DSU (Natural , Medium and Max skew)
- DFT : JTAG , BIST , SCAN , FULLATPG , TDF
- PLL

3.2 AC/DC tests

- Dynamic Current consumption
- PLL Current consumption
- Standby Array and buffer Current consumption
- Input Leakages
- Cold Sparing Input Leakages
- High Impedance State Output Current
- Output currents
- Dynamic parameters :
  - LEON processor timings
    - 26 timing (Min/ Max) values measured at skew natural & max
  - PCI interface
    - Functionality @33MHz
    - Test in Master & Slave Mode
    - 32 timings (Min/ Max) values measured at skew natural & max

3.3 Solved issues

- Additional test benches had to be developed to test :
  - Debugger System Unit
  - Transient Delay Fault
  - SCAN , BIST , JTAG
  - PLL
  - SRAM interface (timings characterization)

- MQFP256 PCI interface : ground bounce issue on PCI signals , during data preload
  - Not confirmed on application board

- T14 Data & CB bus tri-state transition delay
  - STA exhibits out of spec values in typical case (data switches to Z before active control signal)
  - L-H to Z state transition characterized using different test environments
  - Not seen on application board

3.4 Results / Critical parameters / Conclusion

- Results
  - Characterization has been performed on one typical silicon lot
  - Timings results fully match with STA data
  - Parametrical results are on line with ATC18RHA libraries specification

- Critical parameters
  - Main clock Domain frequency :
    - 100MHz at limits in worst case conditions (Process Slow , Vcc Min, hot temperature)
    - Test program will screen out of specification parts

- Conclusion
  - According characterization results and final specification , the AT697F test program has been released to production
  - Supply chain is on line with the demand (test and burn-in capacities)

3.5 ESCC Evaluation

- **TEST PERFORMED :**
  - ESD : CDM & HBM model
  - Electrical Latchup
  - Breakdown voltage
  - Electrical characterization
  - Construction analysis
  - SEM inspection
    - microsectionning with glassivation layer integrity
  - Bond strength and substrate attach strength (stud pull test)
  - Thermal test : group D3
  - Mechanical Test : group D4
  - Endurance Test : 3000H/150°C (HTOL)
- **QUALIFICATION STATUS:**
  - Derived from this technology, AT697F passed successfully all qualification requirements. AT697F has been qualified in November 2011

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Radiation Considerations

- *AT697F Single Event Effects Testing*

- iRoC “smartly” managed a tester designed by TIMA:

  - 1 run = n iterations (Boot , write, wait, dump, capture)

  - Static tests: memory elements are exhaustively SEU tested (Registers, Caches, DFF), protected or not.

  - Dynamic tests: the result of computation (subject to SEUs in memory elements and SET in the logical elements) with or without mitigation schemes are assessed.

  - The set of functional patterns were enhanced to check the occurrence of SEFIs : aocs, sort, math_sw, math_hw, pci_i_w, pci_i_r, pci_t_w, pci_t_r, alu.

Radiation Considerations

- *AT697F Single Event Effects Testing*
  - *SEL : No latchup found at 62MeV.cm²/mg, VCCmax, 125°C Fluence= 2.0E07 part/cm²*
    - *→ LU Cross section < 5E-8cm²*
  - *SEU: Every RHBD technique EDAC, parity, TMR was tested and showed its efficiency. Only few MBU at high LET may interest the user.*
  - *The SEU low sensitivity is enhanced with good practises like cache occupancy management.*
  - *No functional disruption found.*
  - *SET : The TMR technique allows a very good filtering of the SETs in the combinational logic network.*
  - *Proton : Very low sensitivity to 63MeV*

Radiation Considerations

- *AT697F TID tests :*
  - *The first evaluation was done over the lot 8S5247P with 10 parts and worst case conditions:*
    - *Gamma source exposure with Atmel VLSI Testing read outs*
    - *VCC max , static biased , Co 60 low dose rate irradiation , 0 to 300krads[Si] + amb. anneal + 100°C anneal*
    - ➢ *No variation can be found. (functional , parametrical)*
  - *As expected the lot 8S5250-1GA (22#) passed a QML-RHA capability level of 100krads (R) (tested after 100,200,300krads and annealing sequences)*
  - *This confirms the total ionizing dose radiation hardness shown on the ATC18RHA technology.*

Radiation Considerations

- *Conclusion*

- *The exhaustive radiation testing showed:*

- *A good TID hardness at the level of interest of 300krads*

- *A good SEL immunity above 60MeV.cm²/mg (high temp.)*

- *A good efficiency of the RHBD mechanism against SEU/SET that can be emphasized with advised software practices*

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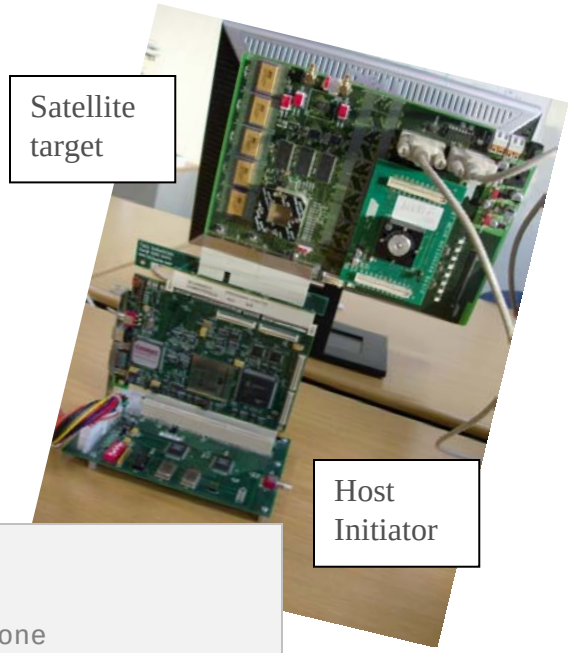
Application – AT697 Validation Test Summary

Performance Testing

- Integer Unit Performance assessment
- Floating Point Unit Performance assessment
- Memory interfaces performances

Functional Testing

- Caches subsystem
- Interrupt Controller
- Memory controller
- Timers
- UARTs
- General Purpose Interface
- Data protection
- PCI Interface (Initiator/Target)



3 different test benches :

- AT697F Evaluation Board standalone
- AT697F Evaluation Board + PCI Analyzer
- 2x AT697F Evaluation Board communicating through PCI (Host / Satellite testing)

Performance Summary

- 7mW/MHz
- 86MIPS (Dhrystone)
- 23MFLOPS (Whetstone)

Functional Validation Summary

- BUG1 : Odd-numbered FPU register dependency (known since tape-out)
- No new bug found by validation

AT697F – Market Introduction Package

Documentation

- AT697F Datasheet
- AT697F Erratasheet
- AT697F Performance Summary
- AT697x Evaluation Board User-Guide
- AT697F Radiation Summary

Hardware

- AT697F Evaluation Board
  - MQFP256 package
  - MCGA349 package

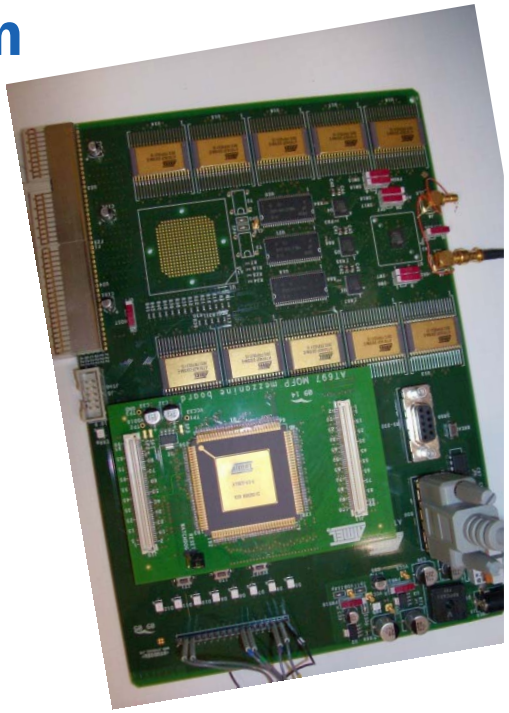
Software

Application – HW Development Platform

Hardware

AT697F Compact PCI Evaluation Board

- Support for Atmel AT697E/F , Rad-Hard 32 bit Sparc V8 Embedded Processor
  - Mezzanine board for MCGA package
  - Mezzanine board for MQFP package
- Memories/Peripherals
  - FLASH 2Mbyte
  - SRAM 4Mbyte made of 2x AT60142 SRAM banks
  - SDRAM 64Mbyte
  - Memory/Peripheral expansion connectors
- PCI support
  - 6U format, 32 bit, 33MHz interface
  - Configurable for System and Peripheral slot operation
- Debug Support Unit interface
- PIO expansion
- On-board power regulation allows operation from PCI slot, or stand-alone with +5V



Key Features

- Support MCGA349 and QFP256 packages
- System based on Rad-Hard memories

Application – Software Development Platform

Existing Software Tools

- Compiler
  - •Bare-C Cross-compiler
  - •RTEMS Cross-compiler

- Debugger
  - • GRMON debug monitor
    target debug through serial DSU or PCI interface
  - • Vision debugger

- Simulator/Emulator
  - • TSIM simulator
  - • LEON probe emulator

- •Real Time Operating Systems
  - • RTEMS
  - • VxWorks
  - • eCOS
  - • Snapgear Embedded Linux (uClinux)

AEROFLEX GAISLER

http://www.gaisler.com/cms/

http://www.visionmc.com/english/html/indexEng.htm

Application – Development Platform

Coming Software Tools

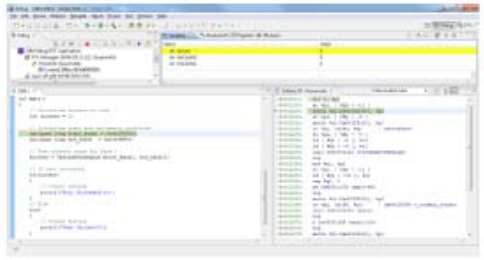
ATMEL proposing a comprehensive, fully integrated set of software development tools developped by Stardundee.

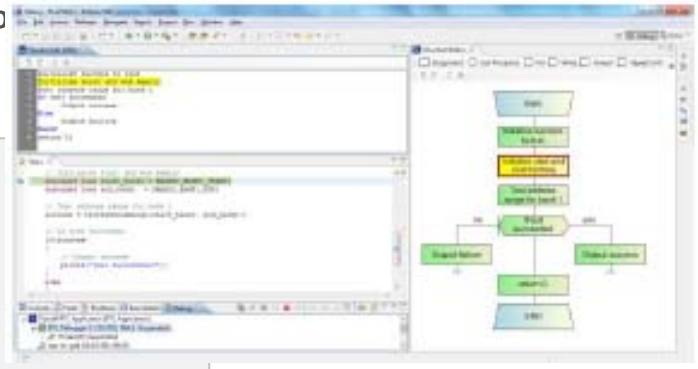
http://www.star-dundee.com/products

This SDE (Software Development Environment) includes the following services :

- **Compiler**
  - **GNU Compiler Collection fully integrated tool chain**
- **Debugger**
  - **Eclipse IDE widely adopted Integrated Development Environment**
  - **Plugins for Eclipse IDE for seamless access to peripherals & componen**
  - **Hardware interface module to manage communication w Eclipse IDE**
- **Monitor**
  - **Code Rocket**

    => abstract pictorial and descriptive input too





Key Values

- **Support all AT697x based processor**
- **Fully European Alternative**
- **Starting point for ATMEL next generation processors**

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ATMEL SPARC V7 / V8 Flight Heritage

- Unique Flight Heritage
  - SPARC V7 TSC695
    - More than 3100 flight models already delivered, since 2003
  - SPARC V8 AT697 (100MHz) starting stronger than TSC695 from the end of 2010
    - AT697E 220 FM delivered reaching 290 by the end of 2012
    - AT697F 100 FM delivered reaching 600 by the end of 2012
  - Preparing the future with a 200MHz Processors with more peripherals and DDR memory interface

- Atmel Processors SPARC V7 and V8 are used worldwide

COMMENTS

- Lowlight
  - First silicon working but too long validation time
  - Not enough ATMEL proposals on spec improvements (MMU, FPU …)
  - Lack of control on the developments tools
  - Lack of ATMEL simulation model for end-user

- Highlight
  - First silicon full spec
  - Very fast market start
  - AT697F is accepted worldwide

- **Both AT697E and AT697F joined ESA – CNES – ATMEL developments are a success**

- **Thank to André Pouponnot, Roland Weygand and David Dangla**

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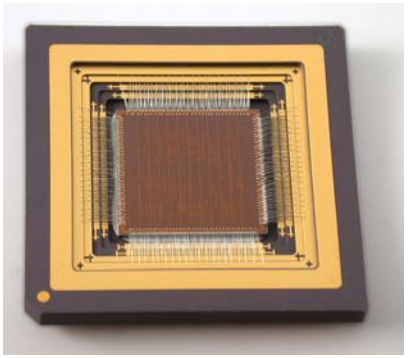
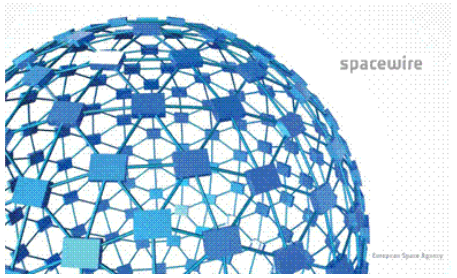
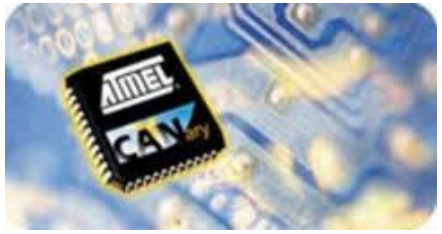
AT7913 Spacewire Remote Terminal Controler

- SPARC V8 Processor - LEON2-FT 50Mhz
  - 4Kinstruction cache, 4K data cache
- Package CQPFP 352 or MCGA 349
- Highly integrated peripherals
  - Digital ADC/DAC
  - Redundant CAN 2.0 with DMA
  - FIFO interface with DMA
- Spacewire
  - 2 links with RMAP
  - LVDS
  - Up to 200Mbit/s data rate
- Onchip Memory 64KBytes EDAC protected
- Radiation
  - Tested up to 300Krad
  - No single event latchup below LET 80 MeV/mg/cm2
- Operating range
  - 3.3V +/- 0.30V for I/O
  - 1.8V +/- 0.15V for Core
  - -55°C to 125°C
- QML-Q, QML-V and RHA grade

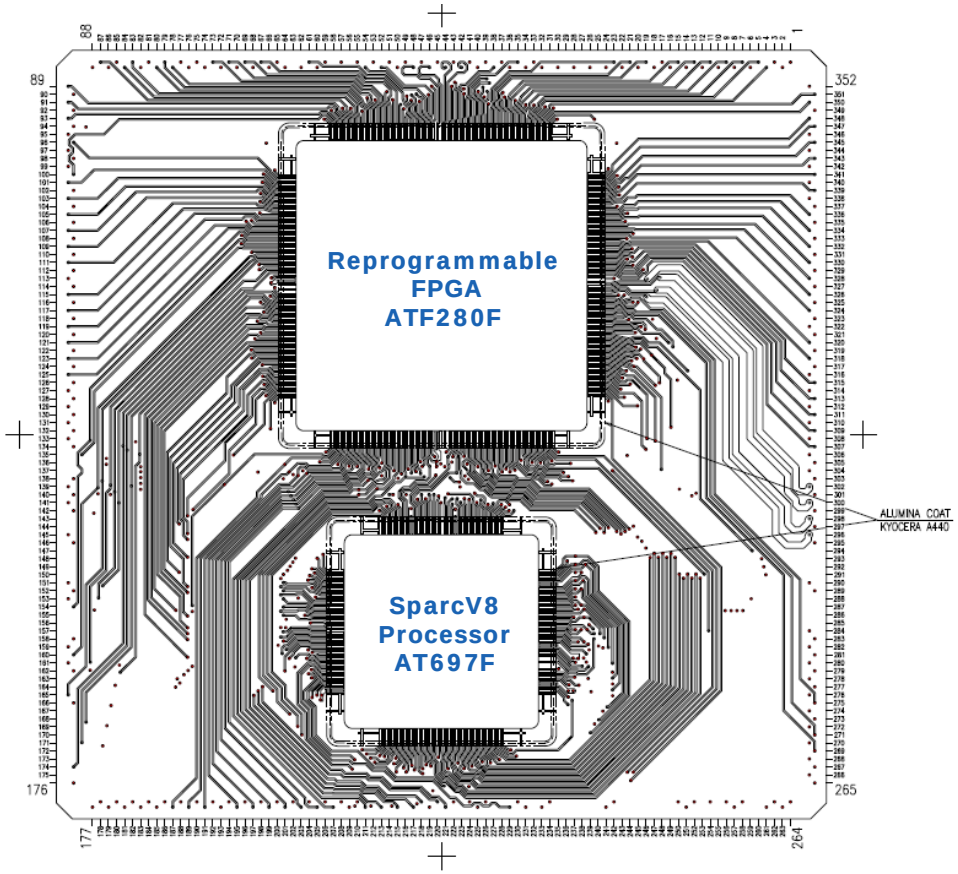






ATF697FF Reconfigurable Processor

- Combined **Rad Hard Processor + FPGA**
  - **SPARC V8 Processor**
    - AT697F LEON2-FT 100Mhz
    - Powerful & Low Power
  - **Reconfigurable unit**
    - ATF280F SRAM based FPGA (280K)
    - Mapped on SPARC Memory Bus
    - Internal PCI link
- Multi-Chip Package CQPFP 352
- Ready for Spacewire
  - 4 LVDS tranceivers & receivers
- Radiation
  - AT697F and ATF280 Legacy
- Operating range
  - 3.3V +/- 0.30V for I/O
  - 1.8V +/- 0.15V for Core
  - -55°C to 125°C
- QML-Q, QML-V and RHA grade

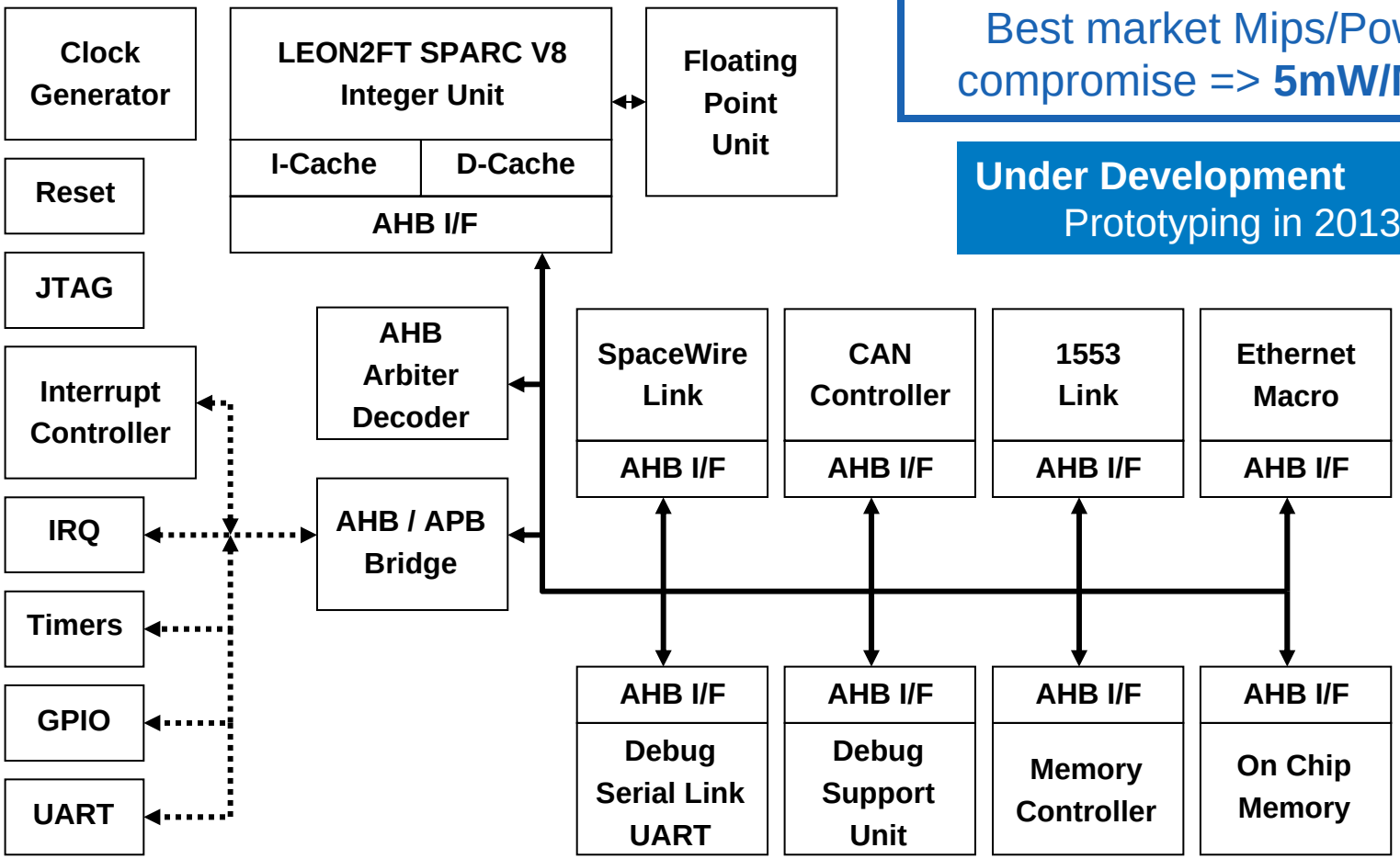


CASTOR – Specifications SPARC V8 200MHz

200Mhz / 1W

Best market Mips/Power compromise => **5mW/Mips**

Under Development
Prototyping in 2013



THANK YOU