ESA MICROPROCESSOR DEVELOPMENT

STATUS AND ROADMAP

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1 ABSTRACT

The objective of this paper is to present the status of ongoing and upcoming microprocessor development activities supported by ESA. The following topics will be addressed:

- Microcontroller Developments
- LEON2-FT microprocessors [AT697E], [AT697F] and [AT7913E]
- LEON3-FT based Spacecraft Controller On-a Chip [SCOC3]
- LEON4-FT based Next Generation Microprocessor [NGMP]
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This paper does not address the needs of Payload Data Processors in the high performance range, which will be the objective of a dedicated contribution to this conference. This paper also does not take into account microprocessors which might be available from other sources, without ESA involvement.

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2 MICROCONTROLLER DEVELOPMENTS

As emphasised in [UC-WIKI], a microcontroller is a small, single-chip computer, and an important objective is to limit the overall cost of embedded systems. This comprises the cost for components, boards, assembly, but also SW development. Power consumption, mass and single-event tolerance are furthermore important requirements in space systems, and often, for real-time applications, predictability is more important than average processing power. Space qualification, in spite of the pressure on components price, can not be waived, yet the required level/flow is still unclear.

Existing components, such as the Atmel 80C32E or the 80S32 developed by ADV/Transwitch in 0.8/0.5 mm technology will soon be obsolete, and their 8-bit architecture and the limited set of peripherals also leave room for improvements. A new space microcontroller needs to be developed. Key requirements are the monolithic integration of digital/mixed-signal peripherals and on-chip memory, an easy-to-assemble low pin-count package and a well-established CPU architecture for which SW development tools are readily available. Space microcontrollers have been discussed during the [MESA] Roundtable.

Pending the availability of a new dedicated space microcontroller, to be developed as an ESA Supported Standard Product [ESSP], the use of COTS components is also being investigated. Single-event test results for two ATMega parts were presented at [MESA]. As an alternative, existing ([LEON2FT]-based) space microprocessors like the [AT7913E] could also be used at low clock frequencies with moderate power consumption. Their high pin count, high sales price and the number/complexity of external components required present however a drawback contradicting the above mentioned cost constraints.

To address some of the drawbacks of [LEON2FT] for its use as microcontroller, a modified version [V8uC] is currently under development by Sitael. It is noted as well in this context, that as of January 2011, the restrictions to use [LEON2FT] only in certain target ASIC/FPGA technologies are not applicable any more.

Key challenge for a new microcontroller will be to identify a suitable silicon technology which allows embedding digital logic, memories as well as mixed-signal peripherals and possibly non-volatile memory. Existing offers for space ASICs either do not support analog design (e.g. Atmel, where analog design kits are not available), or digital design libraries are not existing (e.g. LFOUNDRY, XFAB) or not suitable for large, low power designs (e.g. DARE). A possible solution could be the 180 nm process from TowerJazz (Israel), for which a rad-hard library exists from RamonChips. Commercial access to this solution and possible issues with Israel's export regulations must however be clarified.

For the choice of the CPU architecture, several IP candidates are under consideration, for example LEON2/3FT, AVR, XAP, ARM, PIC or open source IPs such as the OpenMSP430 or the OpenRISC1200 are under consideration. Several aspects should be considered, such as the IP and SW tool availability/cost, expandability (peripheral bus), maturity, SEU hardening. Code density is also an important factor, in particular with the goal to host the application entirely in embedded memory, such that no external memory is required. Research papers, such as [CDENS] show that the code density largely depends on the application and on the code and compiler optimisation. Nevertheless, it seems that lower code size is obtained, if the width of the processor data and address path matches the application requirements. A comparison made in a

frame of [DCPM], compiling 16-bit applications on LEON2 (32-bit), XAP4, OpenMSP430 (both 16-bit) and 8051 (8-bit), also showed that the 16-bit processors yield in lowest code size. These investigations should be expanded, covering a more representative spectrum of space applications and all the candidate IP cores.

Tight budget constraints, for development as well as for the components sales price, also requires to rely on IP cores which are available at limited fee/royalties, such as the [ESA-IP] or open source IP. Full visibility of the HDL source code to ESA is furthermore necessary to ease support of future ESA projects using this part. From this point of view, the use of LEON2FT, or its derivative V8uC, or an open source IP such as the OpenMSP430 seems very attractive. But commercial IPs such as AVR, XAP or LEON3FT can be a solution, provided an agreement can be reached with the suppliers on cost, licensing and source code availability, a license fee is often also compensated by professional support.

In favour of LEON2/3 is certainly that both processors are already heavily used in the European space community. Unfortunately, SPARC and the classical ARM 32-bit instruction sets are not optimal in terms of code density. As an outcome, similar to the approach of the reduced ARM-Thumb instruction set, the development of an optimised SPARC variant could be undertaken. Efforts for re-design of the existing IPs and of the SW tools (compiler) are to be evaluated.

3 LEON2-FT MICROPROCESSORS [AT697E], [AT697F] AND [AT7913E]

[AT7913E] has been established as standard product on Atmel catalog. An SEU test campaign is planned throughout 2011. First missions to use this component are BepiColombo and SolarOrbiter.

The [AT697E] development is completed. For [AT697F], in complement to the presentations at [MPD2010] and [MESA], the following status is reported:

- Electrical characterisation confirms the timings from the preliminary data sheet
- TID and SEL tolerance are in-line with the ATC18RHA technology. Two heavy-ion and one proton SEU test campaigns have

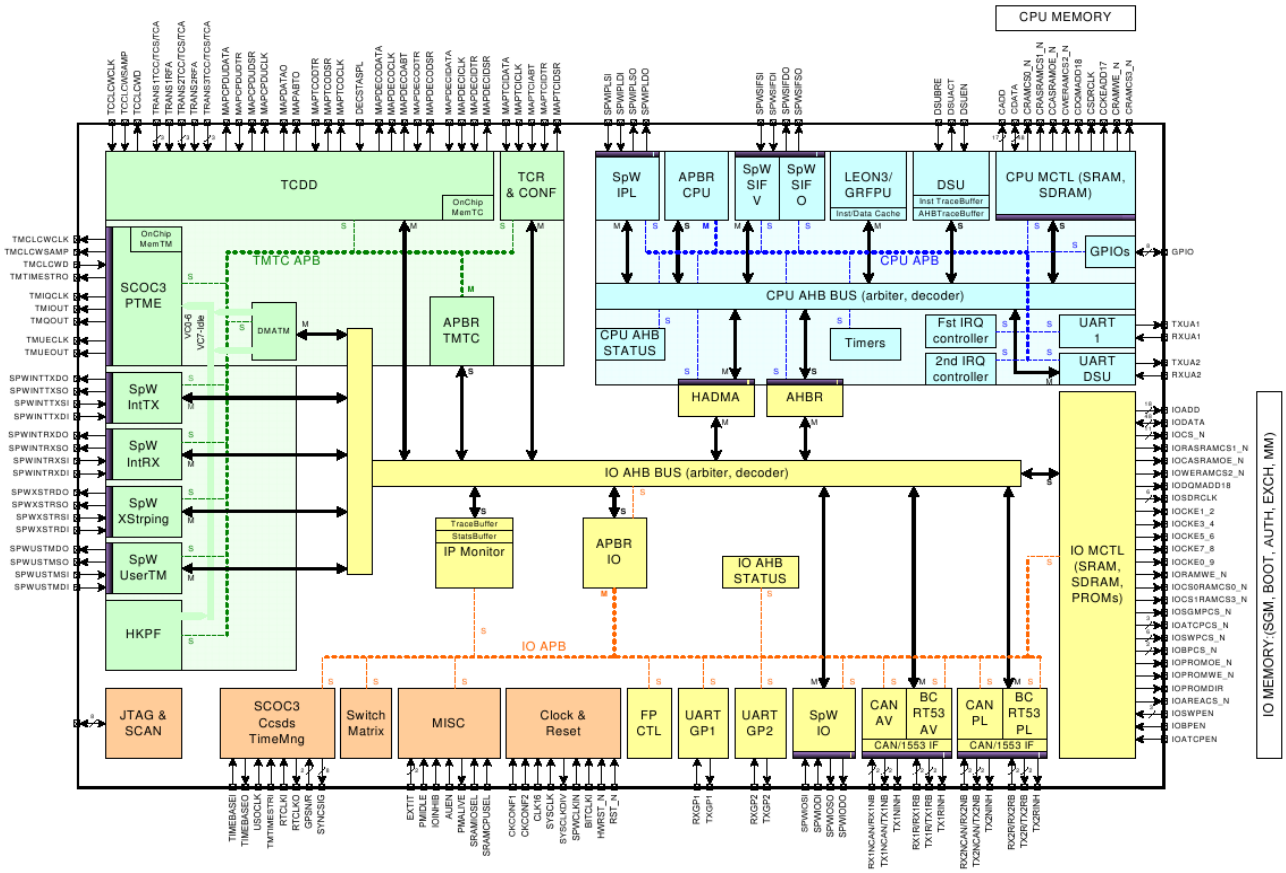

Figure 1: SCOC3 Block Diagram

confirmed the robustness of the device in terms of single-event-effects. The SEU cross-sections obtained for the embedded memories correlate well with the figures from AT697E and from ATC18RHA. With a careful application design, ensuring proper initialisation and regular refresh of on-chip memories to prevent SEU accumulation, the residual, non-correctable upset rate, possibly caused by Multiple Bit Upsets (MBU) in memories or Single Event Transient (SET) effects, is reduced to a negligible rate.

- The development activity will be closed with ESCC evaluation/screening, planned in Q2/2011
- Evaluation boards are available from Aeroflex Gaisler and from Atmel
- Packages: LGA 349, MQFP 256. MCGA 349 is not available any more, alternatives are under investigation

After the success of TSC695 with ~ 2900 flight models ordered since its introduction in 2001, the AT697 family has already booked orders for ~ 600 EM and ~ 400 FM parts since its introduction in 2009. This fast growth rate proves the success of AT697.

4 LEON3-FT BASED SPACECRAFT CONTROLLER ON-A CHIP [SCOC3]

The SCOC3 has been developed by EADS Astrium in France, a block diagram is shown in Figure 1.

After the first prototypes delivered in May 2009, an ESA activity undertaking validation and initial SW development (BSP, drivers and tool chain) is currently progressing. At the end of this activity, foreseen mid-2011, SCOC3 shall be commercially available as an [ESSP]. SCOC3 is equally affected by the unavailability of MCGA packages. As MQFP is not an option for the 472-pin package, LGA is the only alternative currently offered by Atmel. In flight equipment, SCOC3 is currently being used with 6-sigma columns assembled in USA. To mitigate potential ITAR risks, this process should be transferred to Europe.

ESA has furthermore requested to perform an SEU characterisation of SCOC3.

In complement to the ESA activities, as presented in [OBC], a SCOC3 simulator and a starter kit (STARKIT) are now available to support application development. STARKIT was developed with CNES support, and it contains the SCOC3 design in a Xilinx Virtex4 FPGA.

Furthermore, two invitations to tender (ITT) are in progress:

- The TRP activity “SCOC3 SW support” aims at developing a BSP and drivers for SCOC3 under Edisoft RTEMS 4.8.0 and to make them available to the space community
- For the “On-board computer for planetary landers” in the MREP programme, SCOC3 is one possible baseline component

The SCOC3 has been selected for the SEOSAT and ASTROTERRA (SPOT6/7) missions.

5 LEON4-FT BASED NEXT GENERATION MICROPROCESSOR [NGMP]

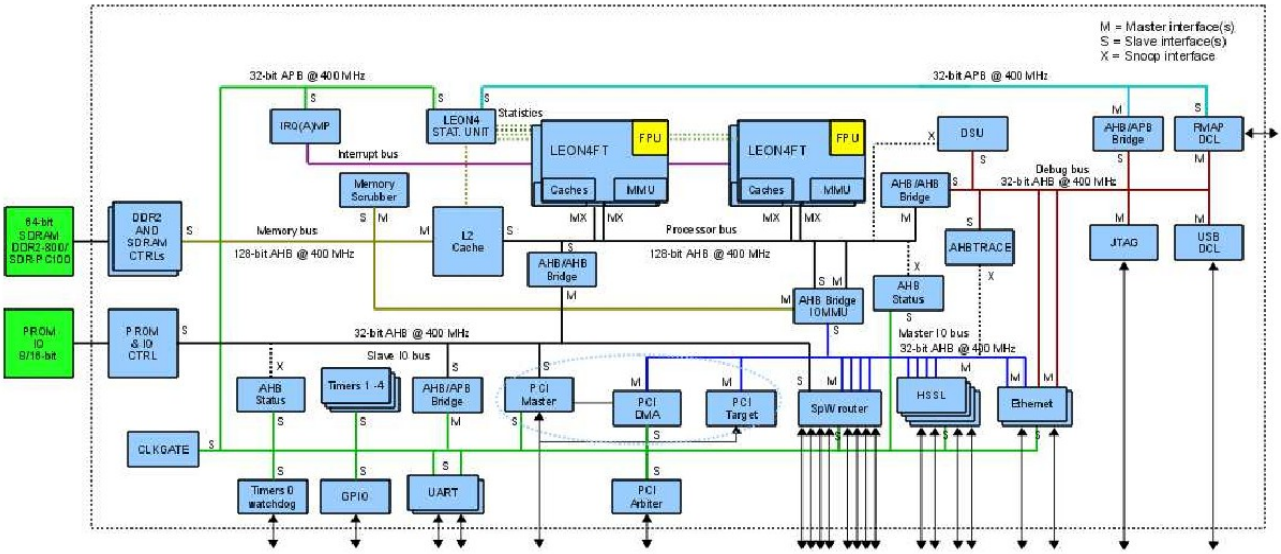

Figure 3: NGMP Block Diagram

The NGMP is currently under development by Aeroflex Gaisler in Sweden. After the System Requirements Review (SRR) in February 2010, the Next Generation Multi-Purpose Microprocessor has had its Preliminary Design Review (PDR) in December 2010. The VHDL code has been established and verified in simulation and on FPGA. The design has been ported onto several commercially available FPGA prototyping boards: Aeroflex Gaisler GR-CPCI-XC4VLX200/GR-PCI-XC5V, Synopsys HAPS-51/HAPS-54 and Xilinx ML510, TerASIC DE2-115 (Altera Cyclone 4). The first boards have been shipped to ESA and other beta users.

Related documents and presentations are posted at [NGMP], and it is intended to keep users informed about the progress of the activity via this web-page. A preliminary data-sheet and a technical note with benchmark results is now available.

The NGMP architecture published in March 2011, represented in Figure 2, is characterised by the following main features:

- 4 LEON4FT CPU cores with 2 shared FPUs. LEON4 implies an L2 cache, a 128-bit AHB processor bus and ranch prediction
- 4 CPU cores with two shared FPUs (baseline)
- Multiple AHB bus structure to decouple IO and debug transfer
- Full MMU protection for processor and DMA IO peripherals
- Duplicated timer and interrupt infrastructure supporting AMP configurations
- Enhanced debug features, such as trace buffers on PCI/AHB, statistics/performance counters allowing to profile SW applications
- Various debug link via Ethernet, JTAG, USB or RMAP
- 64-bit DDR2 / SDRAM / PROM memory interface with background scrubbing unit
- High-Speed-Serial link interfaces (based on ST HSSL, details TBD)
- Spacewire router with 8 external Spacewire ports and 4 internal AHB DMA ports
- PCI 2.3 32-bit 66 MHz link, 2 Ethernet links
- UARTs, GPIOs

Certain implementation details, such as the final choice of memory interface (DDR1/2/SDRAM), or the exact binding of the (shared) FPUs to the CPU cores remain open, as they are either technology dependent or may still be subject to further evaluation.

First benchmark results show that a single core in NGMP has a Cycles Per Instruction (CPI) ratio which is about 30% better compared to AT697, and up to 100% better on floating-point benchmarks. The performance for multi-threaded benchmarks, which fit into the L1 cache furthermore scales well with the number of CPU cores.

Target technology for NGMP is the space 65 nm node from ST Microelectronics [DSM], which is being developed in several ongoing and planned ESA funded activities. Should this technology not be available, a possible back-up could be the 130 nm library from [RAMON] Chips on Tower foundry.

The present TRP development contract is set to end with a detailed-design phase, mapping the NGMP into target ASIC technology. The design is now ready for this synthesis in the target technology (65 nm from ST Microelectronics), but the activity is on-hold due to non-availability of the space design kit from ST Microelectronics.

Next steps in the NGMP development roadmap are the manufacturing of functional prototypes in commercial 45 nm structured ASIC technology [EASIC] and the development of a board which will be made available to users at a moderate cost, allowing the evaluation of the full NGMP architecture at full speed, before going to a rad-hard space technology. The respective contract has been kicked off in April 2011, interfacing seamlessly with the present activity.

Additional funding has been approved under ref. # T701-302ED of the TRP 2011 - 2013 work plan to manufacture and validate NGMP Engineering Models in target ASIC technology. The start of this phase is also delayed, waiting for the availability and accessibility of the space design kit from ST Microelectronics and the appropriate hard macrocells, e.g. DDR2 PHY and High-Speed Serial Links (HSSL).

In parallel, ESA has also initiated a study on the System Impact of Distributed Multicore Systems, a contract being assigned to Astrium Toulouse and UPV. Main objective of this activity is to provision a hypervisor (Virtual Machine Monitor, VMM) for NGMP, but this activity is also expected to provide feedback for the ongoing NGMP chip development.

Several new SW development activities related to NGMP and multi-core computers have been proposed in the frame of the TRP 2011 – 2013 work plan, namely:

- Development Environment for Future Leon Multi-core (T702-302SW)

- Emulators of future NGMP multicore processors (T702-304SW)
- Schedulability analysis techniques/tools for cached/multicore processors (T702-308SW)

6 Conclusion and Outlook

Similar to ERC32, AT697 and AT7913E are or begin to be well established, successful microprocessor products and not much development work needs to be done any more. Nevertheless, documentation, support and supply chain needs to be worked on.

The development of SCOC3 is in overall very successful, but radiation testing is to be done and commercialisation remains to be consolidated, and a fully European packaging solution to be established..

Key challenges for the coming years are NGMP and the development of a new space microcontroller.

While the front-end design of NGMP is progressing very well, on schedule, major concern is the availability of the ST 65 nm space ASIC technology.

For the microcontroller, further ESA internal investigation and consolidation of requirements is necessary, before external development activities can be launched. Main topics are the selection of the processor IP and, again, the availability of a suitable ASIC technology providing in particular mixed-signal capabilities.

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