IP 07

Session : IP business model

ESA IP CORES SERVICE

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Abstract : *The Microelectronics Section of the European Space Agency (ESA) maintains and distributes a catalogue of reusable IP cores, for space and/or commercial use. Many of these IP cores have already been used in various ESA missions, and by the space industry for several space-related developments. This article provides an overview of the ESA IP cores service, with details regarding the available IP cores and the licensing options under which these designs are available. Furthermore, an overview of current and future activities of the ESA Microelectronics Section, related to SoC development, design reuse and high level modeling of digital systems, is also presented.*

1. Introduction

The Microelectronics Section of the European Space Agency (ESA) [1] maintains and distributes under ESA licenses a catalogue of reusable building blocks (also called Intellectual Property Cores, or *IP Cores*) which comprise typical digital functions used in space-born platforms and payloads. Examples of such functions include: telemetry and telecommand (TM/TC), error detection and correction (EDAC), microprocessors (LEON2-FT), on-board data handling (OBDH), SpaceWire, Controller Area Network (CAN), etc. [2] These IP Cores were originally developed in the scope of ESA activities, ranging in their origin from in-house ESA staff developments to ESA external contractors' work, and being implemented and validated in diverse types of integrated circuits spanning from simple Field Programmable Gate Arrays (FPGA) to complex System-On-a-Chip (SOC) full custom application specific integrated circuits (ASIC).

The IP cores provided by ESA are "soft-cores", aiming to be technology independent, and were developed using Very High Speed Integrated Circuit Hardware Description Language (VHDL). They can be easily synthesized and implemented in virtually any ASIC and FPGA technology.

ESA provides this "IP Cores" service in an attempt to meet the following main goals:

- reduce costs of large Integrated Circuits (IC) developments (e.g. Systems-on-Chip) by reusing already designed and validated IC functions.
- help to guarantee the availability of some key functions in a technology independent format ("soft format"), counteracting the limited availability and eventual obsolescence of Application Specific Standard Products (ASSP) which implement these functions.
- promote and consolidate the use of standardized functions, protocols and/or architectures (e.g. SpaceWire, CAN, TMTC, etc) by making these functions readily available to IC design groups.
- centralize IP users' feedback in the European space IC community to improve quality of existing IPs, and identify future needs in order to improve the IP offer to satisfy space industry new needs.

The ESA VHDL IP cores can be licensed for space research and/or commercial use, under specific conditions (depending on the IP ownership) to companies based in ESA member and participant states. [3]

The aim of this paper is to provide a more detailed overview of the ESA IP cores service, the available IP cores, and the procedures for licensing and distributing these IP cores.

2. History and background

As mentioned earlier, the origins of the ESA IP cores were ESA funded internal and external activities. A number of VHDL designs of high

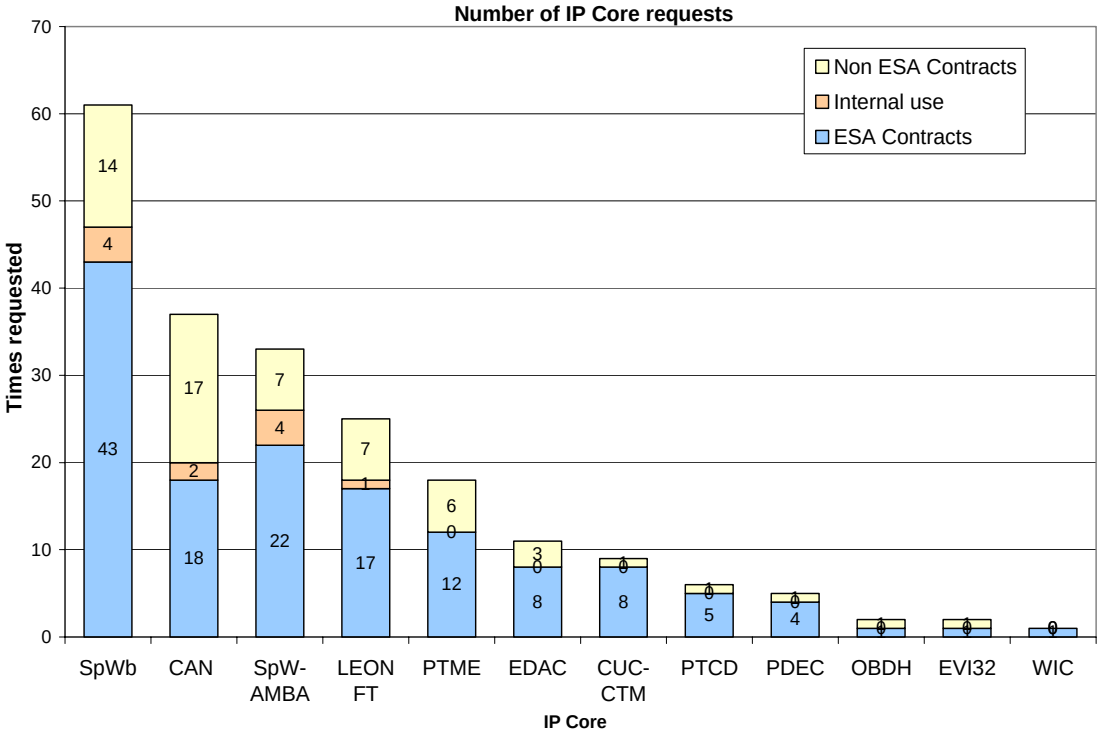

Figure 1: Number of IP requests (April 2002 - November 2007)

reuse potential were developed internally at ESA in the late 90's – early 00's. The designs include a Controller Area Network (CAN) controller, the LEON1/2 microprocessor, a Packet Telemetry Encoder (PTME), Error Detection and Correction (EDAC), etc. Furthermore, ESA contracts normally grant Intellectual Property Rights (IPRs) to the Agency for the reuse and sublicensing of externally developed new VHDL designs. The SpaceWire-b and OBDH cores are examples of designs licensed under such agreements.

In the meantime, ESA contractors - as well as a few non-ESA customers - started requesting these IPs for reuse in ESA contracts or private developments. After a growing number of requests, in 2003 the ESA Microelectronics Section, in collaboration with the Electrical Engineering Contracts Service (both located in the European Space Technology and Research Centre (ESTEC), in Noordwijk, The Netherlands) started to normalize and regulate the ESA IP Cores service: an internal IP Policy was established, along with some technical and administrative databases; licensing models were set up; additional human resources were invested, a new web site was established, etc.

The service has been well received so far, with increasing interest from the space industry. This interest is also reflected in the number of requests for these IP cores (Figure 1).

3. Overview of the ESA IP Cores catalogue

The list of IP cores provided by ESA is given in Table 1. The deliverables with each IP core distribution include the IP documentation (user's manuals, functional description documents, verification documents, datasheet, etc), VHDL source codes for the design and testbench files, and simulation and synthesis scripts. The amount and quality of the existing documents and source code files varies from IP core to IP core, depending on its origin. Nevertheless, ESA considers that the quality of the currently offered IP cores is good enough to encourage and promote their reuse at their current state (or with modifications, if the target application or technology requires it). Furthermore, ESA continues to maintain and improve the present catalogue with the valuable help of the users' feedback and ESA's very limited resources.

3.1. Procedure to request and obtain an ESA IP Core

In order to obtain an ESA IP core, interested parties are encouraged to follow the steps listed below:
In order to obtain an ESA IP core, interested parties are encouraged to follow the steps listed below:

a - Refer to the ESA IP cores website [2] for details about the available IP cores, download public design documentation, and even precompiled simulation models, which should assist in initial evaluations.

IP Core Name	Description	IP Origin
SpW-b	SpaceWire CODEC	University of Dundee (UK) (core) / Austrian Aerospace (A) (testbench)
SpW-AMBA	SpaceWire CODEC with AMBA interface	EADS Astrium, Velizy (F)
LEON2-FT	32-bit microprocessor (SPARC-compliant)	ESA Internal Development / Gaisler Research (S)
PTME	Packet Telemetry Encoder	ESA Internal Development / Gaisler Research (S)
CAN	Controller Area Network	ESA Internal Development
PDEC	CCSDS Packet Telecommand Decoder	Saab Ericsson Space (S)
PTCD	CCSDS Packet Telecommand Decoder. VHDL model of MA28140 chip by GEC-Plessey Semiconductors	EADS Astrium, Velizy (F)
OBDH	On-Board Data Handling bus	Alcatel Espacio (E)
CUC-CTM	CCSDS Unsegmented Code (CUC) & CCSDS Time Manager (CTM)	ESA Internal Development
EDAC	Error Detection And Correction Encoder/Decoder	ESA Internal Development
EVI32	32-bit VMEbus interface for the ERC32 processor chip set	ESA Internal Development
WIC	Wavelet	IMEC (B)

b - Refer to the "Licensing" page on the ESA IP Cores website for the terms and conditions of licensing the core(s). An "IP Request Form" can also be downloaded from that page, which will need to be completed and submitted to the Agency.

c - Once received, the IP request passes through an initial screening process. If all conditions are met, ESTEC Contracts Service proceeds with the preparation of a license agreement tailored to the customer's specific case.

d - Upon reception of the accepted licensing document (bearing licensee's signatures) by ESTEC Contracts Service, the requested IP(s) are delivered to the customer.

3.2. ESA IP Cores Licensing

There are two types of licenses available for the ESA IP cores:

1 – "Standalone" license:
This type of license is issued for the Licensee's "own purposes", as stated in the IP request form. It is issued for a period of 5 years (extendable by mutual agreement). A nominal handling fee is charged per IP core.

2 – License attached to an ESA contract:
This type of license is limited to the objectives, scope and duration of the ESA-funded activity (contract). The requested IPs are then provided free of charge.

There are some general terms and conditions applicable to both types of licenses: the licenses are non-exclusive and non-transferable, except when explicitly agreed (i.e. licensee may be granted the right to sublicense the IP cores to sub-contractors), and can only be issued within ESA member/participant states territory. The target application of the IP cores can be R&D and/or commercial, and must be non-military and peaceful (in accordance with United Nations' guidelines). It should also be noted that due to limited resources, ESA cannot commit to systematic technical support on demand for these IP cores, other than informing about known and independently verified problems and new IP version releases through the ESA IP Cores web site [2].

4. ESA initiatives to support IP reuse

Apart from maintaining, licensing and distributing the IP cores as described in the previous sections, ESA has also evaluated, and supported in some cases, a number other programmes and initiatives related to design reuse, IP packaging and cataloguing, other IP libraries, as well as various tools and methodologies for IP-based design of SoC. Examples of such programs, initiatives, events, tools or methodologies include:

- *SOCCER consortium :*

A consortium of European industries working in Aerospace and Defence, excellence academia and design houses with common interest for IP (re)use

in SoC. The objectives of this initiative were the definition and assessment of methods to select, validate and qualify commercial IP; setup a library of specific IPs commonly used for aerospace and defence applications, providing on-line access to a normalized system of IP quality levels; ease the design of complex, IP-based, SoCs. [4]

A number of ESA IP cores (SpWb, CAN) had been submitted to the SOCCER Consortium for cataloguing and addition to the portfolio.

- *OCP-IP :*

The Open Core Protocol (OCP) is an efficient, flexible, and scalable core connection standard. It specifies a signal exchange protocol over a family of on-chip interfaces, using a structured architecture that allows many different configurations, providing SoC designers a structured but highly configurable interface. [5]

- *IP-XACT (IEEE P1685):*

The IP-XACT standard (IEEE P1685), defined by the SPIRIT Consortium, describes an XML Schema used for meta-data documenting of Intellectual Property (IP) used for the automation of the configuration and integration of IP blocks. The standard also defines an Application Programming Interface (API) to make this meta-data directly accessible to automation tools. [6]

- *GRLIB from Gaisler Research:*

The GRLIB IP Library is an integrated set of reusable IP cores, designed for system-on-chip (SOC) development. The IP cores are centred around the common on-chip bus (AMBA), and use a coherent method for simulation and synthesis. The library is vendor independent, with support for different CAD tools and target technologies. A unique "plug and play" method is used to configure and connect the IP cores without the need to modify any global resources. [7]

- *1st ESA IP Cores Workshop:*

The 1st ESA IP cores workshop was organized in 2005 and took place in ESA's site at ESTEC, the Netherlands, with the participation of representatives from the space industry. The objective of this event was to discuss experiences from, and possible improvements to, the ESA IP-Core offering. [8]

5. Current and future ESA activities on IP cores and SoC technology

5.1. SystemC models of the ESA IP cores:

A SystemC model of the LEON2 microprocessor has already been developed internally in the section, and is due to be released. However, the model is not cycle accurate at the current state. A cycle accurate version is currently under development. Other developments, scheduled to start soon, include the development of SystemC models for the SpaceWire and CAN ESA IP cores, as well as for the LEON3 microprocessor.

5.2. SystemC/Python-based multi-processor simulation platform (ReSP):

In the context of the activities on SystemC, and Transaction Level Modelling (TLM), a Multi-Processor simulation platform (called ReSP) is being developed with the cooperation of Politecnico di Milano. ReSP is based on SystemC and Python, with the latter providing reflective capabilities to the platform. These reflective capabilities are employed to give the designer an easy way to specify the architecture of a system, simulate the given configuration and perform automatic analysis on it.

ReSP enables SystemC and Python interoperability through automatic Python wrapper generation. The overhead associated with the Python intermediate layer is around 1%, therefore execution speed is not compromised. This approach allows for easy integration of external IPs, fine grain control of the simulation, effortless integration of tools for system analysis and design space exploration. The reflective capabilities of ReSP can also be used to inject faults inside the models themselves by modifying the variables which determine their status; reliability analysis can then be performed.

5.3. Research activity regarding OCP-IP and SPIRIT/IP-XACT:

A new activity related to these technologies (OCP-IP and IP-XACT) will be funded under the ESA Technology Research Program (TRP) and it is planned to start in Q1 2008 [9]. The interfaces of a selection of IP cores from ESA's portfolio (LEON2-FT, CAN, SpaceWire) will be ported to OCP. SPIRIT XML descriptions of the selected IP cores will also be developed. The results will be made available to interested users as new IP through the ESA IP Cores Service. The objectives of this activity will be the development of OCP/SPIRIT building blocks for the investigation of the benefits and overheads, and the possible use and application of these technologies for future space SoC developments.

Apart from the aforementioned TRP-funded activity, the Microelectronics Section has carried out internal studies regarding the feasibility and benefits of OCP sockets, by developing OCP interfaces for the CAN and SpW-AMBA IP cores [10]

5.4. ESA ASIC / SoC developments (re)using ESA IP Cores:

There are multiple new SoC ASICs under development, many of which will become Standard ASICs available to the space industry as Application Specific Standard Products (ASSPs). These developments are already benefiting from the reuse of IP Cores, including ones from ESA's catalogue: Scalable Multi-channel Communication Sub-system (SMCS), a 10 port SpaceWire router, a SpW-Remote-Terminal-Controller, an Advanced GPS/GLONASS ASIC, a Spacecraft-Controller-on-a-Chip, and a general purpose SPARC V8 32-bit microprocessor for space (AT697E and AT697F), among others [11].

5.5. New ESA VHDL IP Cores:

In every new ASIC of FPGA development funded by ESA, the Microlectronics section tries to identify if there are new opportunities to produce new VHDL designs that could be reused in future projects. When this is the case, the contract is tailored to ensure that the quality and documentation of the new codes are such that they can eventually be incorporated to the offer of the ESA IP Cores. This has been the recent case of some new AMBA wrappers for existing IP Cores.

In addition, ESA has currently a new Invitation To Tender (ITT) specifically devoted to produce new IP Cores in functional areas where there seems to be a need and interest for them: advanced memory controllers, supporting various types of memory devices in fault-tolerant configurations (e.g. PROM and dynamic RAM types with SEU protection, like Reed-Solomon); mass memory controllers, providing hardware hardware implementation of relevant functions, such as the File Management Layer (FAT or Packet File Management) storage and retrieval functions as specified in the Packet Utilisation Standard; an CCSDS File Delivery Protocol (CFDP) engine implementing a subset of the CFDP core procedures, being compatible with ESA telemetry/telecommand IP cores (PTME, PTCD, PDEC), and interfacing to a file system or a mass memory controller. The activity described under this ITT is expected to be kicked-off in Q1 2008.

6. Space missions using ESA IP cores

There are numerous ESA space missions where many of the ESA IP Cores have already been or will be employed, in either FPGA or ASIC technologies, in the flight segment units but also in some ground test equipment or control applications. In most occasions ESA IP Cores co-exist with other commercial IP Cores and proprietary full custom designs inside the chips used in the spacecraft avionics, but it is clear that the existence and promotion of the ESA IP Cores has greatly contributed to shorten many development times of many ICs, and to foster the adoption of new (and even not so new) standardized communication protocols (e.g. SpaceWire, CAN, CCSDS Telemetry / Telecommand – TM / TC) and on-board computer architectures based on LEON. The trend continues even more so today, as many of these IP Cores start to be flown in space for the first time and this flight/mission heritage enhances the curriculum of proven, validated on the field IP Cores.

A few examples of space missions already using ESA IP Cores are mentioned below (listed per IP core) [12]:

- *SpaceWire (SpW-b)* :

GAIA mission; Proba-3 (Project for On-Board Autonomy-3); Maser-10; Advanced Imaging Interferometer in Geo orbit; BepiColombo mission to Mercury (in multiple instruments: BELA altimeter, MERTIS - Mercury Thermal Imaging Spectrometer, MANGA, SERENA, SYMBIOSYS).

- *Packet Telecommand Decoder (PTCD)*:

Considered for use in ground interface equipment to connect AGCS (ATV Ground Control Simulator) and TTFEEs (Telemetry & Telecommand Front-End Equipment) for ATV-CC (ATV Control Center) test and validation.

- *Packet Telecommand Decoder (PDEC)* :

Being considered for the BepiColombo mission.

- *Packet Telemetry Encoder (PTME)* :

KaTE experiment in SMART-1; Proba-2 (Project for On-Board Autonomy-2); being considered for BepiColombo.

- *SpaceWire with AMBA interface (SpW-AMBA)*:

APS image sensor for StarTracker; BepiColombo MERTIS (Mercury Thermal Imaging Spectrometer).

- *LEON2-FT:*

Proba-2 mission, and now being considered for several future missions such as BepiColombo, GMES Sentinels, Alphasat, Exomars, etc., as a standalone component or embedded in larger SoC ASICs.

7. Conclusions

An overview of the ESA IP cores service has been presented, as run by the Agency's Microelectronics Section at ESTEC, the Netherlands, along with a

presentation of other SoC design and IP reuse – related activities in the Section.

The ESA IP cores service has been well received by the industry so far. This library of reusable designs is being updated with new modifications and enhancements to the already available IP cores, like high level SystemC descriptions and OCP interfaces. New activities are also planned to extend ESA's catalogue of reusable IP cores with new designs.

Many of these IP cores have already been used, or are planned to be used, in various ESA missions. Furthermore, ESA IP cores are also used as the basis for further research and developments in the areas of SoC technology, high level modeling and simulation and on chip interconnect architectures, among others.

The existence and promotion of the ESA IP Cores has greatly contributed to shorten many development times of many ICs, and to foster the adoption of new standardized communication protocols (SpaceWire, CAN, CCSDS TM/TC) and LEON-based on-board computer architectures.

8. References

[1] ESA Microelectronics Section web site: http://www.esa.int/TEC/Microelectronics/index.html
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