Nanoelectronics trends, existing breakthroughs and applications for next generation satellites

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INTRODUCTION

Constant progresses in nanotechnology have induced a lot of ground electronic system breakthroughs in the last decade. Deep Sub Micron technologies are commonly used with up to 10^9 transistors / in up to date microprocessors in 45 nm. It has been mentioned that the computational power of nowadays mobile phones is already more than that used for Appolo programs. Already existing nanotechnology breakthroughs for ground consumer products and other ground embedded systems should deeply modify satellite architectures and performances. The purpose of this paper is to describe how existing new technologies can improve telecommunication satellites and how, on the other side, they allow new generation of sub systems.

The starting point is to appreciate the incredible progresses of nanoelectronic underlined with fresh Intel data. Then, the benefit of electronic miniaturization in satellite systems and strategic considerations will be overviewed. Current landscapes in Europe and technology limitations will emphasis the interest of ongoing 65nm ASIC technology development, future developments and perspectives.

But progresses are not only limited to integrated circuit. The “more than Moore” trend results in very compact mobile embedded systems integrating more and more functions with less and less power consumption, they are getting smaller and smaller thanks to heterogeneous vertical integration (stacked die, System in Packages, Passive integration…).

This level of 3D integration will be mentioned in this paper as well as the packages issues related to these systems in package and integrated circuit evolution.

There are other challenges that will be underlined related to lifetime, reliability and more generally all the issues related to the fact that all these advanced technologies have not been designed for space applications. As they offer an incredible level of performance, very low power consumption per gate and per MHz, Very Deep Submicron devices present a strong interest for space application. In addition, there are now the available technologies driven by mass production! Interest and “no choice” are combining each other.

Even if it is only a part of the clue, there are only a few percentage of Very Large Scale Integrated Circuits (VLSIC), paradigms have changed and it will be necessary to setup new approaches for the proper use of these components for space applications.

PROGRESSES IN MICROELECTRONICS

In 1965, Gordon Moore predicted that the number of transistors on a chip will double about every two years. Known as Moore's Law, this law should remain applicable at least for the next decade (figures 1 and 2) [1]. Regarding the economical interest, all the necessary changes have been performed by the manufacturers.

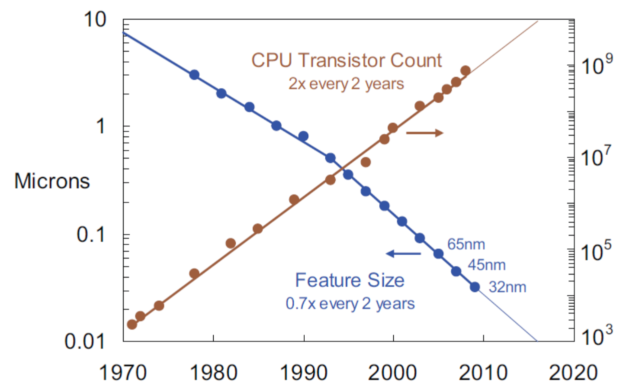


Figure 1: CPU transistor count and feature size trend [1]

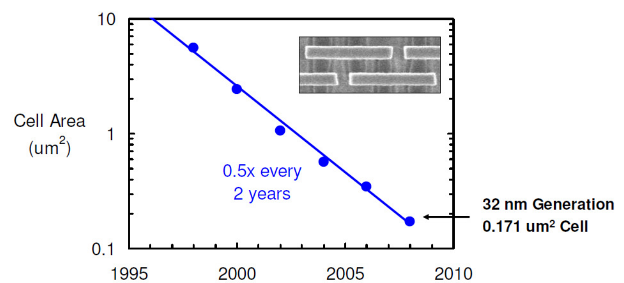


Figure 2: SRAM cell surface trend [1]

From a user point of view, the result can be summarized by the following comparison (table 1) [1] between an “old” 386 core computer and the “latest” generation microprocessor, the 45nm Intel Core i7 Processor with 4 Cores.

	i386	i7
Number of transistors	$280\ 10^3$	$731\ 10^6$
Clock Frequency (MHz)	16	3600
Cores	1	4
Cache	None	8 Mb
IO peak bandwidth	64 Mb/s	50 Gb/s
Adaptive circuit	None	Sleep mode Turbo mode Power gating Adaptive Frequency Clocking

Table 1: 386 versus i7 [1]

In addition to transistor shrinking, technology scaling has produced faster transistors and advanced micro architecture. Permanent technology evolution allows new choices that were not possible before: managing the tradeoff between power and mobility.

Regarding the power consumption, even if it is 10 times more for i7 compare to i386, we still have a huge improvement we can estimate by the following factor of merit F (equation 1).

$$F = N * F / W \quad (1)$$

With N number of transistor, F clock frequency and W power consumption at full speed.

Therefore, F_{i7} is 500000 higher than F_{i386}.

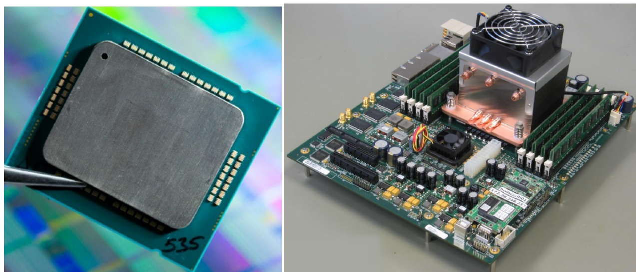


Figure 3: Intel Single-chip Cloud Computer (left) and board (right)[3]

A constant level or slight increase in performance give the opportunity of ultra low power consumption and very small devices, optimized for mobile application and ready for self powering. On the other hand, keeping quite the same chip size (and price) while technology evolves offers a calculation gain allowing now supercomputing and cluster computing on a chip [2] as it has been recently demonstrated by Tera-scale Computing Research Intel team [3]. They will offer Proven method to build reliable applications that scale to 100's or even 1000's of processors in clusters and datacenters today but with a little bit of power management to deal with as shown in Figure 3 [3].
In addition to architecture and thermal management issues, the large amount of data and high clock frequency result in high data rate transfer achievable by high speed serial links. So far, nanoelectronic has enough speed to deal with this but it should change in few years. Wired electronics is approaching practical limits for speed and length, due to electro-magnetic interference (EMI) and other issues. However, optical technology does not have these limitations since it transmits data using light instead of electricity.
Once again, Intel started to implement optical links as a concept of a new high-speed optical cable technology designed to interconnect electronic devices. Their Light Peak concept (Figure 4) delivers high bandwidth starting at 10Gb/s with the potential ability to scale to 100Gb/s over the next decade.

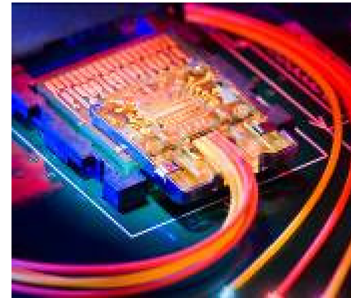


Figure 4: Light Peak concept implementation at chip level

BENEFIT OF ELECTRONIC MINIATURISATION IN SATELLITE SYSTEMS AND STRATEGIC CONSIDERATIONS

The electronic miniaturization is playing an ever-increasing role in satellite systems. The miniaturization has allowed major savings in mass, volume, and power at payloads level but allowed reliability improvements too. Over the last decade on board computer equipments (OBC) have evolved from multi boards systems populated with hundreds/thousands of components to multi chip modules (MCM hybrids) and finally to their ultimate evolution, systems on chip (SoC). Modern SoCs merge on a single monolithic chip, hardware digital processing features and software functions which were up to a recent past split over several boards.

This evolution has been made possible thanks to the increasing integration in the electronic industry, doubling the transistors density every 24 months according to the famous Moore's law. The Space sector, while being conservative and slow to endorse new technologies, has greatly benefited from the miniaturization essentially driven by consumer demand (computers, mobile phones).

For satellite Primes (Astrium, Thales, RUAG) following the technology pace, even with 2 or 3 generations, delay is vital in order to remain competitive. This is particularly true in the global market of telecom satellites systems (Boeing, Huges, Space Loral) where the most advanced miniaturized electronic, ASIC technology, can reveal to be a key differentiator with respect to competition. Nevertheless miniaturization may also be a benefit to other mission profiles such as science, exploration, and robotic.

The micro/nano electronics sector is strategic to enable Europe independence and competitiveness. Today all satellites make massive use of ASICs or FPGAs devices to implement digital functions such as microprocessors, DSP-

processors, networking, encryption, encoding / decoding. Securing a European supply chain is mandatory to first guarantee the continuity of existing products and second to stimulate the emergence of new products free from any export license restrictions (ITAR).

CURRENT LANDSCAPE IN EUROPE AND TECHNOLOGY LIMITATIONS

Over the last decade Atmel has been the main European supplier for Space grade microelectronics solutions. Its mainstream technology currently relies on a CMOS 180nm node (ATC18RHA) while other nodes (500nm and 350nm) were also proposed in the past. The ATC18RHA technology was recently used on telecom programs such as 'Digital Transparent Processor' led by Thales Alenia Space and 'Inmarsat XL' led by Astrium.

In both projects technology was pushed to the limits in terms of integration, speed, power dissipation and packaging. ASICs of 5 millions gates (~20 million transistors) were developed but the power dissipation exceeding 8 watts was a limiting factor to integrate more functions even if the technology would have allowed in theory up to 8 million gates per device.

Special techniques were deployed to cool down the ASICs and maintain their junction temperature at an acceptable level, which would have otherwise compromised their reliability and lifetime. In the case of Inmarsat XL a special AlN (Aluminum Nitride) package was developed to dissipate the power that a standard ceramic package would not have managed (Figure 4).

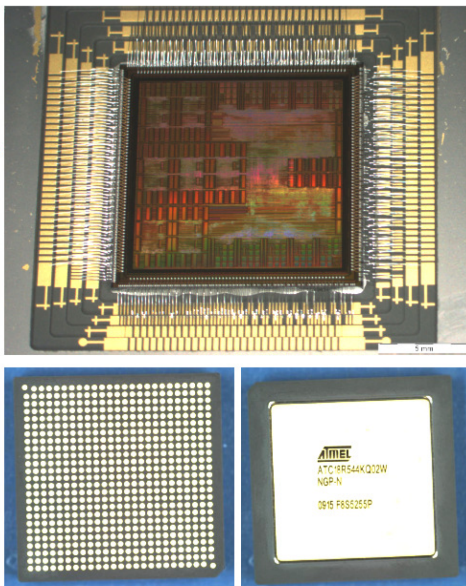


Figure 4: Astrium / Inmarsat XL ASIC and Aluminum Nitride (AlN)

The number of pins available on the package was also another issue. Indeed the increasing clock rates (~ 300 Mhz), internal but also external, generated by ADC and DAC converters for instance, required the demultiplexing of the data paths by a factor 2 or 4 to lower the clock rate and hence reduce the power dissipation. As a consequence of the demultiplexing and clock rate reduction (150 or 75 Mhz) the number of LVDS I/Os increased by a factor 2 to 4 and the number of internal data paths and associated logic increased as well in the same proportions. Those constraints translated in the need of having a new package with a higher number of pins. An AlN package with 625 pins was then specifically developed in the frame of Inmarsat XL program.

The solution hence adopted by Astrium was able to cope with the stringent requirements for more power dissipation and higher pin count. This development was challenging in the sense that it represented a big leap from previous package solutions limited to ~ 480 pins; new assembly techniques and PCB reporting had to be tested and qualified.

Close network are usually used to ensure the full connectivity, involving then thousands of Gbps links between ASICs and also between ASICs and data converters (ADCs / DACs).

Today limits have been reached with current ASIC technologies (180 nm), parallel synchronous buses using LVDS buffers for instance are limited in speed to ~ 200 Mbps requiring therefore a high level of parallelization to reach Gbps throughput. In some cases like digital beam forming payloads (Inmarsat XL), synchronicity has to be maintained within the payload or between all the ASICs. Therefore complex calibration mechanisms based on plesiochronous techniques (FIFOs) have to be deployed to compensate the various delay paths between ASICs. All those elements put together, more LVDS buffers due to parallelization and additional glue logic to compensate delays between ASICs translated in extra complexity, bulkiness / mass and at the end, power consumption. In telecom payloads every Watt lost in anything else than transmission represents a pure loss of revenue from the Operator point of view.

To tackle those issues and make digital telecom payloads more appealing with respect to their analog counterparts, ASIC technologies have to be pushed further ahead. That was the rational for the new ESA activity named "Deep Sub Micron" (DSM) kicked off in Q1 2008.

65nm ASIC TECHNOLOGY DEVELOPMENT

When launched in 2008 the objective of the DSM program, in partnership with ST Microelectronics (Grenoble / France), was to bring an answer to the challenge for higher integration, higher data rates, higher pin count and better power efficiency. The specifications at that time were aiming at an improvement factor 4 in integration capacity compared to Atmel 180nm process.

Therefore the new Rad Hard 65nm process had to offer a capacity of ~ 30 millions gates (120 million transistors) and

also an increased data rate of ~ 400 MHz. But higher integration and higher data rates would mean little without efficient interfaces. That is why from the very beginning of the DSM program high speed serial links interfaces (HSSL) were identified as a key element to support the Giga bits or Tera bits of data processed per ASIC and to overcome the bottlenecks that the limited number of IOs represented. Moving from an old paradigm where data were transmitted over synchronous parallel LVDS buses limited to ~ 200 Mbps to a new paradigm where data were serialized and transmitted asynchronously at a very high speed, 6.25 Gbps, was a major leap.

This evolution has been accompanied by a change in packaging technologies, where classical wire bonds solutions were replaced by flip-chip solutions. Flip-chip techniques allow higher pin count while minimizing package parasitic (RLC) and making then possible the use of very high-speed interfaces (6.25 Gbps).

Another important aspect of the future DSM technology is its cost and affordability. The manufacturing of a complete mask set in 65nm may rise to ~ 1M€. Therefore two options will be proposed in the future to end users: either a Rad Hard "standard cell" library or a "metal customizable" library.

The standard cell library will definitely offer all the degrees of freedom plus the possibility of embedding as many HSSL interfaces as needed. The down side of this approach is its associated cost.

On the other hand the metal customizable library might be economically more interesting, and will offer an ASIC platform where resources are pre-diffused or pre-placed and routed. The metal customizable platform might be comparable to an FPGA approach where resources such as high speed serial links (HSSL), IOs, memories, glue logic are already present in the silicon and the end user performs the customization at interconnects level. In FPGAs technologies the interconnect customization is done thanks to SRAM based look up tables (Xilinx, Altera) or by a programmed burning of anti-fuses (Actel).

In the case of an ASIC metal customizable platform interconnects are defined at manufacturing time and only the 5 top mask layers are manufactured as opposed to the ~ 30 mask levels needed in a classical standard cell approach. This brings therefore significant time and cost savings; but on top of the cost advantages just mentioned, metal customizable platforms may also offer easier manufacturability and testability which in turn means higher reliability.

Indeed having the logic arranged in a regular matrix pattern, allows easier design for manufacturability rules (DFM) and also easier radiation hardening techniques to be deployed. This ensures then higher reliability and yield at manufacturing time but also easier testing since the logic is not anymore randomly placed like in standard cell technologies but follows instead a regular matrix pattern layout.

All the advantages listed here above are counter balanced by less customization flexibility and lower gate density when compared to standard cell solutions. Those are the tradeoffs an end user will have to carefully assess before starting any new design. In terms of requirements the future DSM platform will deliver 30 Millions equivalent ASIC gates, will feature 32 HSSL (6.25 Gbps), will offer ~ 1000 IOs (CMOS, LVDS), will dissipate ~ 15 watts max and lastly shall be operable for 20 years in harsh Space environment (radiations, extreme temperature).

FUTURE DEVELOPMENTS AND PERSPECTIVES

DSM 65nm technology and HSSL will be key enabling elements to open new horizons for a set of demanding applications. Among those applications, telecom might be the first to benefit from advanced integration / miniaturization progress. The availability of a 65nm Space technology should enable the emergence of a new class of telecom satellites, more agile and more versatile. When procuring a satellite system, for 15 or even 20 years lifetime, telecom operators can hardly predict how the traffic and demand will evolve over that period.

Therefore more system flexibility is desired and this will be introduced thanks to, for example, more antenna beam flexibility. Multi beam antenna systems built upon hundreds of sub beams will have the ability to adapt with a fine granularity to the geographical and time traffic evolution.

Future telecom satellite systems will support as well multi role missions and will for instance broadcast HD TV services and offer point to point services, internet or mobile telephony. To guarantee those multiple services, a better onboard power management is needed in order to allocate dynamically more or less power to the beams according to traffic demand.

This fine power management will be enabled thanks to a new class of broadband digital beam forming satellites systems. More power will be allocated to sub beams where traffic is higher. Beams might also be shaped and steered in such a way that they may adapt to geographical constraints or avoid interference due to frequency reuse. Complex multi beam antenna systems will also require very accurate and adaptive optimizing techniques to minimize link losses and again optimize onboard power.

The emergence of this new class of broadband digital beam forming satellites will be conditioned by the availability of the DSM 65nm technology. The demanding requirements set by those new payloads, cannot be fulfilled with the existing state-of-the-art digital technology for space application (Atmel 180nm), nor by analog RF payloads that may potentially offer alternatives from a power consumption

point of view but will certainly not bring the flexibility or versatility offered by digital beam forming payloads.

Other applications will also benefit from DSM 65nm with microprocessors and DSP processors. In Q1 2010 the Next Generation Multipurpose Microprocessor (NGMP) activity was kicked off. This new activity aims to develop a successor to the LEON II / III Space microprocessors, while still maintaining compatibility with Sparc V8 architecture. The current single core LEON architectures can only deliver 80-100 MIPS but the new multi core processor (NGMP), planned as a quad core, will aim at 400 MIPS. Such a level of performance can only be reached with the availability of a DSM 65nm technology.

Space Fiber is another field of application that may benefit from Space DSM advances. Space Fiber will be the successor of the current and well known Space Wire, a high speed serial link offering today a peak transmit rate of ~ 400 Mbps. Those limitations in speed are conditioned by the performances of the 350nm and 180nm ASIC libraries used to implement the Space Wire transceivers.

Tomorrow those limits might be overcome by the use of the DSM 65nm Space technology. The new Space Fiber transceiver will exhibit 6.25 Gbps data rate for a power that may not exceed 150 mW.

Another potential application for the DSM is the future high density SRAM based European FPGAs. The availability of the 65nm technology coupled with HSSL (6.25 Gbps), the NGMP microprocessor and Abound Logic FPGA technology may enable the design of a full European high density reprogrammable FPGA for Space. This reconfigurable FPGA platform may allow the integration of multi million equivalent ASIC gates, presenting functional capabilities very similar to the well known Xilinx technology. The amount of FPGAs embedded in satellite systems tends to grow from year to year. In the medium-long term FPGAs will most likely never replace ASICs entirely but surely FPGAs will stay as a very significant percentage of the total number of custom integrated circuits used on board.

Now if we project ourselves in a longer term future which type of applications could we envisage thanks to DSM technology? Definitely massive parallel architectures or Network on Chip (NoCs) will be the answer.

As mentioned earlier the future DSM technology will offer an integration capacity beyond the 100 Million transistors per chip. Therefore if we want to boost the development of future complex Systems on Chip (SoCs) we have to find a way to shorten the development cycles and a way to manage the increasing complexity. This can be achieved by the introduction of a new paradigm called Network on Chip. Thanks to NoC paradigm micro/nano electronics will enter in a new area where design will become more modular. The various intellectual property functions (IPs) within a SoC will not be anymore organized around an old fashioned bus-based architecture, leading to congestions, bottlenecks and limited scalability. Instead, IPs within NoCs will be organized configuring a network, with point to point connections between routers (Figure 5).

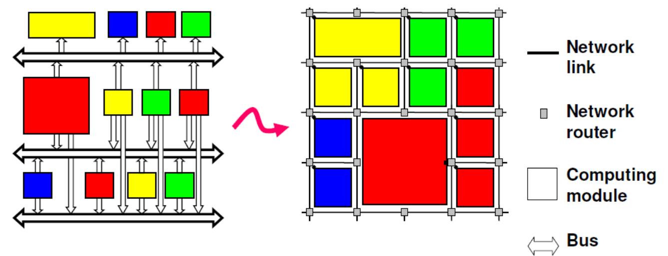


Figure 5: the NoC paradigm shift

In NoCs each IP function will be associated with its own router, clock system and possibly standardized "Open Core Protocol" interface (OCP). This new paradigm from a design point of view will lead to handle each IP function as an independent "island". This approach will hence encourage and facilitate IP reuse as well as scalability of the system. Introducing point to point communication between IPs will also alleviate the typical congestions of shared communication media inherent to bus systems.

Finally from a mission perspective NoCs could introduce novel concepts for on ground and in flight testability. New fault tolerant strategies could be deployed and take advantage of NoCs scalability in order to implement graceful performance degradation by, for example, performing static or dynamic network reconfiguration in the event of local malfunctions or traffic congestions.

ASICS VERSUS COMMERCIAL COMPONENTS

Integrated circuit market is mostly driven by consumer mass market products. New technologies stand also for challenging processes with hundred of elementary step, expensive tools, skyrocketing design and process costs (Figure 6). A 300 mm wafer fab cost is 2 000 M€.

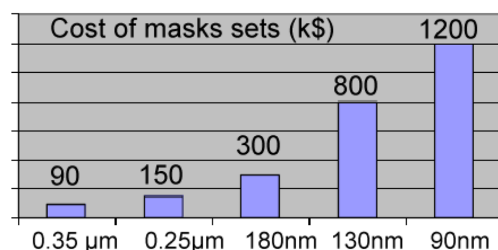


Figure 6: Cost of masks sets versus technology node

On the other hand, as predicted by Moore's law, the cost of elementary function is always decreasing: in 1973, the cost of 1Mb memory was 75 k€, nowadays, it is 0.05 € and the trend is still the same.

This apparent discrepancy is the direct result of mass production concentration: there are less and less wafer fabs to make the worldwide VLSI production.

Most advanced wafer fabs have a production of more than 10000 wafers a week while few 300 mm wafers a month could be enough for space needs. There are few consequences:

- ASICs are getting more and more expensive (design and masks sets) and even if it is the "best" solution; it will probably remain limited to few key applications. Configurable devices (FPGAs) will limit a little bit impact of No Recurrent Engineering.
- For performance purpose, large FPGAs, DSP, high density memories and other ultimate digital commercial products which require high development costs can be used for space applications with a specific product procurement and quality approach (not the purpose of this paper).
- In both cases (ASICs and commercial parts), the technology developed by the Integrated Circuit Manufacturer is not primarily dedicated to space applications and therefore trigger challenging tradeoffs.

ADVANCED PACKAGING ALTERNATIVES

Whatever the component is, ASIC or commercial, the packaging is getting more and more challenging. We already mentioned thermal issues, high density interconnections and high speed.

Scaling for conventional planar packaging of ICs (2D) is nearing its practical limits, even with Flip Chip and BGA approaches. To overcome these technological and physical limitations, Three-dimensional (3D) integrated systems in package (SiPs) allow smaller, lighter, and thinner packages with an improvement of the inter chip signal and power distribution.

Among various possibilities to use the vertical dimension to integrate electronics, three solutions are nowadays quite "standardized". These three architectures are described in the Figure 7.

The first one called "stacked dice" is the more spread for the mass market. It consists to stack die with or without an interposer (raw silicon) between each die level. Dice are connected to the PCB using wire bonding or using flip chip technology to connect the first level directly to the PCB.

The second one called "Package on Package" does not offer the same potentiality for integration but offers other advantages. For instance this kind of technology allows the individual electrical testing of each component prior the vertical integration and allows the flexibility for the integration of elementary IC from multiples suppliers. The challenge for this technology is to manage the stacking process.

The name of the third one "Package in Package", suggests all the possibility of this technology to provide the flexibility of combining structures to meet the functional needs in one package. The challenge is to manage the assembly of various kind of package while mastering CTE, thermal dissipation, EMC, … of this large Lego. This configuration is mostly used for custom products.

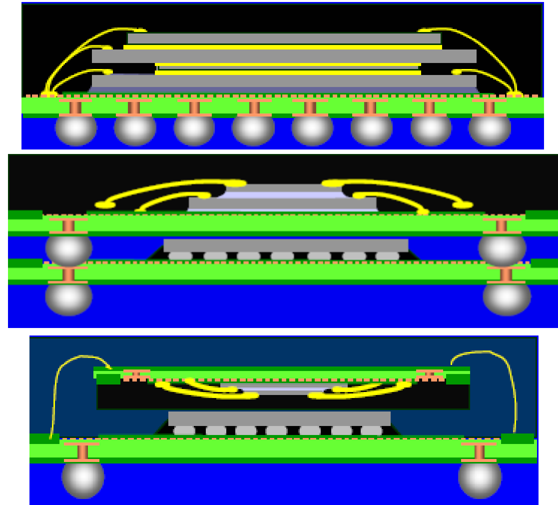


Figure 7: SiP technology overview- stacked dices (top), Package on package (middle), package in package (bottom)

3D packaging using stacked and interconnected chips is probably the technology at next generation for IC packaging as it has a promising potential. With such a technology we can achieve high silicon efficiency, less signal time delay, less power consumption of system, more speed and clock rate due to lower overall interconnection … etc. Through-hole Silicon Via (TSV), Figure 8, is currently considered as the ultimate 3D interconnects [5].

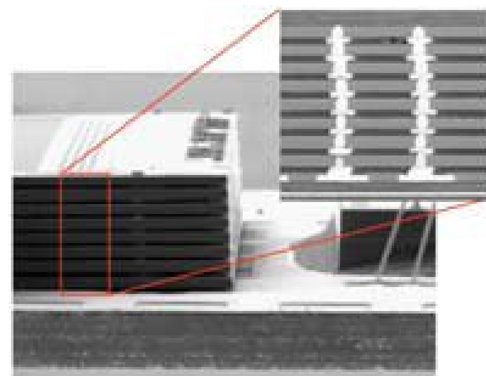
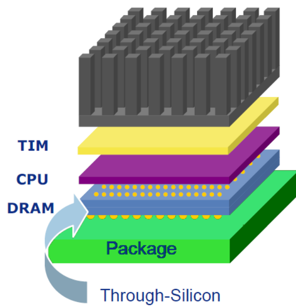


Figure 8: Cross section of stacked dice with TSV [5]

After long R&D phases, TSV technology appears ready to move into the industrialization phase where economic realities and rules will determine which technologies will be adopted and probably standardized.

Ultimate 3D integration for VLSI will combine die-to-die vias and TSV to stack different devices (Figure 9)



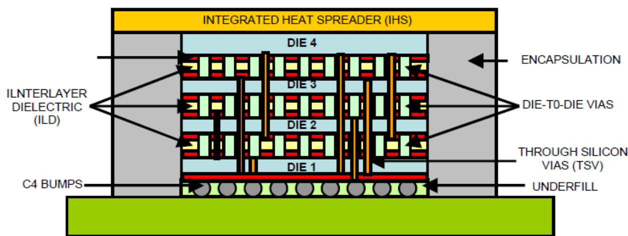


Figure 9: Die Stacked (top) and interconnections (bottom)[6]

The purpose of 3D integration is not only to solve packaging issue for coming VLSI, it is also the possibility to integrate various technologies (logic, analog, sensor, power, RF …) to form a specific system with very small dimensions.
For instance, among potential targeted applications for 3D integration, we find image sensors, flash, DRAM, processors, FPGAs, and power amplifiers. They can integrate embedded passives devices that provide right capacitors value for decoupling for instance.
This trend has been identified as "more than Moore" trend (Figure 10) moving from System on Chip (SoC) to System in Package (SiP)..

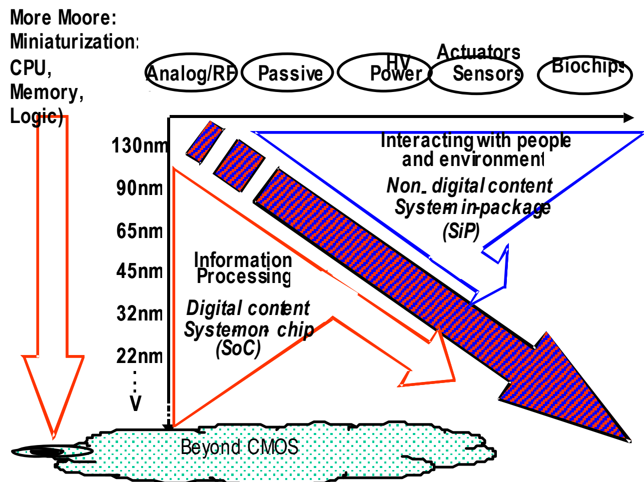


Figure 10: More Moore, more than Moore and beyond CMOS

MORE THAN MOORE APPLIED TO SPACE

SiPs allow a flexible integration of various electronic function within a single component. The resulting system level integration is emerging as a driver of assembly and packaging solutions replacing single chip packaging. Mobile phone industry is the main driver for this kind of integration with high complexity, so the process must be cost effective and the design and the material used must preserve the basic functions of the package as a mechanical support able to withstand the signal and power distribution, the environment (Moisture Sensitivity Level)…

Beyond Moore's law that predicted 45 years ago the doubling of transistors density every 24 months, the More than Moore's law focuses on benefits introduced by system integration technologies.

In many cases, Moore's Law Integrated Circuits deal with only 10 percent of the system. The other 90 percent is still there, composed of bulky discrete passive components--such as resistors, capacitors, inductors, antennas, filters, and switches--interconnected over a printed-circuit board or two through bulky connectors. System In Package (SIP) or System On Package (SOP) bring well beyond Moore's Law (Figure 11). It aims at integrating heterogeneous functions in a same package 0.

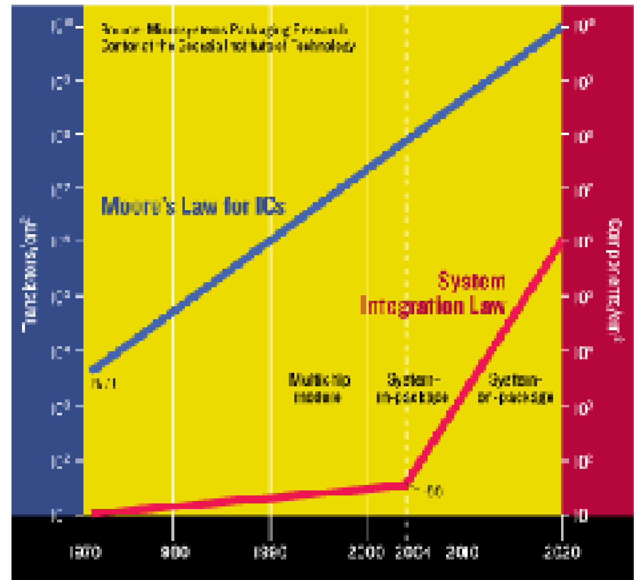


Figure 11 : Integration of transistors (more Moore) or Components (More Than Moore) 0

More than Moore systems combine ICs with micrometer-scale thin-film versions of discrete components, Micro Electro Mechanical Systems (MEMS), integrated batteries, antennas, etc. It embeds everything in a new type of package so small that eventually satellites could be reduced to less than a kilogram (i.e. pico satellites).

Micromachined (later MEMS) silicon sensor technology evolved started in 1960's and accelerated in recent years. In aerospace applications, such sensors are often subjected to shock and vibration, temperature and radiation requirements that exceed the needs of many earth bound applications.

Silicon sensors, because of the inherent physical properties of silicon, and especially because of the decades of process refinement in mainstream IC's, are uniquely positioned to address those needs. Early silicon MEMS piezoresistive

sensors made possible the development of modern jet fighters and advanced weapons systems. Today, silicon MEMS sensors will be found in the most space applications, from the space shuttle to satellites.

Coupled with wireless communication capabilities these sensors introduce new satellite architecture breakthroughs. Indeed, a satellite requires an important number of telemetry sensors to control it and monitor its health. On the other hand, satellite is constrained by size and weight. This issue limits the number of sensors that can be embedded in a satellite.

For ground experiments, it's also the same issue that limits the number of sensors used during the qualification phases. Vibration sensor cables induce weight that modifies satellite's response to vibration solicitations.

Self-powered wireless sensors offer new perspectives as they replace wires by wireless links and can be placed almost everywhere. Used in decentralized architectures, they monitor locally if a subsystem abnormally heats or consumes too much energy. If a problem is detected, they send alarms and diagnostics reports through long range wireless links. They can manage several Microsystems sensors and work corporately.

EADS Astrium studied on-board wireless networks (Optical or Zigbee) to reduce use of cables (Figure 12). Its work focused on link quality and electromagnetic compatibility. Several demonstrators were designed and tested 0.

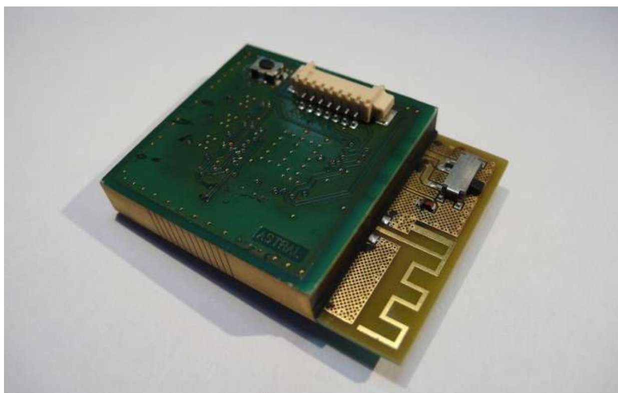


Figure 12 : Wireless prototype designed with CEA/3Dplus 0

First application will be used to monitor energy inside the satellite. Temperature/energy sensor will be integrated in each main satellite sub-system. The monitoring is decentralized: each wireless sensor monitors locally energy produced by solar cells, stored by batteries or consumed by equipment.

If an issue is detected, the sensor will communicate to the satellite controller and be relayed back to earth through the telemetry channel.

Figure 13 illustrates the SIP designed by INTESENS and that will be integrated in Astrium monitoring architecture.

Figure 12: INTESENS System In Package 0

NASA/GRC launched studies in Aerospace Structural Health Monitoring System along with advanced technical support. The impedance based structural health monitoring system targets to be designed as an autonomous, self-contained unit capable of assessing the general structural health of multiple material types within various aerospace components (e.g., turbine engine, airframe and space exploration components).

Furthermore, the system would have self powering capability, thereby reducing the dependence on wired external energy sources or batteries. The data acquisition, analysis, and reporting would be in the form of a distributed system where each node is self contained, hence ensuring high reliability.

Specifically, the SHM system would detect localized damage in the form of cracks, excessive deformations, or corrosion common in metals as well as various forms of distributed damage concerning composite materials (e.g., transverse matrix cracks, delaminations, fiber breaks, oxidation and etc.). Lastly, the system would differentiate between material damage and modifications in boundary conditions 0.

These examples clearly demonstrate the existing ability of SiP to measure (sensor), to process data (embedded processor), to store results (memory), to interact (actuator) and communicate (short range wireless communications). This kind of standalone, self powered and small SiP triggers a new generation of autonomous sub-system.

All the advantages provided by constant evolution of microelectronic must not hide the specific challenges we are facing using them.

DSM CHALLENGES AND OPPORTUNITIES

We can consider one technical challenge and another one linked to obsolescence. The technical challenge is linked to wear out mechanism.

International Technology Roadmap for Semiconductors still forecast integration evolution up to 2020. Size per function will decrease down to 0.001 μm^2 for Flash cells in 2 years and 10 times less in 2020 while average functions per chip will target 1010 at the same date. To do this, new materials,

new processes and extremely challenging trade off are continuously managed.

The very high level of VLSIC performances that can be used in embedded system is not free of charge!
Technology nodes are getting smaller and smaller, power supply decrease and margin voltage between 2 logic states is reduced down to few hundred of mV. On the other hand environment and atoms are not scaling!

Failure rate [11] is well described by a bathtub shape curve representing the variation of failure rate in Failure In Time (FIT) other time (see Fig. 14). It can be described by a Weibull law (equation 2):

$$\lambda(t)=\frac{\beta}{c^{\beta}}t^{\beta-1} \quad (2)$$

When the components begin to wear out, the failure rate increases. This final stage is known as wear out (β>1).
Old technologies, down to 0.35 µm, usually have hundred years of useful life so they easily fit with the mandatory lifetime. Components used in high reliability applications belonging to infant mortality part are screened by burn-in therefore these integrated circuits have their reliability mostly related to constant failure rate.

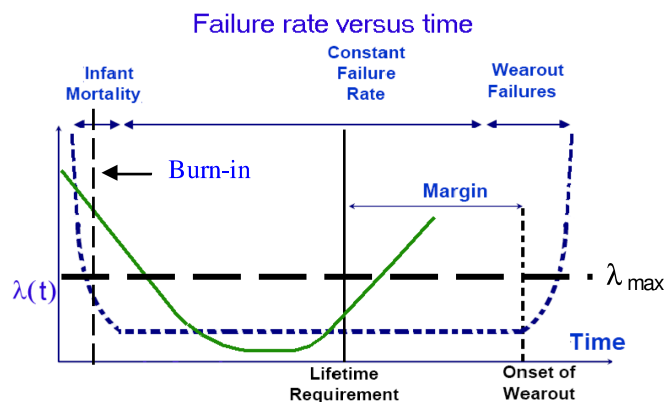


Figure 14: Bathtub curve for old (dashed lines) and new technologies

Frightening forecasts [12, 13] underline a critical decrease of useful life with new technologies down to few years. Direct consequences of integration (reliability technology requirements) for a long term reliability targeted from 10 to 100 FITs (1 FIT is one failure every 10^9 hours or 114155 years!) is to keep at least the same overall Integrated Circuit failure rate while integration challenges it.

As the number of transistors per chip increases, the relative failure rate per transistor must decrease from 1 (2005) to 0.2 (2013), so it should be divided by 5. As the length of interconnect per chip increases, the failure rate per m of interconnect must decrease from 1 (2005) to 0.33 (2013), so it should be divided by 3.

Unfortunately, Moore's law also means elementary size reduction. Aging factors like electrical field and current density are increasing. Electrical field, now limited by dielectric gate thickness, has increased from 1MV/cm (1970) up to 6 MV/cm. Interconnect current density is 10 times more (1 MA/cm²) than it used to be in 1970 (0,1 MA/cm²).

Atoms are not scaling so, consequently, some layers (like gate oxide) are only few atoms thick! Processes are getting more and more complex (hundred of steps) and coupled with atomic scale constraints, they trigger a lot of variability. It makes reliability management even trickier.

We can consider both FEOL (Front End Of Line) that represents active part of the devices (transistors) at substrate level and BEOL (Back End Of Line) that represents interconnections between transistors.

FEOL changes
A simplified description of MOS transistor performances is linked to a high saturation current IDSAT (equation 3):

$$I_{Dsat}=\frac{C_{ox}\,\mu Z\,(V_{GS}-V_T)^2}{2L} \quad (3)$$

with $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$

where µ is the mobility, Cox the gate oxide capacitance, tox the gate oxide thickness, VT the voltage threshold and VGS the gate source voltage. In order to keep a good VDSAT with node shrink, some choices have been done by ICM.
To keep Cox high with smaller surface, tox has been reduced but it cannot be done more than a minimum thickness to maintain dielectric property: the maximum electrical field must remains lower than the breakdown one. To face this limitation, another dielectric can be chosen in order to decrease εox. SiN has been used instead of SiO2 and now more and more High K dielectrics are used (HfO2…).

The main reliability drawback of these gates is an important wear out mechanism: NBTI. NBTI affects PMOS at on state. NBTI is one of the main wear out phenomena of up to date technology. It jeopardizes lifetime and force ICM to complex tradeoffs between performances, cost and lifetime. In addition, thin gates and other FEOL choices are very good for high speed but they also trigger a lot of leakages. Power consumption becomes important (up to 100 W for a 2 cm² chip) triggering challenging thermal management and wear out issues.

Another consequence of ultra thin gate oxide is that parasitic capacitance caused by polysilicon gate depletion is no longer negligible, even when polysilicon gates are heavily doped. It is why we have more and more metal gate with subtle VT engineering. Mobility is another parameter ICM can play with. Stress engineering can improve mobility by 30%!

Finally, all these parameters are subjected to ICM tradeoffs. For the same technology node, ICMs chose different process and design parameters according to device purpose: low

consumption or high performance… Reliability and lifetime are strongly dependent of these tradeoffs.

BEOL changes

In up to date technology, speed is not only related to IDSAT but also to RC charge related to interconnections. In order to reduce it, both R and C have to be minimized. R is reduced by the use of a less resistive metal; copper instead aluminum, while C is reduced by the use of low K materials. These choices have induced a lot of consequences. As copper etching is not possible, damascene and dual damascene processes, based on Chemical and Mechanical Polishing (CMP) are used. Copper easily migrate and thin metal barriers (Ta/TaN) encapsulate it to prevent copper migration in dielectrics.

To connect billions of transistors, more and more interconnection layers are used. The result is a stack of metal layers (up to 12 interconnection layers) with inhomogeneous mechanical and thermal properties. A lower K also means a lower Young modulus and a lower hardness for low K dielectric. Copper encapsulation causes residual constraint up to 2 GPa while thermal expansion layer mismatches, poor low K hardness and the stacked structure of BEOL facilitate thermo mechanical fatigue and its consequences (cracks, delaminations).

Time Dependant Dielectric Breakdown (TDDB) is a new failure mechanisms that appears at BEOL level while Stress Induced Voiding (SIV) is getting more important than the usual Electro Migration (EM).

Obviously, for each problem, a solution can be found. Trade-offs managed by ICM are not dedicated to long term use of electronics so we cannot longer expect to have incredible margins has we had during more than 30 years.
In addition to FEOL / BEOL failure mechanisms, integration and performances of VDSM devices also induce higher transient currents. The power consumption for each transition for each transistor is decreasing but transition is shorter: resulting current remains the same while the number of transitions tends to increase with the number of transistors. At constant die surface, transient current roughly double at each node generation (180 nm, 130nm, 90 nm, 65 nm, 45 nm …)

For all these reasons, wear out mechanisms happen earlier and they affect integrated circuits at transistor level (FEOL) and at interconnection level (BEOL). At FEOL level, HCI and NBTI induce leakages and slower transition.

Early wear out of device has to be properly evaluated. When a strong link with the manufacturer is established, these data are available with a great level of confidence and realistic reliability studies can be achieved by Design in Reliability [14].

For commercial parts, new approaches are under development [15]. In both cases, it is underlined that wear out mechanisms have to be taken into account at a very early design step.

The other challenge is linked to fast obsolescence of new technology. Manufacturer data presented during a CCT workshop [15] underline the strong reduction of technologies life cycle from 20-25 years in the sixties down to 2.5 year today.

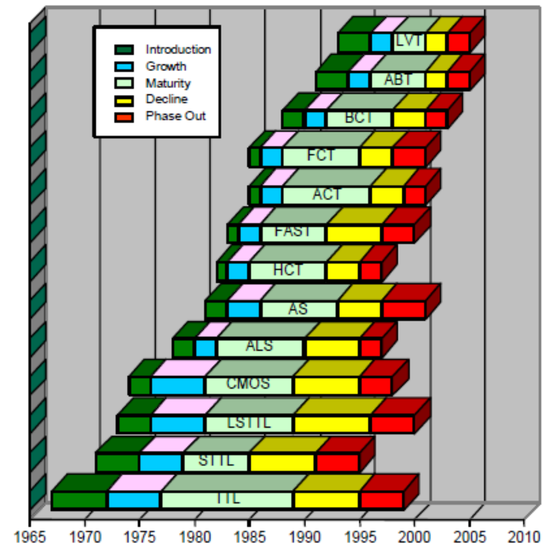


Figure 15: Technologies life cycle

Adapted circuit procurement or new architecture approach (plug in? function and interface? ...) have to be established.

CONCLUSIONS

Advance in nanoelectronic is a key enabler for two kinds of applications:
1) Massive and fast computation (telecommunication satellite for instance)
2) Standalone, self powered devices (new generation of miniature autonomous sub-system).

Nevertheless, Integrated Circuit manufacturers address Mass market and up to date devices are neither designed nor processed for space application.
In order to properly use them, early estimation of wear out issue has to be taken into account.
For commercial part, a specific attention has to be brung to obsolescence issues.

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