

## Deep sub-micron 65nm program Perspectives for the next generation satellites

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**Abstract:** This paper presents the recent advances in terms of European digital microelectronics technologies for space applications. This article exemplifies the case of the Deep Sub-Micron 65nm program led by ESA and CNES in partnership with semiconductor industry, ST Microelectronics. Recent programs such as Inmarsat XL (Astrium) have exacerbated the limits of the current digital ASIC (Application Specific Integrated Circuit). Those limits have been reached in all areas; transistors/gates integration, speed, power and number of available IOs. The DSM 65nm program shows how those limits will be overcome thanks to breakthrough technologies such as high speed serial links (HSSL / 6.25Gbps), high pin count flip chip package technology (1600 pins).

### I. ELECTRONIC MINIATURISATION IN SATELLITE SYSTEMS AND STRATEGIC CONSIDERATIONS

The electronic miniaturization is playing an ever-increasing role in satellite systems. The miniaturization has allowed major savings in mass, volume and power at payloads level, but allowed reliability improvements too. Over the last decade on board computer equipment (OBC) have evolved from

multi boards systems populated with hundreds/thousands of components to multi-chip modules (MCM hybrids) and finally to their ultimate evolution, systems on chip (SoC). Modern SoCs merge on a single monolithic chip hardware digital processing features and software functions which were until recently split over several boards.

This evolution was made possible thanks to the increasing integration levels in the micro electronic industry, doubling the transistors density every 18 months according to the famous Moore's law. The space sector, while being conservative and slow to adopt new technologies, has greatly benefited from the miniaturization essentially driven by consumer demand (computers, mobile phones).

For satellite Primes (e.g. Astrium, Thales, RUAG) following the technology pace, even with 2 or 3 generations delay, is vital in order to remain competitive. This is particularly true in the global market of telecom satellites systems (e.g. Boeing, Hughes, Space Loral) where access to the most advanced miniaturized electronics, ASIC technology, can reveal to be a key differentiator with respect to competition. Nevertheless miniaturization may also be a benefit to other mission profiles such as science, exploration, and robotic.

The European micro/nano electronics sector is strategic to enable Europe independence and competitiveness. Today all satellites make massive use of ASICs and FPGAs (Field Programmable Gate Array) devices to implement digital functions such as microprocessors, DSP-processors, networking, encryption, encoding / decoding. Securing a European space microelectronics supply chain is mandatory to first guarantee the continuity of existing products and second to stimulate the emergence of new products with only European-controlled export license.

## II. CURRENT LANDSCAPE IN EUROPE AND TECHNOLOGY LIMITATIONS

In Europe, ATMEL(F) remains the main supplier for space grade ASIC solutions [1]. Its mainstream technology currently relies on a CMOS 180nm node (ATC18RHA) while other nodes (500nm and 350nm) were also proposed in the past. The ATC18RHA [2] technology was recently used on telecom programs such as ‘Digital Transparent Processor’ led by Thales Alenia Space and ‘Inmarsat XL’ led by Astrium [3].

In both projects ASIC technology was pushed to the limits in terms of integration, speed, power dissipation and packaging. ASICs of 5 million gates (~20 million transistors) were developed but the power dissipation exceeding 8 Watts was a limiting factor to integrate more functions even if the technology would have allowed in theory up to 8 million gates per device.

Special techniques were deployed to cool down the ASICs and maintain their junction temperature at an acceptable level, which would have otherwise compromised reliability and lifetime. In the case of Inmarsat XL a special AlN (Aluminium Nitride) package [3] was developed to dissipate the power that a standard ceramic package would not have managed (Figure 1).

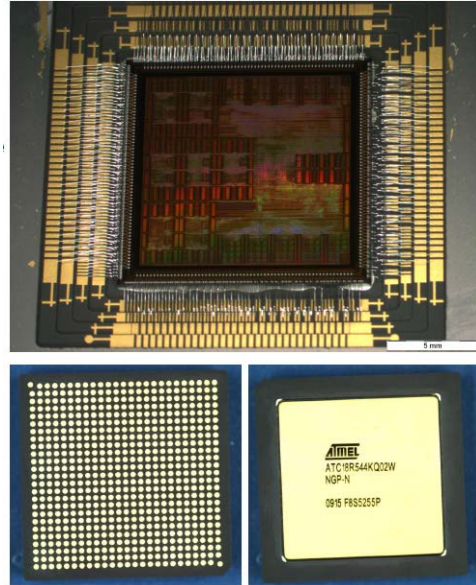


Figure 1: Astrium / Inmarsat XL ASIC and Aluminium Nitride package(AIN)

The number of pins available on the package was also another issue. Indeed the increasing clock rates (~ 300 MHz), internal but also external, generated by analog to digital (ADC) and digital to analog (DAC) converters for instance, required the demultiplexing of the data paths by a factor of 2 or 4 to lower the clock rate and hence reduce the power dissipation. As a consequence of the demultiplexing and clock rate reduction (150 or 75 MHz), the number of LVDS I/Os and associated internal data paths increased as well by a factor of 2 to 4. Those constraints translated in the need of having a new package with a higher number of pins. An AlN package with 625 pins was then specifically developed in the frame of Inmarsat XL program.

The solution hence adopted by Astrium was able to cope with the stringent requirements for more power dissipation and higher pin count. This development was challenging in the sense that it represented a big leap from previous package solutions limited to ~ 480 pins; new associated printed circuit board assembly techniques (PCB) had to be tested and qualified.

In telecom payloads, “clos network” ( architectures are often used to ensure a full connectivity between ASICs. This full connectivity involves hundreds of Gbps links from ASICs to ASICs and ASICs to data converters (ADCs / DACs).

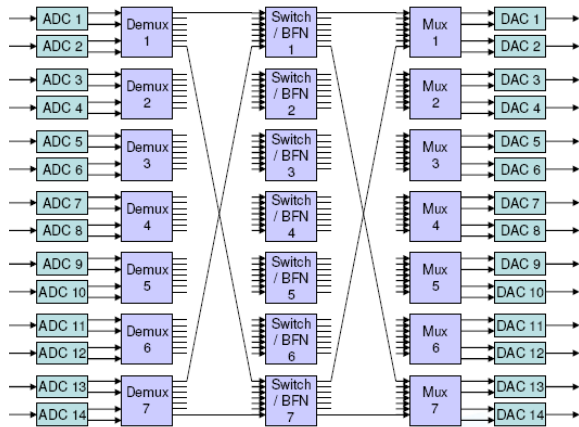


Figure 2: Astrium / Inmarsat XL Clos network architecture

Today's limits have been reached with European state of the art ASIC technologies (180 nm); parallel synchronous buses using LVDS buffers for instance are limited in speed to ~ 200 Mbps requiring therefore a high level of parallelization to reach the Gbps throughput. In some cases like digital beam forming payloads (Inmarsat XL) [3], synchronicity had to be maintained within the payload and between all ASICs. Therefore complex calibration mechanisms based on plesiochronous techniques using FIFOs were deployed to compensate the various delay paths between ASICs. Putting those elements together, more LVDS buffers due to parallelization and extra logic to compensate delays, resulted in extra complexity / mass meaning at the end additional power consumption. In telecom payloads every Watt lost in anything other than transmission represents a pure loss of revenue from the Operator point of view. To tackle those issues and make digital telecom payloads more efficient than their analog competitors, ASIC technologies had to be pushed further ahead. All those considerations led to ESA "Deep Sub Micron" program (DSM) launched in 2008 and based on ST 65nm technology node (CMOS / bulk) [4].

### III. DEVELOPMENT OF A NEW RAD HARD 65nm TECHNOLOGY AND ASSOCIATED CHALLENGES

When launched in 2008 the objective of the DSM program, in partnership with ST Microelectronics (Grenoble, France), was to bring an answer to the challenge for higher integration, higher data rates, higher pin count and better power efficiency. The specifications at that time were aiming at an improvement factor by 4 with respect to integration

capacity compared to ATMEL(F) 180nm ATC18RHA [2].

Therefore the new Rad Hard 65nm ASIC technology had to offer a capacity of ~ 30 million gates (120 million transistors) and also a higher data clock rate of ~ 400MHz. But higher integration and higher data rates would mean little without efficient interfaces. That is why from the very beginning of the DSM program high speed serial links interfaces (HSSL) were identified as a key element to support the Giga bits or Tera bits of data processed per ASIC and overcome the bottlenecks that the limited number of IOs represented. Moving from a conventional paradigm where data were transmitted over synchronous parallel LVDS buses limited to ~ 200 Mbps per lane to a new paradigm where data were serialized and transmitted asynchronously at a very high speed, 6.25 Gbps, was a major leap. The 6.25 Gbps rate, stands from the fact that each 10 or 12 bits ADC-DAC sampling at 1.5GHz, generates after 8b/10b encoding a throughput of 18 to 22 Gbps. DSM 65nm ASIC technology cannot accommodate such a data rate over one single lane. The maximum achievable rate today is 6.25 Gbps per lane, requiring therefore the aggregation of 4 HSSL lanes to accommodate a 18 or 22 Gbps data rate.

The evolution from parallel busses to high speed links had to be accompanied as well by a change in packaging technologies; the classical wire bonds solutions had to be replaced by flip-chip. Flip-chip techniques allow higher pin count while minimizing package parasitic (RLC) and making then possible the use of very high-speed interfaces (6.25 Gbps). Despite better efficiency thanks to Giga bits serialization, future demanding applications such as broadband telecom payloads clearly show that the number of useful IOs (data) will exceed 800, resulting therefore in flip-chip packages that will exhibit more than 1600 pins. The rationale for this impressive number of pins is linked to the fact that 40 to 50 percent of the pins are needed for power distribution and test. Indeed in the 65nm technology the core will be supplied with 1.2V and IOs with 2.5V, while the overall power dissipation per die will exceed 15W or 20W. Lower voltages with lower margins (ripples) and higher power mean higher currents and potentially higher voltages drops. To mitigate this risk a larger number of pins dedicated to the power distribution will be added. Therefore, overall, the number of pins per package may drastically increase due to power and signal integrity considerations. Such a package will materialize in a 40x40mm<sup>2</sup> package exhibiting 1600 pins with a pitch of 1mm. The die itself may not exceed 1cm<sup>2</sup> while

offering an integration capacity of 30 million gates for high end applications (telecom). Future telecom needs also show that more than 16 HSSL per die will be needed resulting in 4 ADCs or DACs per telecom ASIC. Those HSSL macros and associated pins will be pre-placed and routed for signal integrity reasons. The entire path starting from the layout of the HSSL IP until the package pin / ball will have to be carefully designed to ensure 6.25 Gbps data rate performances. Another important aspect regarding space packaging is hermeticity. Hermetic packages have been used so far for conventional ASIC technologies (180nm, 350nm). But the introduction of flip chip technology for DSM to satisfy the needs for higher pin count and higher data rates has led at the same time to larger package sizes (40mm x 40mm). Can hermeticity with such a package size be achieved? How 15W to 20W can be dissipated and drained from the top of the package? All those questions will be addressed in a new ESA EC13 activity (European Component Initiative Phase3) intended mid-2012 [5]. This new development will certainly have to align and get inspiration from the recommendations made by the QML-Y working group [6] led by NASA, Space Corporation with ESA participation.

Regarding the Rad Hard standard cells ASIC library development, several steps have been reached in the completion of the DSM Phase1 activity (KIPSAT) [7]. A set of cells have been designed and prototyped thanks to CNES support. Also a quad high speed serial link device has been prototyped (Quatuor) [7]. Both devices have undergone radiation test campaigns showing that enhancements related to latch up and flip-flop's hardening were still possible. Those first test vehicles, library and HSSL (Quatuor), helped to establish a preliminary "cartography" and to better define where efforts had to focus. As lessons learned from this first return on experience, the CAD flow has been enhanced to better check latch up protections and to ensure that Deep N Well insertion (DNW) systematically covers all critical areas. New Rad Hard flip flops and clock tree buffers have been designed exhibiting better performances with respect to SEU rate while minimizing speed, area and power penalties with respect to standard non hardened flip flops.

Moreover this Space Library is sustaining 20 years ageing models and  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Tj. Main failure modes have been implemented for 65nm Design in Reliability (DiR) models, and thus reliability targets can be addressed at CAD level.

At the time of writing this article the new Rad Hard library cells have been validated under simulations only. A new library test vehicle is being

manufactured and planned for Q2-2012. The radiation test campaign and reliability tests are planned in Q3-2012 in order to characterise the design/simulation models.

The final library offer will include a set of three hardening levels. A first non-hardened set of cells (~ 800 cells) directly extracted from the commercial offer will be latch up protected but no special hardening is foreseen regarding SEU or SET. Those cells will be used wherever speed, area and power optimizations are needed but where radiation hardening is less critical. Typically those cells could be used in DSP data pipelines where erroneous data are anyway flushed after several clock cycles or corrected by on ground equipment thanks to special coding techniques (Reed Solomon, Viterbi, turbo codes, LDPC). A second set of medium hardened cells will be available (~ 70 cells). Those cells will offer a compromise between hardening (SEU rate x100 better) while keeping the same speed and minimizing area and power penalties to 70% with respect to their non-hardened equivalent (commercial cells). Finally a third set of cells (~ 70 cells) will target high hardening level (SEU rate x250 better) at the expense of 50% penalty in speed [8]. The final user will have the choice to combine those cells together in order to harden the design where needed and choose between medium or high hardening according to the mission profile. The new 65nm Rad Hard library [7] will therefore allow trade-offs between speed, area, power and hardening. Should higher hardening be needed the designer, could still combine the flip flops in a TMR approach at the expense of higher area and power penalties (x3.2) [8].

#### IV. FUTURE DEVELOPMENTS AND PERSPECTIVES

DSM 65nm technology and HSSL will be key enabling elements to open new horizons for a set of demanding applications. Among those applications, telecom might be the first to benefit from advanced integration and miniaturization progress. The availability of a 65nm space technology should enable the emergence of a new class of telecom satellites, more agile and more versatile [9]. When procuring a satellite system, for 15 or even 20 years lifetime, telecom operators have difficulties to predict how the data traffic and service demand will evolve over that period.

Therefore more system flexibility is desired and this will be introduced thanks to, for example, more antenna beam flexibility. Multi beam antenna systems [10][11] built upon hundreds of sub beams

will have the ability to adapt with a fine granularity to the geographical and time traffic evolution.

Future telecom satellite systems will support as well multi role missions and will for instance broadcast HD TV services and offer point to point services, internet or mobile telephony. To guarantee those multiple services, a better on-board power management is needed in order to allocate dynamically more or less power to the beams according to traffic demand.

This fine power management will be enabled thanks to a new class of broadband digital beam forming satellites systems [12][13]. More power will be allocated to sub beams where traffic is higher. Beams might also be shaped and steered in such a way that they may adapt to geographical constraints or avoid interference due to frequency reuse. Complex multi beam antenna systems [10][11] will also require very accurate and adaptive optimizing techniques to minimize link losses and again optimize on-board power.

The emergence of this new class of broadband digital beam forming satellites will be conditioned by the availability of the DSM 65nm technology. The demanding requirements set by those new payloads, cannot be fulfilled with the existing state-of-the-art digital technology for space application (ATMEL 180nm), nor by analog RF payloads that may potentially offer alternatives from a power consumption point of view but will certainly not bring the flexibility or versatility offered by digital beam forming payloads [12][13].

Other satellite programmes such as Earth Observation or Scientific missions will also benefit from DSM 65nm with more powerful microprocessors and DSP processors. In Q1 2010 the Next Generation Multipurpose Microprocessor (NGMP) [8] activity was kicked off. This new activity aims to develop a much higher processing component that will add to the family of existing microprocessors and SoC based on the LEON II / III space microprocessors [8] while maintaining compatibility with Sparc V8 architecture. The current single core LEON architectures can only deliver 80-100 MIPS but the new multi core processor (NGMP), planned as a quad LEON4 core, will aim at more than 300 MIPS. Such a level of performance can only be reached with the availability of a DSM 65nm technology.

Space Fibre is another field of application that may benefit from space DSM advances. Space Fibre will be the successor of the current and well known Space Wire [14], a high speed serial link offering today a peak transmit rate of ~ 400 Mbps. Those limitations

in speed are conditioned by the performances of the LVDS drivers in ASIC libraries 350nm and 180nm used to implement the Space Wire transceivers. Tomorrow those limits might be overcome by the use of the DSM 65nm space technology. The new Space Fibre transceiver will exhibit 6.25 Gbps data rate for a power that may not exceed 150 mW.

Another potential application for the DSM is the high density SRAM based European FPGAs. The availability of the 65nm technology coupled with HSSL (6.25 Gbps) and FPGA fabric is hoped to enable the design of a full European high density reprogrammable FPGA for space. This reconfigurable FPGA platform will allow the integration of multi million equivalent ASIC gates, presenting functional capabilities very similar to the well-known Xilinx technology. The amount of FPGAs embedded in satellite systems tends to grow from year to year. Because differences in performances FPGAs will most likely never replace ASICs entirely, but surely FPGA usage will stay at a very significant percentage of the total number of custom integrated circuits used on board.

Now, if we project ourselves in a longer term future which type of applications could we envisage thanks to DSM technology? Definitely massive parallel architectures and Network on Chip (NoCs) will be the answer.

## V. CONCLUSIONS

The DSM 65nm Rad Hard ASIC technology based upon ST process represents a major undertaking and challenge for European space industry. It will enable the design of disruptive applications such as, broadband telecom payloads, multi cores microprocessors, high density FPGA, complex system on chip (SoC) and network on chip (NoC). DSM 65nm represents a major leap with respect to previous ASIC technologies for space (180nm). Therefore DSM 65nm is strategic to maintain Europe competitiveness, non-dependence and innovation. Year 2012 will see the early deployment of the Space 65nm Design Environment. A first "Alpha version" released by ST in Q2-2012 will be restricted to "advanced users". A second deployment phase, "Beta version", in partnership with ATMEL(F), is foreseen in Q4-2012 and will be open to a larger number of customers. In parallel new development activities funded by ESA and CNES will continue, aiming at completing the final library offer, validating a flip chip package solution, qualifying the technology and also strengthening the recent partnership ST-ATMEL(F).

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