PDFE: A PARTICLE DETECTOR FRONT-END ASIC

J. Wouters, S. Redant, K. Marent, C. Das,*
S. Habinc, B. Johlander, T. Sanderson**

IMEC (Interuniversity Micro-Electronics Center), B-3001 Leuven, Belgium
Tel: +32-16-281 250; Fax: +32-16-281 584; e-mail: jan.wouters@imec.be

***** ESA (European Space Agency), Postbus 299, NL-2200 AG Noordwijk, The Netherlands***
Tel: +31-71-565 4722; Fax: +31-71-565 4295; e-mail: sandi@ws.estec.esa.nl

ABSTRACT

This paper describes a low power low noise mixed analog-digital PDFE (particle detector front-end) custom chip developed by IMEC for ESA and intended for scientific energetic particle space born instrumentation (spectroscopy). The ASIC (application-specific integrated circuit) is designed in a standard 0.7-µm CMOS process. The chip comprises a charge sensitive amplifier, a semi-gaussian pulse-shaping amplifier, a peak detector, a discriminator, an 8-bit ADC and control logic. A second channel is provided for (anti-)coincidence purposes. For cost reasons the circuit is made as versatile as possible by providing several digitally programmable configurations. ENC (equivalent noise charge) is 800e [illegible] µs. Conversion gain is 30mV/fC and full scale input is 0.1pC. Power consumption is 50mW when all blocks are enabled; power supply is 5V. The die area measures 31mm². A baseline shift of 15mV is realised at 250Ksamples/s (this is the maximum counting rate) for inputs limited to 2.5fC and at 25Ksamples/s for full scale inputs. Radiation hardness is implemented both at the transistor level and at the architectural level. Table 1 lists the main specifications.

I. INTRODUCTION

The increasing demand to lower the cost of space missions is a driving force for size and power reduction. This is why ESA (European Space Agency) is developing a chipset for particle detection front-end and back-end electronics. The back-end is based on an 8052 microcontroller and both masters the system and takes care of the data generated by the PDFE. The PDFE, which is designed by IMEC (Interuniversity Microelectronics Center), is the front-end of the system and is discussed in this paper. Another advantage of monolithic solutions is an increased reliability, provided the chips are well screened and tested.

Bipolar technology is generally considered to be less noisy and more radiation tolerant than CMOS. However, it is shown in [1] that CMOS allows a better noise performance than bipolar. Other advantages of CMOS are lower power consumption, larger industrial availability, both at the design level and at the manufacturing level, and the ease to implement digital functions. CMOS then was the natural choice for this design. In standard CMOS technology all circuits have a common substrate, hence special attention was paid to reduce the feed-trough of digital noise to the analog blocks. Precautions at the design level are taken to protect this CMOS device against space radiation.

Because of the high NRE (non-recurring engineering) and development time, multi-functionality is build-in as much as possible by implementing several operating modes. These modes can be selected through a serial link. This link also allows to cascade several ASICs, allowing easy scalability and hence further enabling the use of the PDFE in various instruments. Finally the link allows to set the discriminator levels. Blocks that are not used in certain operating modes are powered off, minimising power consumption.

The paper is organised as follows. In section II the PDFE architecture is presented. Section III discusses the building blocks. Section IV explains the radiation precautions. Sections V and VI present simulations and measurements respectively. Conclusions are drawn in section VII.

II. ARCHITECTURE

A block diagram is depicted in fig. 1. The PDFE performs all required analog signal processing up to the analog-to-digital conversion. The analog chain essentially consists of a charge sensitive amplifier (CSA), a pulse shaping amplifier (PSA), a baseline restorer, a peak detector, a discriminator and an 8-bit ADC. A classAB buffer is provided to both drive the ADC and to get the analog pulse off chip.

Incident particles generate a charge pulse on an external reverse biased detector diode. This charge pulse is integrated by the CSA, resulting in a fast-rising voltage step, and is then shaped into a semi-gaussian pulse by the PSA. The PSA is actually a bandpass filter and increases the signal to noise ratio of the chain. The amplitude of the pulse is a measure for the charge and hence for the energy of the detected particle. The peak detector holds the maximum value of the pulse which is then converted by the ADC. The discriminator, which is a fast comparator, detects the occurance of an event by comparing the output of the PSA to a detection level. This level is programmable through the serial link and is generated by an on chip 8-bit R-2R digital-to-analog converter. A predefined time after event detection, making sure that the peak detector has captured the peak of the pulse, the ADC performs one conversion. The peak detector is then

reset and the system is ready to accept and process the next pulse. The peak detector does not require a digital input for switching to hold mode, greatly improving the peak detect accuracy.

It was found beneficial to include the ADC on the chip to minimise system complexity, important for a space born instrument.

The digital part implements the 32-bit serial link and handles these 32 bits. These bits select the required operating mode, set various controls, contain PDFE status info (to be read out) and set the discriminator level. The digital part also contains a parallel link to read-out the ADC results. Finally it contains the timing logic to drive and synchronise the various analog blocks.

A 4MHz clock for on chip timing is needed. To minimise clock-induced noise, the PDFE incorporates a crystal oscillator, the active circuit being on chip. This solution was preferred above the distribution of a clock signal at board level. For the same reason, TTL levels are used for digital I/O pins that are active during analog processing. Also, these digital outputs have extended rise and fall times.

The PDFE is completely event driven, again to keep the digital noise to a minimum. Out of the 1500 on-chip gates, only 30 flip-flops are continuously active. The remaining digital part and the ADC are kept quiet until the discriminator flags an event and the peak detector has subsequently captured the corresponding analog peak value.

III. Circuit Description

A. Charge Sensitive Amplifier

The CSA is implemented in a classical way: a folded cascode amplifier with capacitive feedback. To establish the DC operating point, a feedback resistor is used. This resistor is high–valued (20MΩ) in order to obtain the noise spec and is realised as a 50KΩ resistor, implemented in the high-ohmic polysilicon layer, and an MOS current divider. A source follower at the output of the CSA is needed to drive the 50KΩ. The CSA has a PMOS input transistor because, as is generally the case, the NMOS shows significantly higher 1/f noise in the chosen technology. Also, the PMOS is shielded from the substrate by his NWell bulk. A W/L of 10000 and a DC operating current of 1.8mA are required to obtain the noise spec.

B. Shaper

A Gm-C filter is used as described in [2]. The circuit is shown in fig. 2. A 1^{st} order low pass filter is followed by a 2^{nd} order bandpass. In order to cancel the pole due to the CSA reset, a zero is introduced in the shaper by adding resistor Rpz. Rpz is implemented in the same way as the CSA reset resistor to guarantee good matching between the pole and the zero. The vOutDC input sets the shaper's DC output.

C. Baseline restorer

Due to the shaper's DC gain being significantly bigger than 1, and due to device mismatches, the DC level (or the baseline) at the output of the shaper would show a significant random (this is varying from chip to chip) offset which would even be a function of conditions like temperature and biasings. This error is eliminated with a baseline restorer. Using an OTA (operational transconductance amplifier) in open loop and loaded with the R1-R2-C combination as shown in fig. 3, the difference between the shaper output and analog ground is amplified (DC gain = gm.R1) and low pass filtered (τ=(R1+R2).C). The result is fed to the shaper's offset tuning input vOutDC. Negative feedback assures that the output of the shaper is auto-zero-ed, with a residual and acceptable error being the offset of the OTA.

The function of the low pass characteristic of the baseline restorer is to limit the loop's reaction on the semi-gaussian pulses appearing at the shaper's output. The external capacitor C (100nF) together with the on chip resistors R1 and R2 (200KΩ) gives a cut-off frequency of a few Hz, and the frequency spectrum of the semi-gaussian pulses lies significantly higher. Differently said, this baseline restorer makes the *DC component* of the shaper output equal to analog ground. When pulses arrive at high counting rate and high amplitude, the baseline will still show a significant drift. However the high frequency gain (gm.(R1//R2)) is made that big that supply clipping at the output of the OTA removes a big part of the pulse but *without* removing the amplified DC error of the shaper's output. This clipping acts as an extra, non-linear, filtering and further reduces baseline shift due to pulses. Note that the time constant τ also assures loop stability by providing a dominant low frequency pole.

D. Peak detector S/H

A peak detector as described in [3] is used.

The detector continuously compares the content of its analog memory, a capacitor holding the until then maximum input voltage, with the current input voltage. If current input is bigger than memorised maximum, the capacitor voltage is updated. The memory is only reset after an A-to-D conversion.

An intrinsic problem results from current leaking into the capacitor. This current is a combination of MOS source/drain reverse biased diode leakage and MOS transistor leakage. A priori one cannot know the sign of this leakage current. A current that decreases the memory content is not that severe: when a peak of sufficient amplitude is

detected (discriminator), that peak is immediately A-to-D converted. A net leakage current in the opposite direction is however worse, because then the memory will drift until it saturates. Note that the discriminator is in parallel with the peak detector, and hence will not be triggered. To avoid this potential drift, an explicit current source is put in parallel with the memory. The current is small, but bigger as the to be expected leakage. The net current is then in the acceptable direction. Although the current is small, one would still see its effect during the A-to-D conversion. To solve this, the explicit source is switched off when a peak is detected and until the ADC has finished .

E. Discriminator and DAC

The DAC is a classical 8 bit R-2R design. Speed is not important, because the discrimination level is essentially DC. No active buffering is needed because the load is a CMOS comparator.

The discriminator is a time-continuous comparator. High speed (100ns) is required. The comparator must still resolve pulses that are only slightly higher (10mV) than the discrimination level. To realise these requirements, a technique described in [4] is used. The schematic is shown in fig. 4. Essentially, a differential stage is loaded with an inverter, and that inverter is, at zero differential input, set close to its threshold. Also, the voltage excursions of the differential stage output are minimum. This then results in a very fast detection of a comparator differential input signal.

F. Analog to digital converter

A study of several ADC architectures together with the accuracy, speed and power consumption requirements resulted in the selection of a subranging two-step flash structure [5]. The ADC runs at 250Ksamples/s. A 4-bit course conversion is followed by a 4-bit fine conversion. Both the coarse and the fine circuits consist of a resistive 4 bit ladder and 15 comparators. The coarse result is used to switch the fine ladder across the coarse resistor to be interpolated. The fine ladder is high resistive with respect to the coarse ladder in order not to distort the coarse resistors, but is still able to settle in the available time slot. No S/H (sample and hold) is provided because a hold function is performed by the peak detector.

The comparator is shown in fig. 5. The specified ADC accuracy is ½LSB. The target is 0.1LSB, which is 1.2mV. The offset of CMOS differential pairs can hardly be made smaller than 5 to 10mV (three-σ), hence an auto-zero technique is implemented which allows to reduce the offset to about 100μV.

The front-end of the comparator is based on principles described in [6]. A differential-out differential difference amplifier is used. The two differential inputs are the main input and an auxiliary input. The output is the result of both inputs. The main input has an openloop gain AM towards the ouput, the aux input has a gain AAux, and AM is significantly bigger than AAux. Auto-zeroing (or correlated double sampling) eliminates the offset of the main input. In phase 1 the input offset is compensated by a voltage generated at the auxiliary input by the feedback loop. This voltage is sampled at the auxiliary input at the end of phase 1. The result is an equivalent input offset which is equal to the offset of the main input divided by AAux (the offset of the aux input gets divided by AM, and is hence neglected). AAux is made significantly bigger than one, and hence a small input offset results. The sampling (MOS switching) results however in an error due to charge injection. This error is reduced by the factor AM/AAux when considered as an, equivalent, main input offset. A second reduction is realised by putting capacitors after the sampling switches, reducing the charge-to-voltage conversion factor. A third reduction results from the differential nature (both charge injections do match to a significant extend), and the common mode rejection ratio of the aux input. After phase 1, the input voltage is amplified and applied to the comparator backend.

The comparator backend is a classical clocked regenerative (or latched) comparator, resulting in a fast digital discrimination. The inputs are sampled at the start of phase 2, the comparison (regeneration) is done during phase 2. Because of the gain in the front-end, offset in this stage is unimportant. The phase 1 – phase 2 switching is repeated every A-to-D conversion, and the technique could only be applied because the comparators are not used continuous-time. The ADC accuracy is then expected to be dominated by the matching of the resistors of the two ladders.

A classAB opamp buffers the peak detector output towards the ADC. The opamp is also used to bring the semi-gaussian pulse off chip in the PDFE analog output mode. ClassAB here implies the ability to realise the required slew-rate with significant capacitive load but with limited DC power consumption. However, the resistive load at the opamp output should be minimum 100KΩ.

IV. RADIATION PRECAUTIONS

The space radiation environment makes special precautions necessary to protect the chip.

The digital part is protected against Single Event Upsets (SEU). This is done in several ways and on several levels. The digital library as provided by the silicon foundry (Alcatel Microelectronics) was screened: only the most robust (for SEU) cells 6(n)9r

field-oxide leakage and gate oxide threshold voltage shift. Critical devices are identified by adding to each NMOS transistor a parasitic NMOS modeling field-oxide leakage. Gate oxide threshold voltage shifts are covered by corner analysis, and supposing that for the limited number of devices needed for the project no worst case wafers will be used.

Latch-up is a general concern, but the silicon technology chosen uses a thin epi layer on top of a heavily doped and hence low impedant substrate. This makes the structures intrinsically robust for latch-up.

V. Simulations

Extensive mixed analog-digital co-simulations have been performed using the combination of eldo (a spicelevel simulator) and verilog. The Alcatel Microelectronics Made design kit based on Cadence tools is used. These simulations were necessary because of the many different operating modes and because the complex and event driven interaction between digital and analog circuitry. Also, at certain moments three independent clock regions are active, serial link – local oscillator – events coming in, further making the circuit operation cumbersome to analyse.

Fig. 6 shows simulation results of the nonlinearity of the whole analog chain up to the ADC input. Two curves are shown, the PDFE can accept both positive and negative charges (the sign of the charge is selected by strapping a digital input). The best straight line nonlinearity is seen to be better than 0.5LSB and 0.15LSB respectively.

VI. Measurements

The device is currently being characterised; no final results are yet available. A die photograph is shown in fig. 7. The PDFE is fully functional. Fig 8(a) shows the semi-gaussian pulse. Fig 8(b) shows the output of the peak detector and a digital output signaling the availability of the ADC results; the peak detector is reset a little bit earlier (A-to-D conversion finished). Both pictures also show the output of the discriminator. The ADC was characterised and the results are shown in fig 9; both INL and DNL are within ½LSB. The current evaluation PCB does not allow to measure the intrinsic noise of the PDFE as it is mainly intended to be as versatile as possible, compromising the noise performance. Boards to evaluate the noise are currently being made.

VII. Conclusions

A 5V low power low noise particle detector front end ASIC is developed. The device is fabricated in a standard CMOS 0.7-µm process. All required analog signal processing up to an 8 bit A-to-D conversion is implemented. The device implements various operating modes which are digitally selectable, making it suitable for different applications. Power consumption is 50mW. Maximum counting rate is 250Ksamples/s. The noise spec is 800e□□□□□□□□□□□□□□□□□□□□□□□ capacitance. Full scale input is 0.1pC.

References

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Detector capacitance	100 pF	Number of channels	2
Detector leakage	1 nA	ADC resolution	8 bit
Full Scale input	0.1 pC	ADC INL and DNL	½ LSB
Conversion gain	30 mV/fC	Power supply	5 V
Noise	800 e^- rms	Power consumption	15 mW / per channel
Peaking time	1 µs		ADC: 20 mW
Counting rate	250 Ks/s @ 2.5 fC	Ambient temperature	-40 to 65 °C
	25 Ks/s @ 0.1 pC	Technology	0.7-µm CMOS,
Baseline drift	15 mV		Alcatel Microelectronics
Nonlinearity	1 LSB	Package	64-pins quad flat package

Table 1. PDFE specifications.

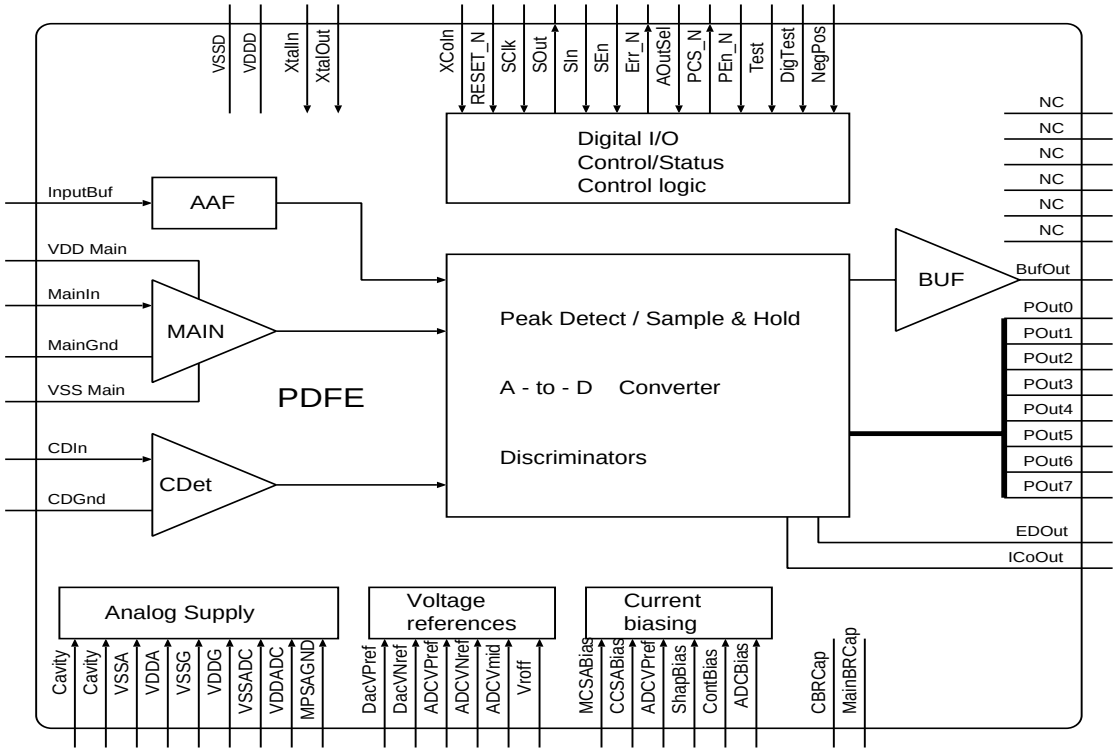


Fig. 1. PDFE blockdiagram.

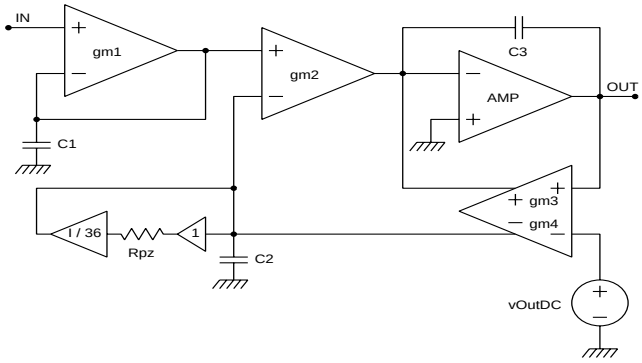


Fig. 2. Shaper (Gm-C filter).

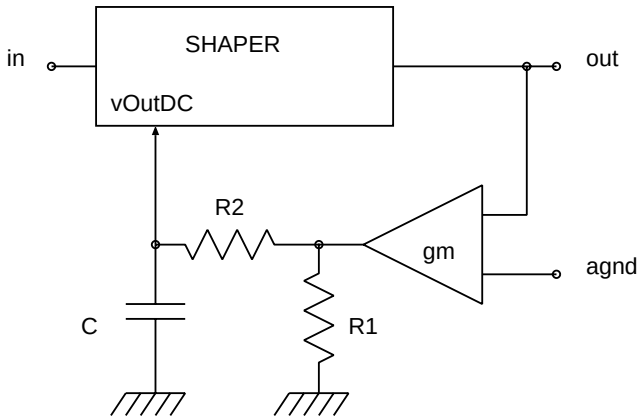
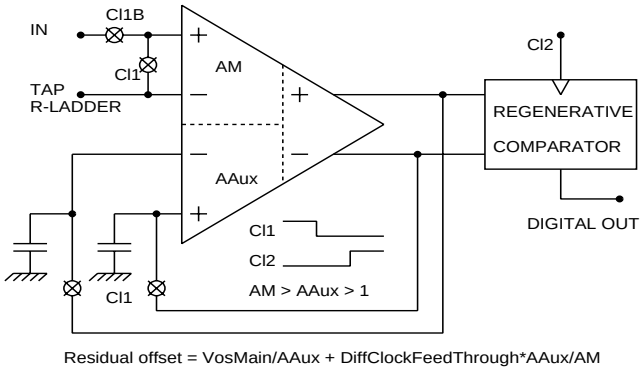


Fig. 3. Baseline restorer.



Residual offset = VosMain/AAux + DiffClockFeedThrough*AAux/AM

Fig. 5. ADC comparator: auto-zeroing & regenerative comparator.

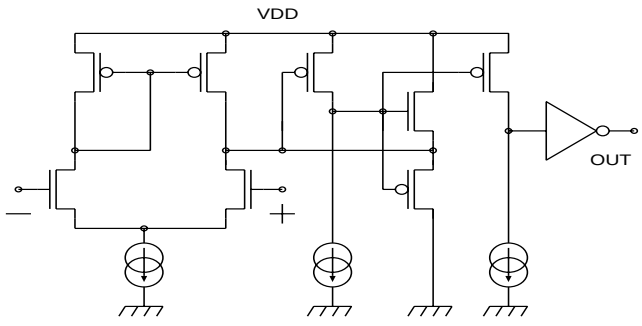
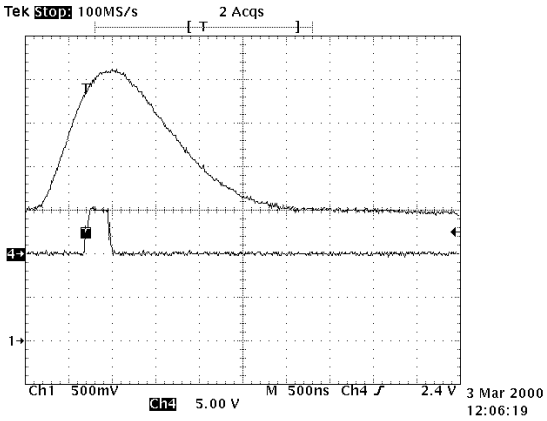
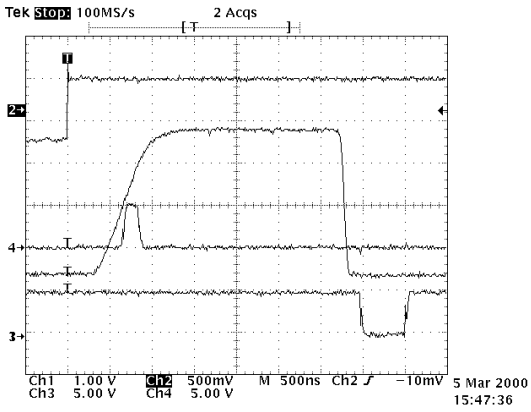


Fig. 4. Discriminator (comparator).



(a)



(b)

Fig. 8. Channel outputs: (a) semi-gaussian pulse, (b) peak detector and ADC active.

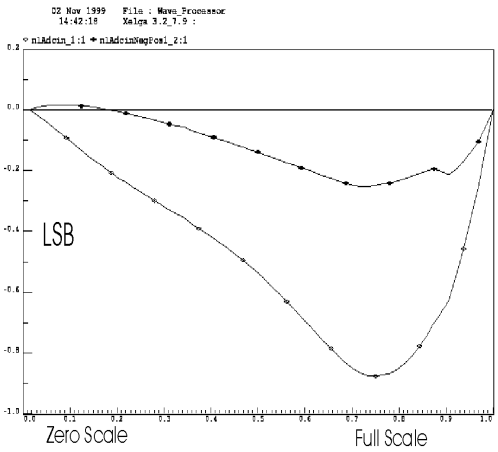


Fig. 6. Channel nonlinearity.

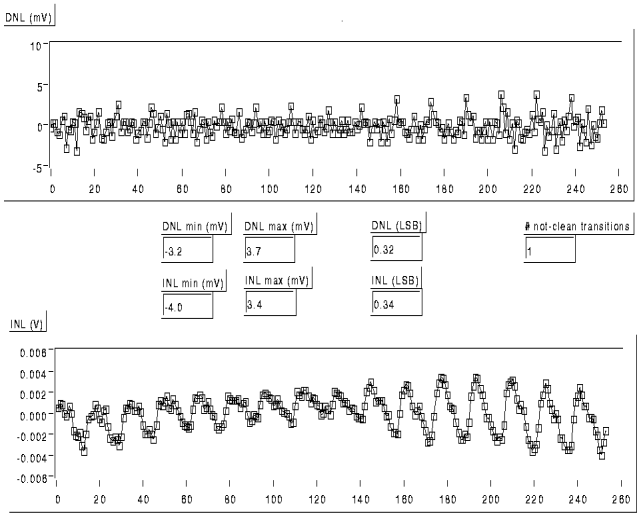


Fig. 9. ADC measurement results: DNL and INL.

Here comes a picture (still photo)
of the chip.

Fig. 7. Die photo.