

NGMP

QUAD-CORE NEXT GENERATION MICROPROCESSOR

WITH ON-CHIP SPACE WIRE ROUTER

Session: SpaceWire Components

Long Paper

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ABSTRACT

The Next Generation MicroProcessor (NGMP) is a quad-processor system-on-chip currently being developed by Aeroflex Gaisler in an activity commissioned and funded by the European Space Agency. Compared to earlier generations of European space processors, the NGMP design provides higher performance and places greater emphasis on support for both symmetric and asymmetric multiprocessing.

The design's features include four LEON4 SPARC32 processors, one SpaceWire router with eight external SpaceWire links and four internal AMBA ports, two 10/100/1000 Ethernet MACs, 32-bit 66 MHz PCI interface and DDR2-800 SDRAM main memory interface.

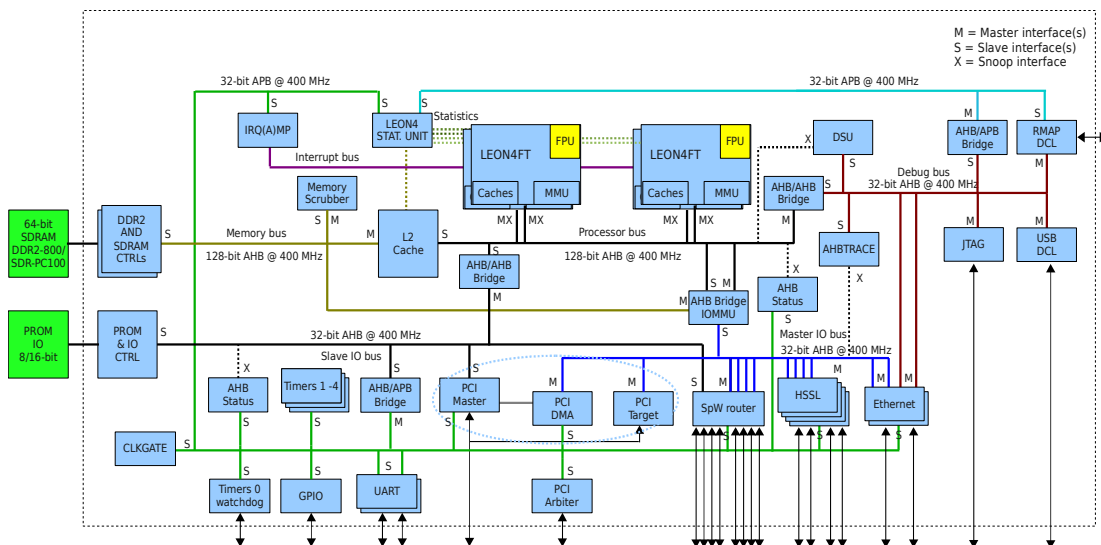


Figure 1: NGMP Block Diagram

The SpaceWire router allows the NGMP to act both passively and actively in a SpaceWire network. The target frequency for the NGMP device is 400 MHz. Preliminary results for this target frequency show that, using only internal routing, the architecture is able to sustain a data throughput of 1.5 Gb/s per SpaceWire AMBA port. In a scenario where the two full-duplex Ethernet links and all SpaceWire AMBA ports are run flat out, the sustainable throughput is roughly 1.5 Gb/s per Ethernet link and 1 Gb/s per SpaceWire AMBA port. In addition to this the SpaceWire router will also be able to simultaneously route packets at maximum speed.

NGMP is part of the ESA roadmap for standard microprocessor components, and it will be commercialised under fair and equal conditions to all users in the ESA member states. It is fully developed with manpower located in Europe, and it only relies on European IP sources. It will therefore not be affected by US export regulations.

A preliminary datasheet and further information can be obtained from:
<http://microelectronics.esa.int/ngmp/>