ASIC and FPGA for space applications: technology and strategies to counteract radiation effects

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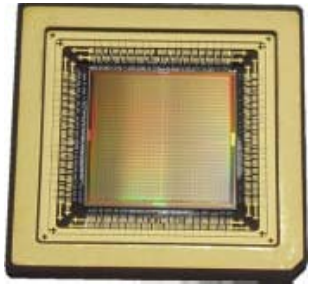
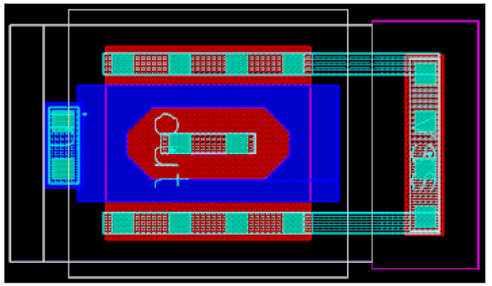
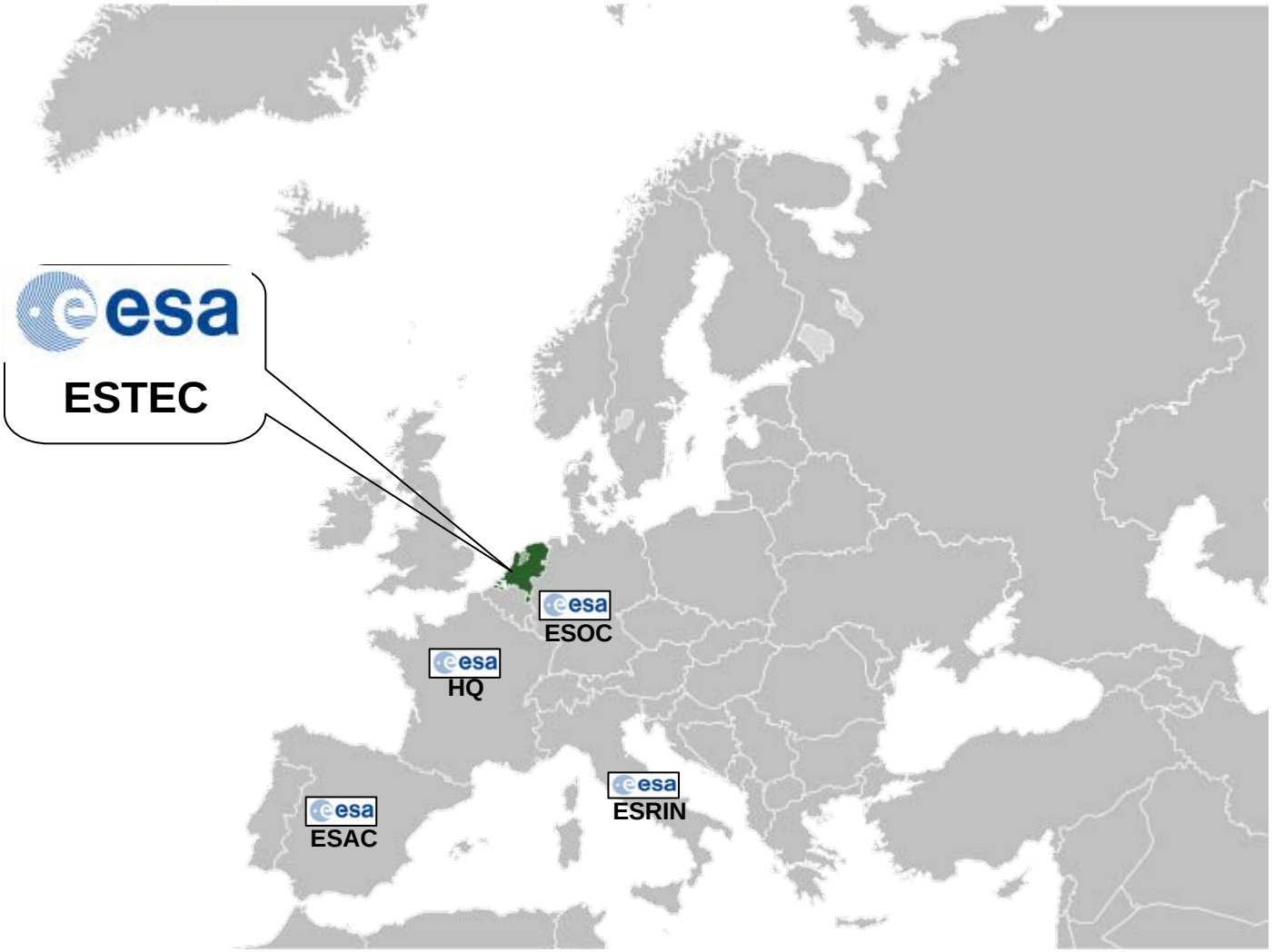



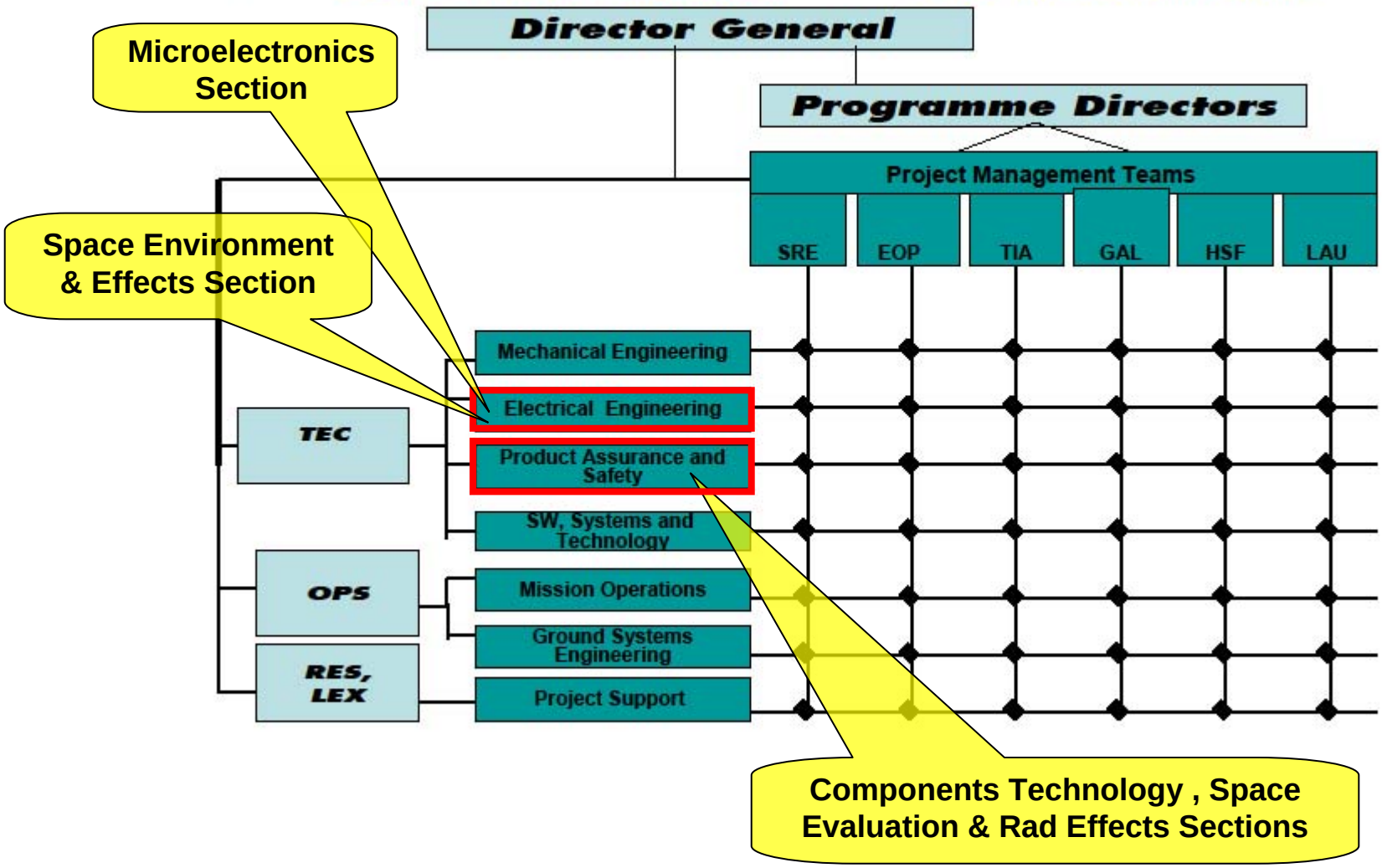
Outline

- Microelectronics & Rad Effects groups in ESA
- Why are radiation effects a concern?
- Radiation environment and effects on ICs
- Countermeasures (two examples, STMR and RHbD libs)
- ESA activities for rad hard ASIC and FPGA solutions
- Space FPGAs
- Validating Mitigation Techniques (one example: FT-UNSHADES)
- Summary

ESTABLISHMENTS

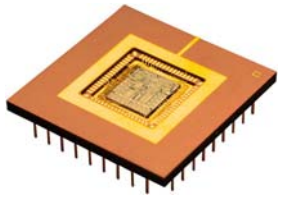


ESA Matrix Structure



Why radiation effects in ASICs and FPGAs are a concern?

unprotected



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can be

- temporary or permanent IC malfunctions

- risk of mission failures or loss

- on-board IC replacement or repair not an option

Radiation propagating EFFECTS

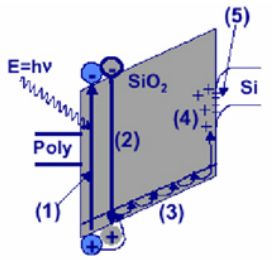
effects in semiconductor elements

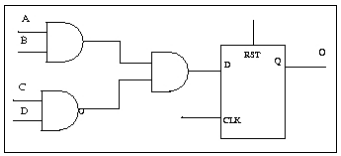
effects in basic analogue and digital cells

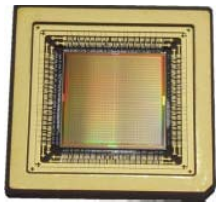
failing devices, components

failing units, sub-systems

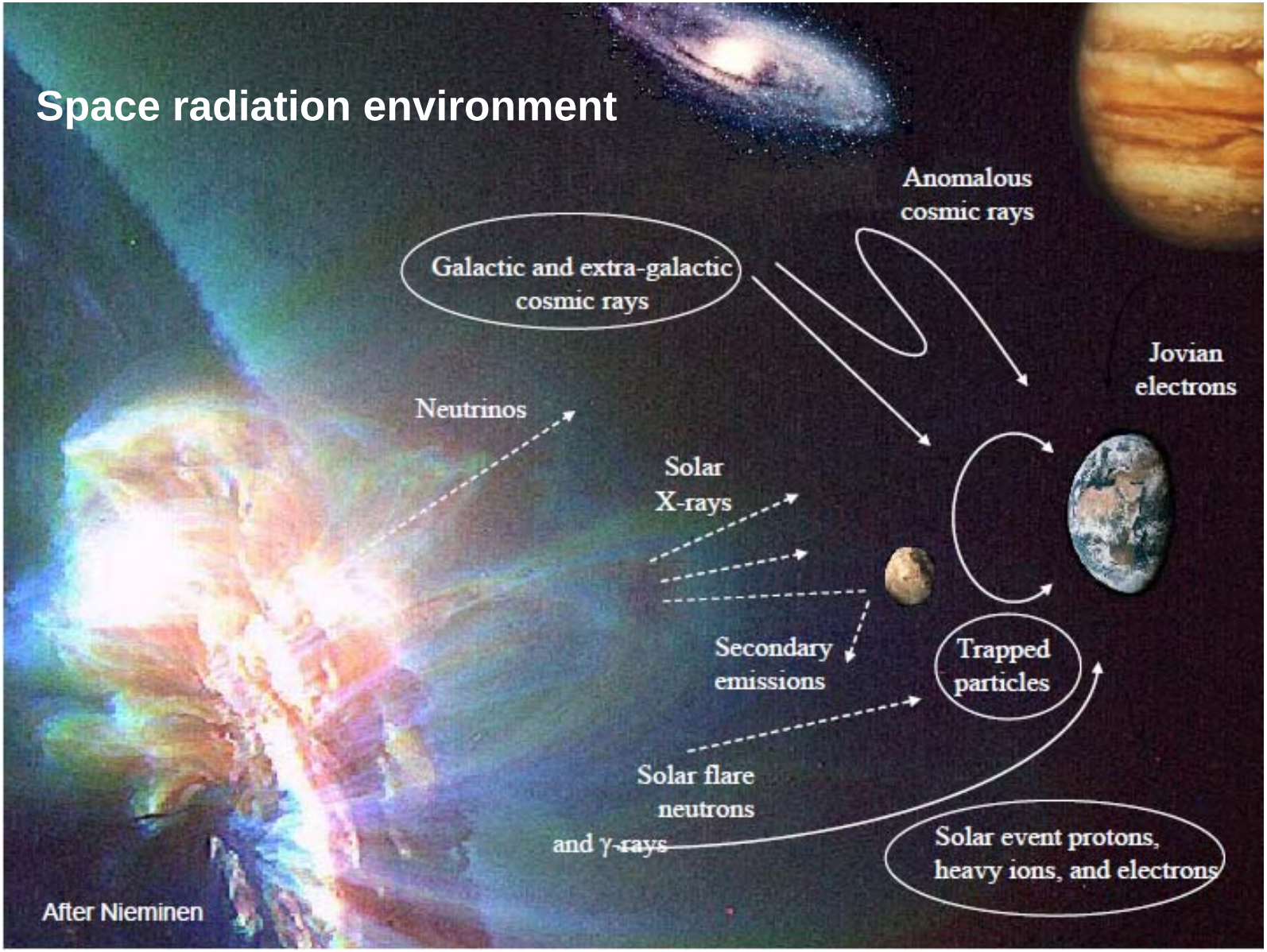
failing onboard experiments, spacecrafts!!







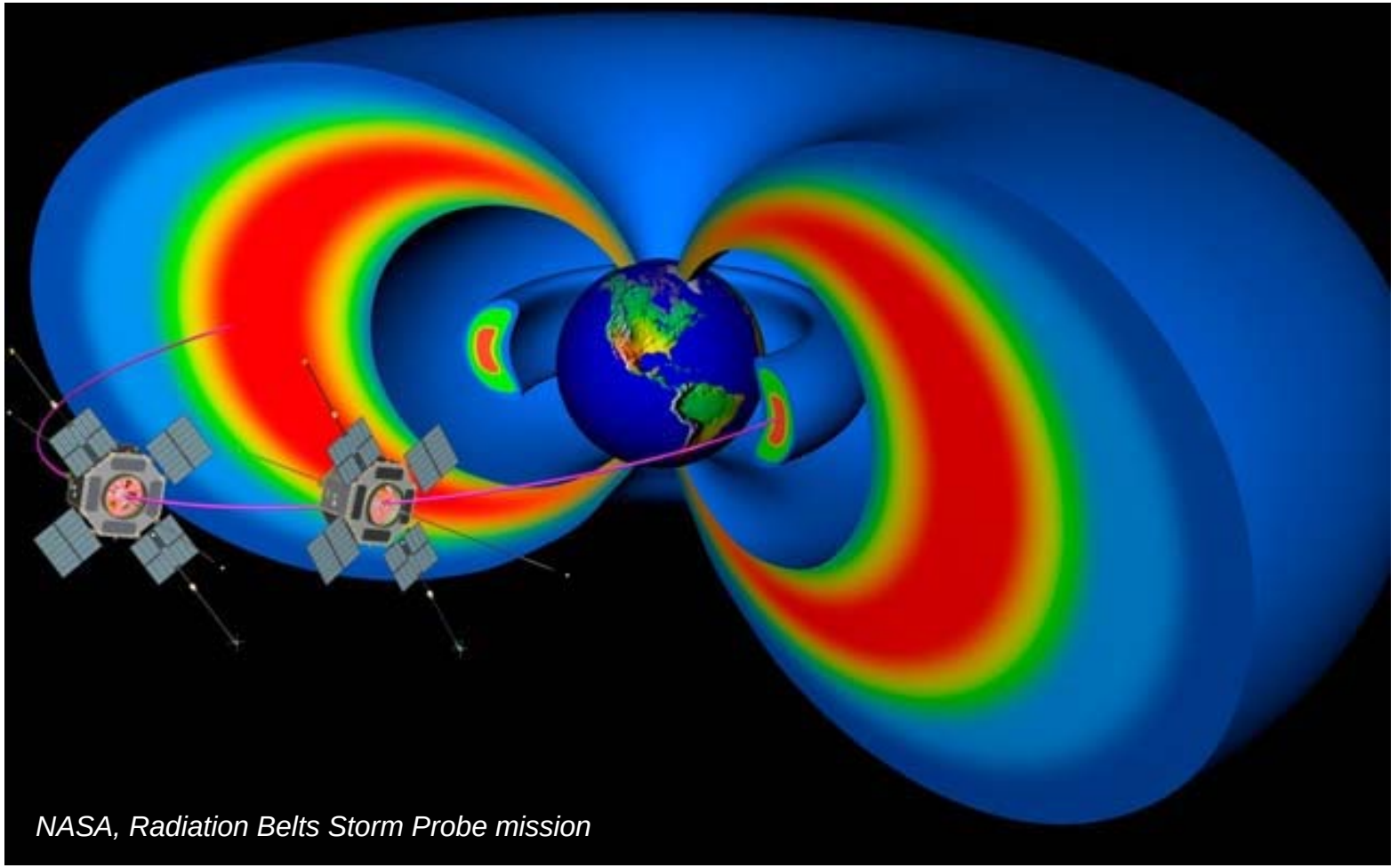
Space radiation environment



Trapped radiation: the Van Allen Belts

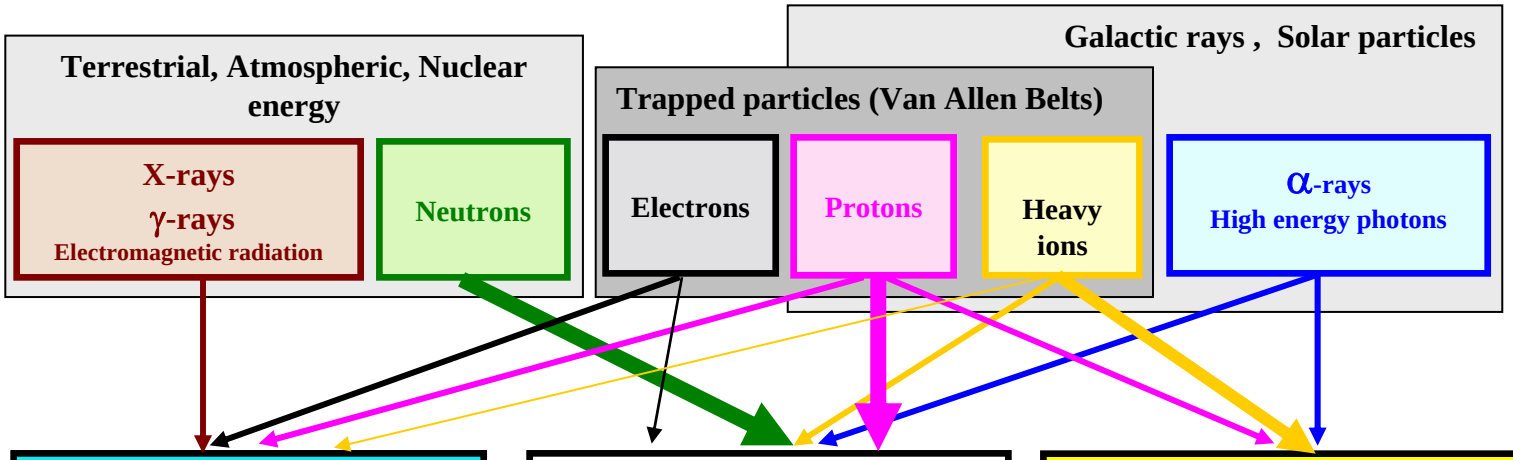
• Discovered during first space missions.

• **Electrons** and **protons** trapped in Earth Magnetic field (Lorentz force)



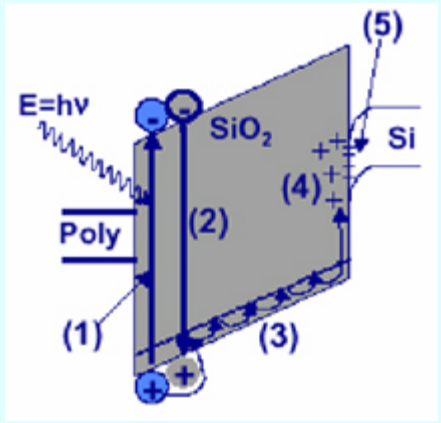
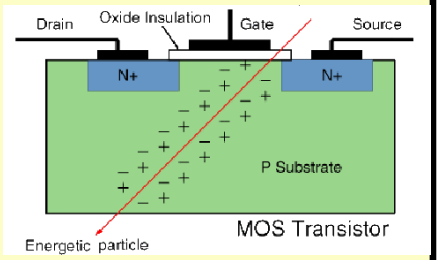
NASA, Radiation Belts Storm Probe mission

Radiation Effects in semiconductor devices



	TOTAL IONISING DOSE EFFECTS	DISPLACEMENT DAMAGE EFFECTS	SINGLE EVENT EFFECTS
♦ effects in semiconductor elements	♦Creation of electron-hole pairs ♦Charge build-up, excitation, transport →Threshold voltage negative shift in n-channel →Threshold voltage shift in parasitic transistors in bulk or thick epi layers →Reduction of mobility in channel conductance and transconductance	♦Atomic dislocation, nuclear displacement in lattice ♦Reduction in mobility ♦Reduction in carrier concentration ♦Increase in dangling bonds / free radicals ♦Increased defect concentration ♦"rapid annealing" of minority carrier lifetime ♦More defects, accelerated aging (shorter life time)	♦Local Ionisation (volume effects) →**Single Event Latch-Up (SEL)** activation of parasitic npnp/pnpn structures causing anomalous switching behaviour of main transistor and large draw currents. Possible permanent failure. →**Single Event Upset (SEU)** temporary "bit-flip" in memory element caused by internal charge deposition →**Single Event Transient (SET)** transient current or voltage spike. If propagated and latched by memory element, may result in "bit-flip" →**Single Hard Errors (SHE)** such as gate/dielectric rupture, burn-out, in high V junctions transversed by heavy ions
→effects in basic analogue and digital cells	→Increase of standby / off-state / leakage current →changes in circuit parameters: operating point, gain, impedance, drive	→changes in circuit parameters: operating point, gain, impedance, drive	

Rad Effects in ASICs and FPGAs

TOTAL IONISING DOSE EFFECTS	DISPLACEMENT DAMAGE EFFECTS	SINGLE EVENT EFFECTS
	Typically this only concerns **electro-optic sensors, diodes, opto-couplers, solar cells, wide-base bipolar transistors**	
➢ **POWER CONSUMPTION INCREASE** ➢ **DEGRADATION OF ANALOGUE FUNCTIONS / PERFORMANCE**		➢ **TEMPORARY OR PERMANENT MALFUNCTION** ➢ **LOSS OF DATA** ➢ **POWER CONSUMPTION INCREASE** ➢ **DEVICE BURN OUT**

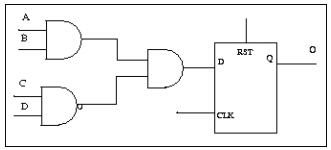
⟶potential effects at ASIC or FPGA level

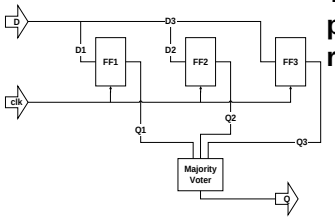
Rad Effects in ASICs and FPGAs: Countermeasures (1/3)

How to classify them?

WHO implements them?

- system HW and SW designer
- IC designer (IC Design Kit user)
- IC design (CAD) tools developer
- IC library / Design Kit / layout designer
- Foundry process & manufacturing engineer



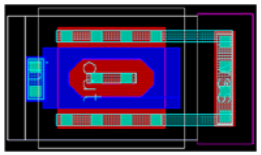


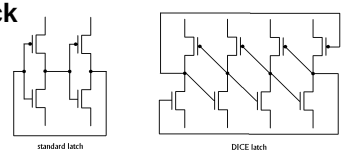
TMR, EDAC, parity, time redundancy

Power cycling

scrubbing, TMR, current limiters

Enclosed transistors, hard FF, hard clock trees

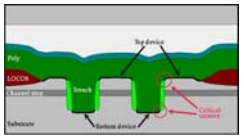


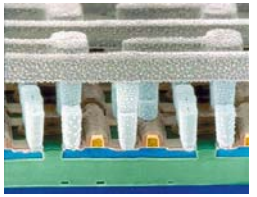


At which **LEVEL** are they applied?

- system (PCB, software, case)
- IC architecture (netlist)
- logic cell, layout level (libraries, reset/clock lines)
- foundry process (wafer substrates, conductive, dielectric and isolating materials and sizes)

SOI, epi, thin OX, wells, STI, guardbands





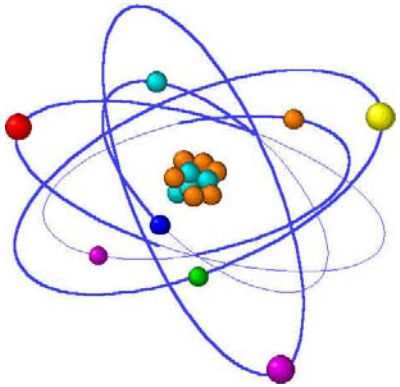
Rad Effects in ASICs and FPGAs: Countermeasures (2/3)

Which **EFFECTs** do they counteract?

Level	Radiation effect mitigation technique	TID	SEE		
			SEL	SEU (or sampled SET)	SET
System	Temporarily remove and re-apply power supply ("**power cycling** ") to eliminate "microlatch" or non-destructive latch-up condition.		X		
	Apply **reset** to "persistently flipped" memory elements			X	
	External leakage **current detection and protection** (current limiters) for latch-up in sensitive devices	X	X		
	Fault detection and Reconfiguration / systematic scrubbing (RAM based architectures)			X	
	HW or time redundancy at system level (for voting or reconfiguring)		X	X	
	Cold-sparing & Hot swap	X	X		
Structure	**Aluminium Shielding**	X	X	X	X
Wafer process	**SOI** processes	X	X	X	X
	thin epi over heavily doped substrates	X	X		
	trench isolation / p+ guard rings around NMOS transistors	X	X		
Cell Layout (RHBD)	Hardened libraries: **edgeless transistors, capacitive and resistive hardening; guard bands or equipotential source and/or drain regions,** Part parameters **de-rating** to reach immunity to expected degradation (i.e. drain-to-source voltage), **redundancy and feedback** at transistor level	X	X	X	X
Netlist design	EDAC: **parity, checksums, codes** ; fault masking: **TMR, Hamming/cyclic codes**, dead-lock-free **FSM /Counter hardening**			X	X

Rad Effects in ASICs & FPGAs: Countermeasures (3/3)

What are the **COSTS / DRAWBACKS** of rad effects protections?



-More Silicon area, less integration

-Lower speed

-More weight

-Higher power consumption

-higher design complexity, longer development times

-Export constraints dependencies

-Higher technology prices (special=expensive components, tests and tools) !!

Rad protection can have a high price, but the cost of loosing on-board experiments or the entire satellite is much higher !!

ESA activities to make rad hard ASIC/FPGA solutions available

1. **Handbook on Mitigation Techniques**
2. **ASIC Rad Hard libraries based on commercial processes**
3. **IP Cores service**
4. **Standard processors and ASICs**
5. **Space Multi-Project Wafer programme**
6. **Radiation Effects in Deep Sub Micron (DSM) CMOS**
7. **RHbD analogue front-ends, and more…**

ESA rad hard ASIC/FPGA solutions

"ECSS Handbook" on Mitigation Techniques against Radiation Effects for ASICs and FPGAs

- **GOAL:** help system and IC designers to choose and apply the best mitigation techniques depending on project requirements.

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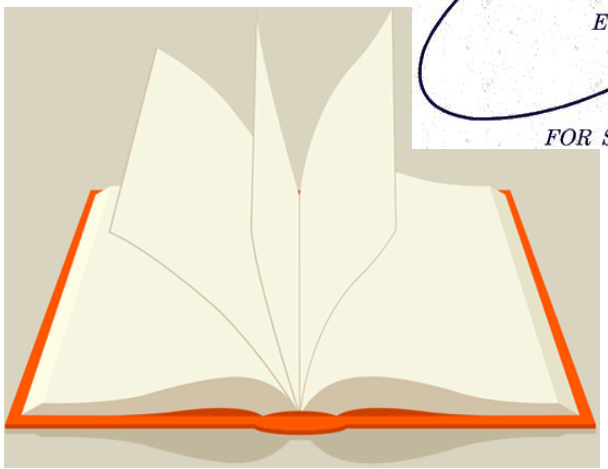
- **CONTRACTOR:** TIMA(F) and Floralis (F)
- **Cost:** 100K€
- **Start:** March 2010
- **Expected duration:** 12 months



One mitigation example (1/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)

WHAT FOR? Reduce sensitivity to Single Event Upsets (SEU) and Single Event Transients (SET) in ASICs.

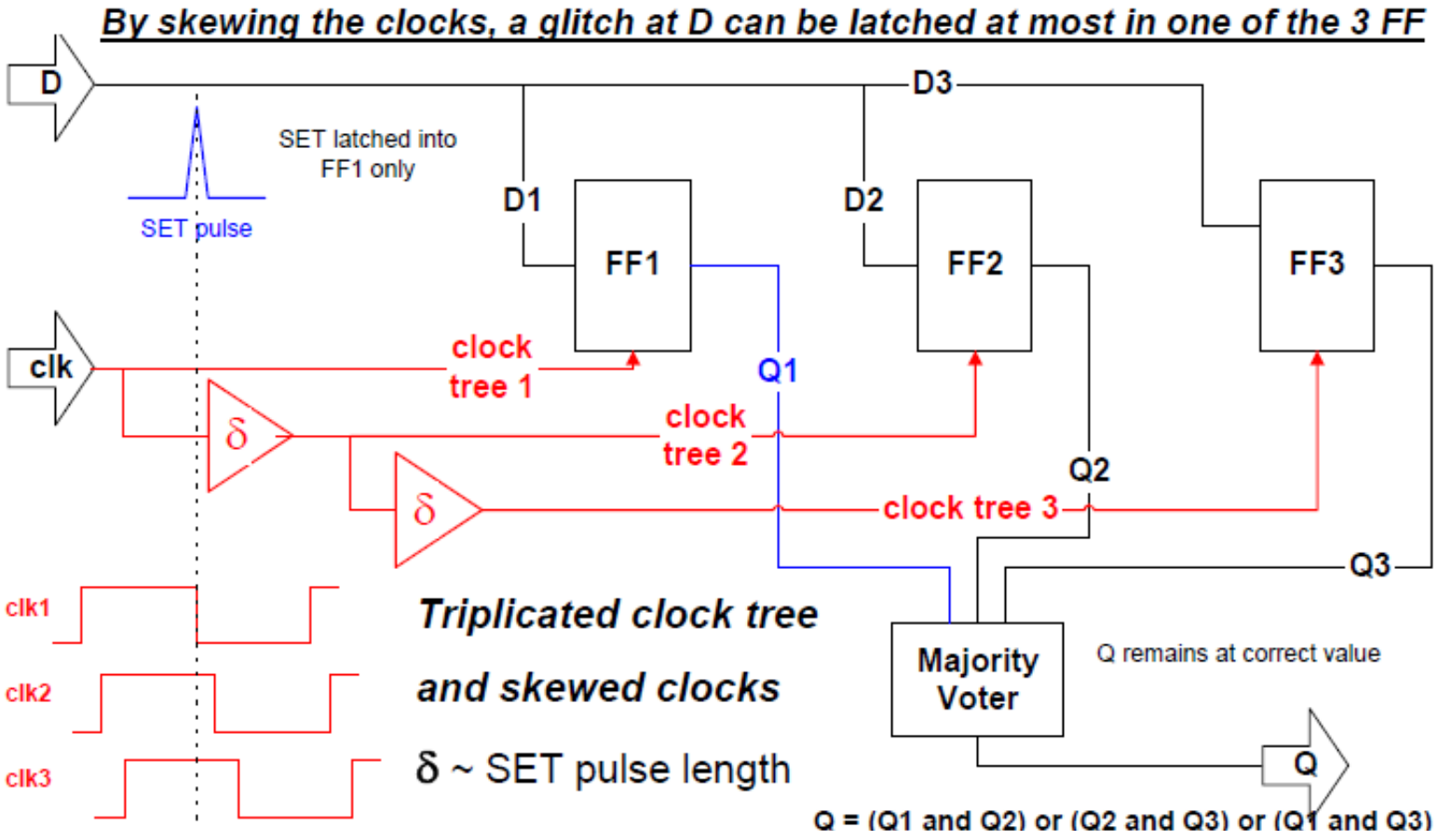
WHO? ASIC RTL designer with help of ASIC layout designer

WHERE? Gate-level netlist and clock-tree layout

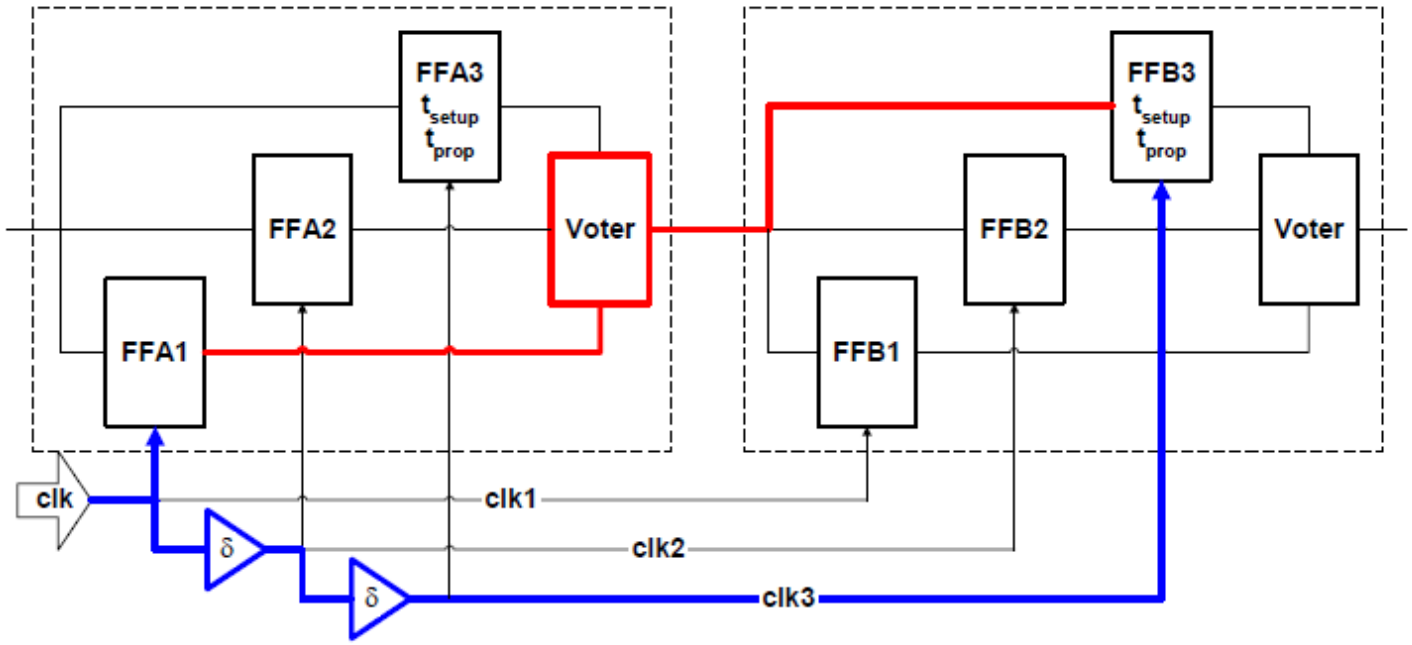
HOW? Flip-flop triplication and majority-voting to mask out SEUs, and clock-line triplication with different skews to avoid that SET pulses are latched simultaneously by flip-flops of same TMR triplet.

DRAWBACKS? More die area used, higher interconnect delays, lower max speed, higher power consumption, difficult to implement with EDA tools. Coherent skewed clock trees require manual optimization. Can introduce “hold” timing violations. Requires special attention during synthesis and netlist optimization.

One mitigation example (2/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



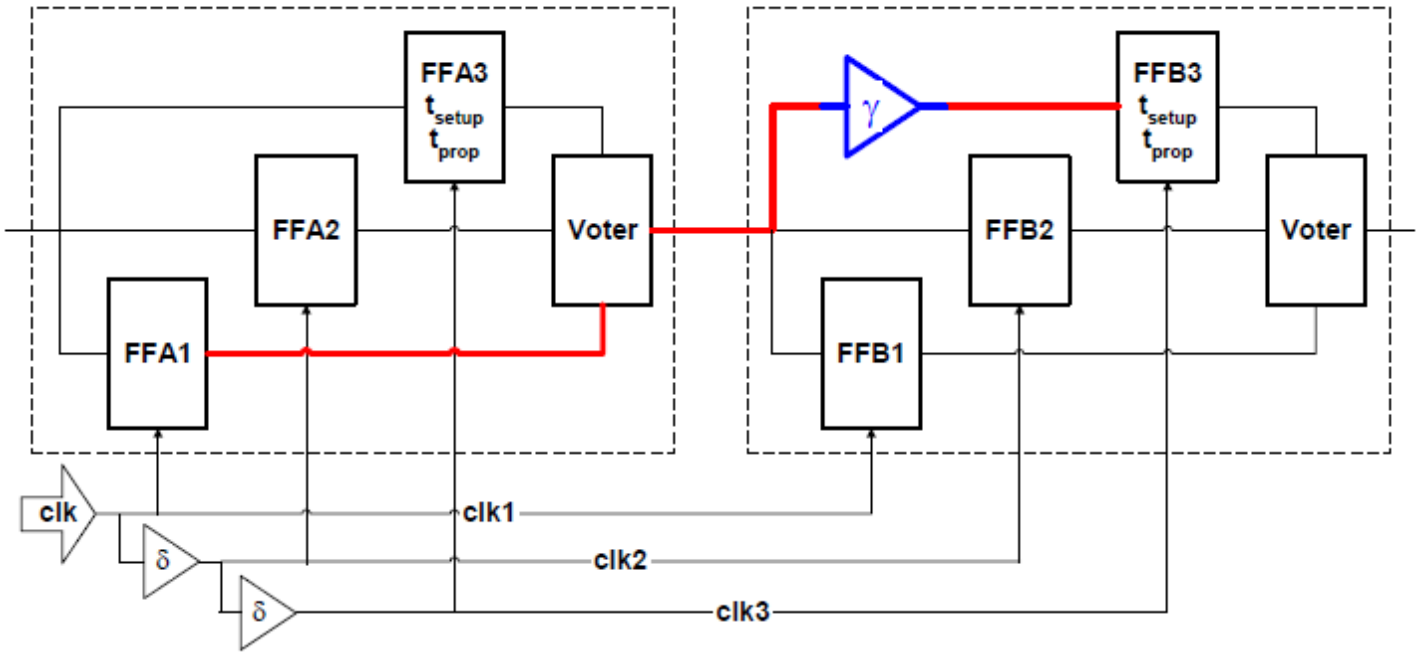
One mitigation example (3/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



When propagation delays (t_{prop}, voter) < (2 δ) clock skew

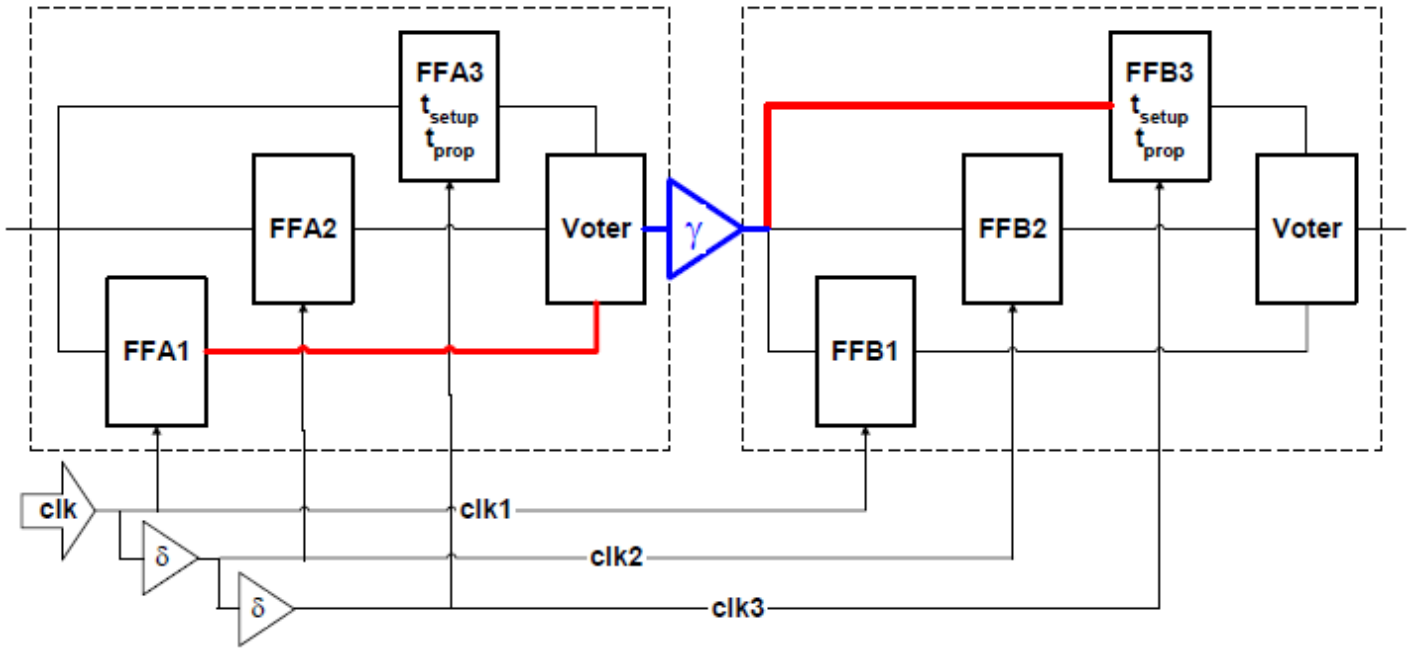
➔ hold violation FFA1 → FFB3

One mitigation example (4/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



Automatic buffer insertion by fix-hold of synthesis tool compensates clock skew → and spoils SET protection

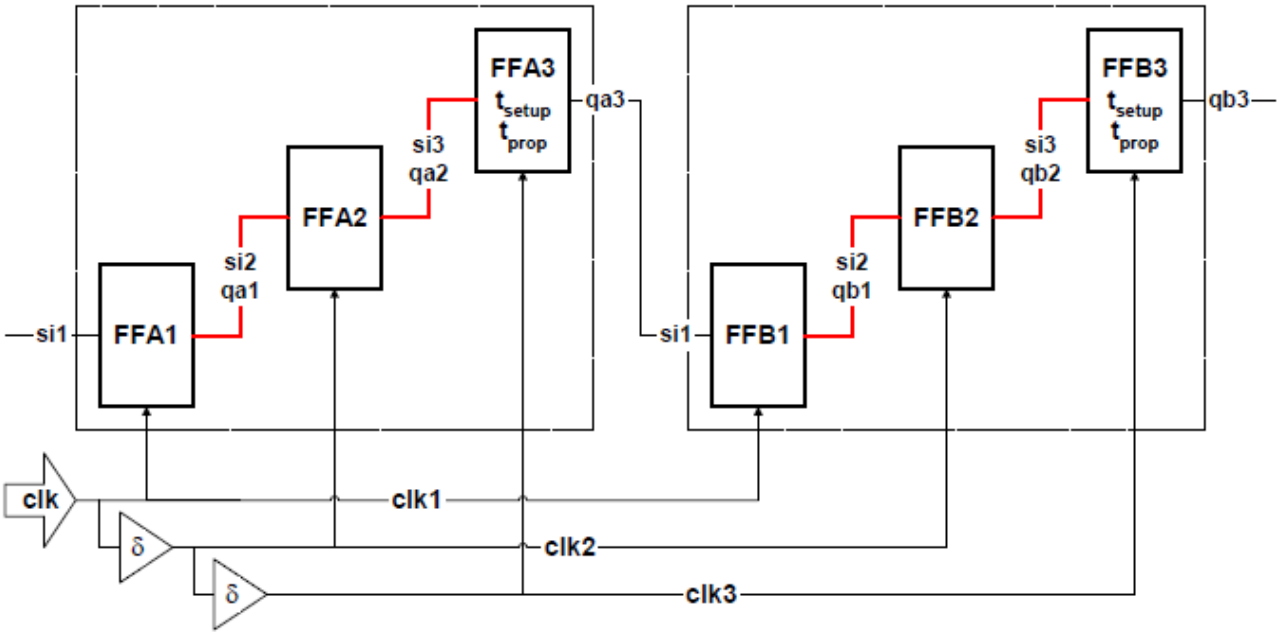
One mitigation example (5/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



Group FF belonging to the same triplet and dont_touch

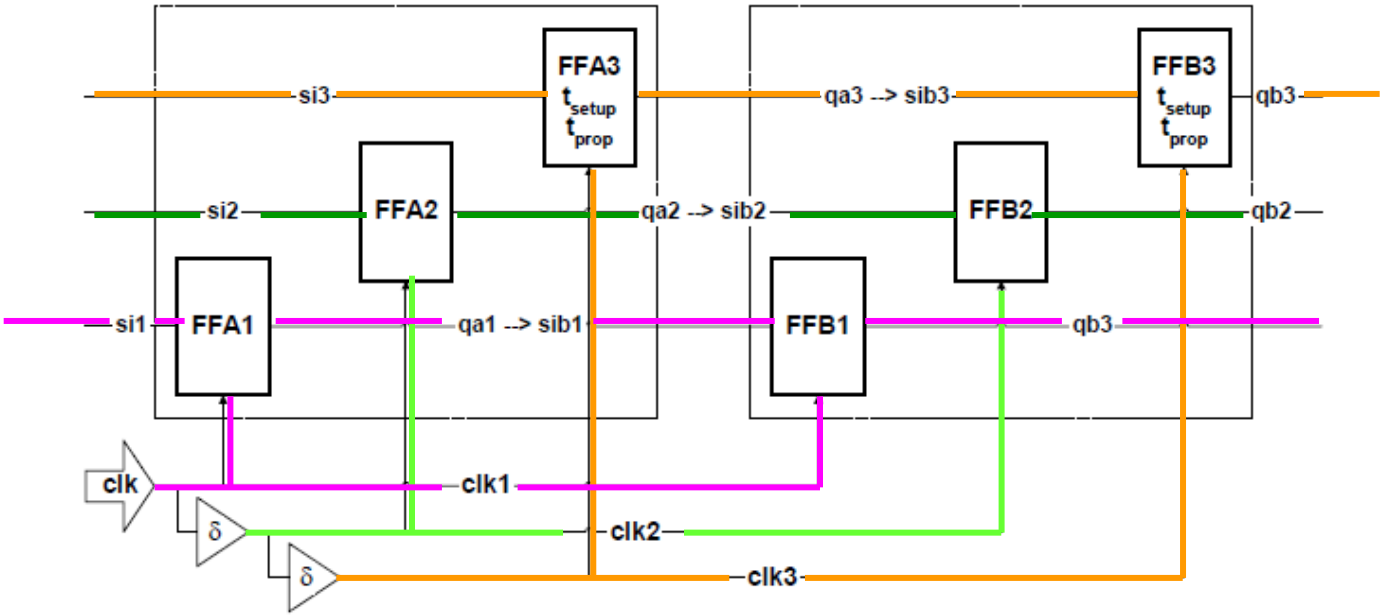
➔ SET protection through clock skew conserved

One mitigation example (6/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



Scan path routing across sub-clock domains ➔ *hold violations*

One mitigation example (7/7):
Triple Modular Redundancy with Triple Skewed clocks (STMR)



Better: one scan path per sub-clock domain

Mitigation example two (1/3):
Radiation Hardened by Design (RHbD) of memory cells

WHAT FOR? Reduce sensitivity to Single Event Upsets (SEU) of memory cells used in ASICs and FPGAs.

WHO? ASIC or FPGA cell-libraries designer

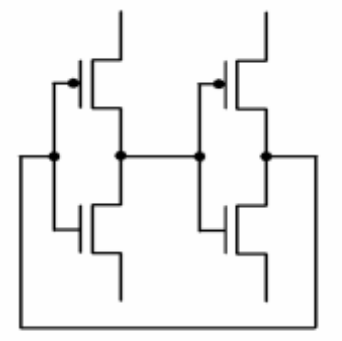
WHERE? Transistor-level (layout) cell design

HOW? Various techniques exist, all implementing feedback loops between transistors and additional memory stages that help to balance out single-event ion-induced sudden temporary excesses of charge.

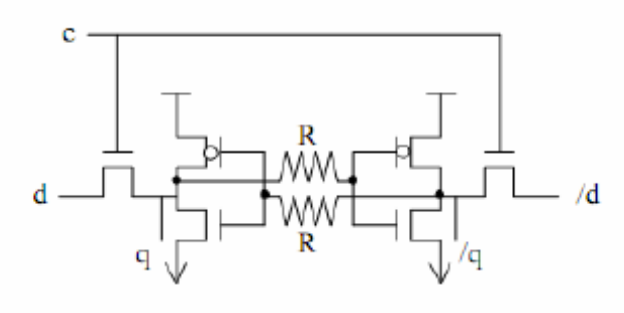
DRAWBACKS? More die area used, higher transition delays, lower max speed, higher power consumption

PLUS POINTS: vendor (ASIC or FPGA) provided solution, simplifies job of IC designer, simple synthesis constraints allow applying this mitigation where it is required only, thus minimizing its bad side effects.

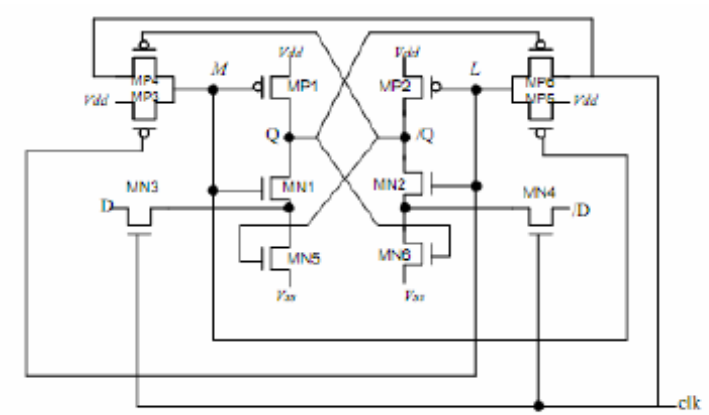
Mitigation example two (2/3):
Radiation Hardened by Design (RHbD) of memory cells



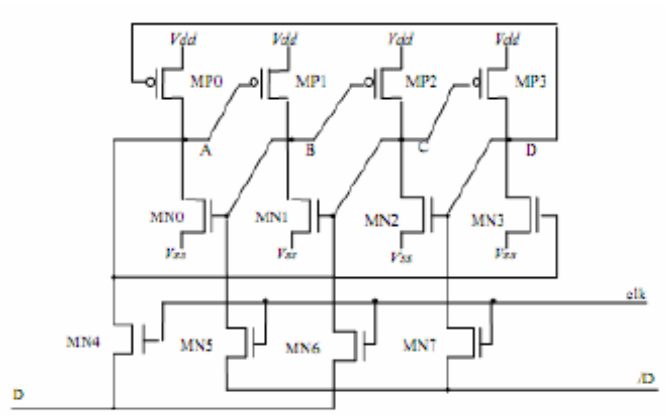
standard latch



Resistor memory cell



HIT memory cell



DICE hardened memory cell

Mitigation example two (3/3):
Radiation Hardened by Design (RHbD) of memory cells

Resistor Memory Cell
H. T. Weaver, C. L. Axness, J. D. McBrayer, J. S. Browning, J. S. Fu, A. Ochoa, R. Koga, "An SEU Tolerant Memory Cell Derived from Fundamental Studies of SEU Mechanisms in SRAM," Nuclear Science, IEEE Transactions on , vol. 34, no. 6, pp. 1281-1286, Dec. 1987

HIT = Heavy Ion Tolerant storage cell
D. Bessot R. Velazco, "Design of SEU-hardened CMOS memory cells: the HIT cell" RADECS, 1993

DICE = Dual Interlocked storage CEll
R. Velazco, D. Bessot, S. Duzellier, R. Ecoffet, R. Koga, "Two CMOS memory cells suitable for the design of SEU-tolerant VLSI circuits," Nuclear Science, IEEE Transactions on , vol. 41, no. 6, pp. 2229-2234, Dec. 1994.

Examples of RHbD ASIC libraries which include RHbD memory cells

ATMEL MH1RT (350 nm) and ATC18RHA (180 nm) – http://www.atmel.com

DARE (Design Against Radiation Effects) library for UMC 180 nm and 90 nm (under development)
http://microelectronics.esa.int/mpd2010/day1/MPD-IMEC-DARE-30March2010.pdf

ST Microelectronics library for 65 nm (under development)
http://microelectronics.esa.int/mpd2010/day2/DSM65nm.pdf

Ramon Chips library for 180 nm Tower Semiconductors (130 nm under development)
http://nepp.nasa.gov/mapld_2008/presentations/i/05%20-%20Ginosar_Ran_mapld08_pres_1.pdf

Aeroflex (600, 250, 130, 90 nm) – http://www.aeroflex.com/RadHardASIC

MRC Microelectronics on TSMC (0.35/0.25), UTMC/AMI, HP, NSC, Peregrine
http://parts.jpl.nasa.gov/mrqw/mrqw_presentations/S4_alexander.ppt

HIREC/JAXA - Fujitsu 0.18, OKI 0.15 SOI (NSREC2005)

ESA rad hard ASIC/FPGA solutions

ASIC Rad Hard libraries based on commercial processes (1/3)

- **GOALS:** “Radiation Hardened by Design” (**RHbD**) ASIC libraries used with commercial ASIC processes to produce SEL, TID and SEE resilient ASICs. RH-libs are normally a subset of existing commercial libs, where most sensitive cells are eliminated, rad hard flip-flops and other RHbD macros (PLL/DLL, RAM blocks, etc) are added. RESET and CLOCK buffered trees are optimized to reduce SET propagation.

- **ESA CONTRACTORs:** Atmel (F), STMicrolectronics (F), IMEC (B)

ESA rad hard ASIC/FPGA solutions

ASIC Rad Hard libraries based on commercial processes (2/3)

vendor	ATMEL	ST	imec UMC
Lib name	MG2RT, MH1RT, ATC18RHA	RH-CMOS65LP (TBC)	DARE (design against rad effects)
Techno node	0.5, 0.35, 0.18µm	65nm	180nm, 90nm
Library developer	ATMEL (F), co-funded by ESA	STM(F,I) co-funded by ESA	IMEC(B) funded by ESA
ASIC Manufacturer	MG2RT => **MHS**(F) Nantes, MH1RT & ATC18RHA => **LFOUNDRY** (F) Rousset	**STMicroelectronics** (F) Crolles	**UMC** (Taiwan)
Status	**MG2RT** => Discontinued, 2010 last time buy **MH1RT** => Discontinued, 2011 last time buy **ATC18RHA** => stable, ESCC certified	After several rad tests on test vehicles for terrestrial radiation (2006-2007), ESA launched a Deep Sub-micron 1st phase in 2008. 1st feasibility and definition of rad hard lib done. New lib test vehicle tape-out in April 2010, including High Speed Serial Link	180nm stable since 2004. Activities in progress to add lib elements, fix memory compilers, mixed-signal DK and consolidate end-to-end space ASIC flow . Porting to 90nm in progress. TID tests finished, SEE test results pending.

ESA rad hard ASIC/FPGA solutions

ASIC Rad Hard libraries based on commercial processes (3/3)

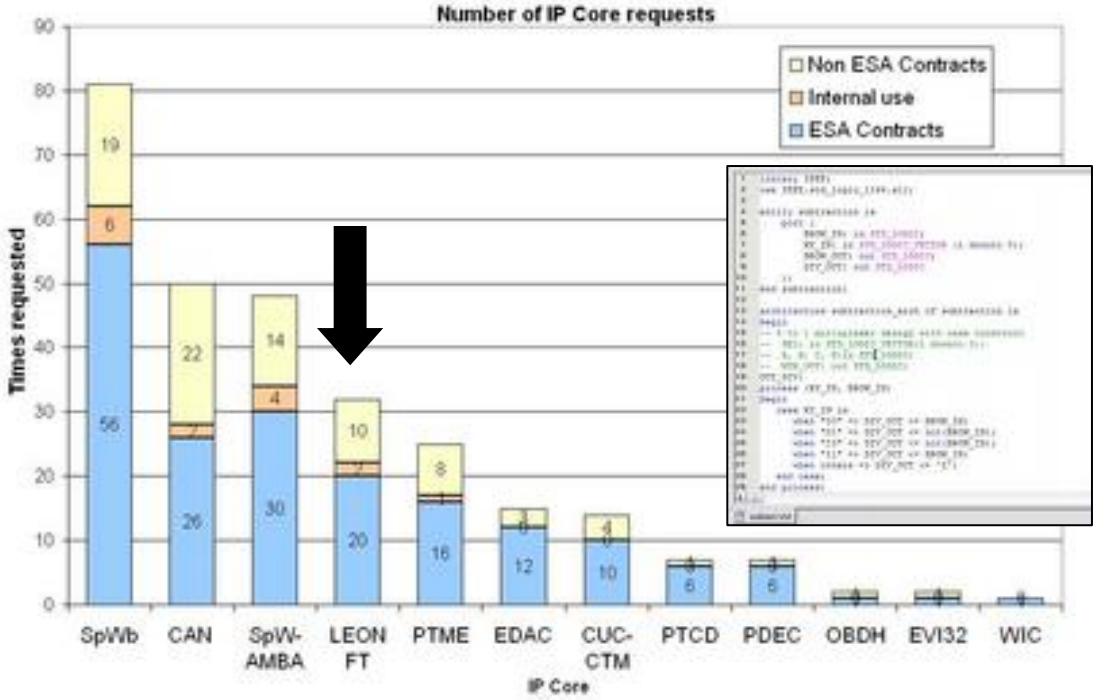
Library developer	www.atmel.com	Preliminary info	IMEC/Europractice
Lib name	MG2RT, MH1RT, **ATC18RHA**	RH-CMOS65LP (TBC)	**DARE** (design against rad effects) 180nm
SEL (MeV/mg/cm2)	**80**, **>70**, **90**(T=125C)	**> 85** (Deep-N-Well)	> **55.9**
SET	less than SEU sensitivity, more with higher clock frequencies	**TBD**	**No SETs** up to LET of **55.9** MeV.cm2/mg and total fluence of 5E+6 #/cm2
SEU (FF, SRAM, saturated cross section for Heavy Ions and Protons, **cm2/bit** or GEO/LEO **SEU/bit/day**, CREME96, solar min, 100mm Al)	MG2RT (0.5µm) => **5E-7**, LETth = 15 MeV/mg/cm2 MH1RT (0.35µm) => **2.5E-7**, LETth = 15 MeV/mg/cm2 ATC18RHA (0.18µm) => **4E-8** LETth = 30 MeV/mg/cm2 (e.g. <1E-5 errors/device/day for GEO, for LEON2FT microprocessor)	**1.3 - 2E-7** (HI, 25C-125C, HFF) **1.2E-13** (protons, HFF) **7.3E-9** (GEO, HI, HFF) **3.6E-9** (GEO, protons, HFF) **6.2E-7** (LEO, protons, HFF) **3.4E-7** (std FF, GEO, HI+P) **1.44E-6** (std SRAM, GEO, HI+P)	**8.8 10-6** (RT-FF, HI) LETth = 3.2 MeV/mg/cm2 **No SEUs** on RH-FF up to LET of 55.9 MeV.cm2/mg and fluence of 5E+6 #/cm2 (HI) **3E-5** (SRAM, HI) LETth = 3.2 MeV/mg/cm2 **No SEUs** up to 150 MeV and fluence of 5E+11 p/cm2 (protons) **3.4 E-11** (SRAM, protons)
TID (Krad(Si))	300, 300 , 300 (tested)	**100** tested, goal is **300**	**1000**

ESA rad hard ASIC/FPGA solutions: PORT , RE-USE !

1

ESA IP Cores service: maintenance, licensing and distribution of several functions in VHDL & SystemC. **LEON2FT IP Core** is the only one hardened at VHDL level.

Faster & cheaper ASIC/FPGA (pre)developments (Standard and proprietary), board model simulation, design porting to new technology, etc.



2

ESA co-funds developments of space **Standard Products** (e.g. TSC695 - ERC32, AT697 -LEON2FT, NGMP) and **Standard ASICs** (e.g. AT7013 - SpW-RTC, SCOC3)

"Off-the-shelf" catalogue space component availability (procurement leadtime proportional to stock availability and desired quality levels).

Standard ASICs and microprocessors (1/2)

All with ATMEL 0.5, 0.35 or 0.18µm

AT697E,F (*)	LEON2FT **32bit SPARC engineering and QML-Q flight models**
AT7909E	**(**SCTMTC**) Single Chip TeleMetry and TeleCommand**
AT7910E	**(**SpW-10X**) SpaceWire Router.**
AT7911E	**(**SMCS332SpW**) Scalable Multi-channel Communication Subsystem I/F between 3 SpaceWire links, central data processing unit and communication data memory.**
AT7912E	**(**SMCS116SpW**) I/F between 1 SpaceWire link and data i/f: ADC/DAC, RAM, FIFO, GPIO's, UARTs.**
T7906E	**(**SMCS lite**) Single Point to Point IEEE 1355 High Speed Controller**
TSS901E	**(**SMCS332**) Triple Point to Point IEEE1355 High Speed Controller**
TSC695 (*)	**(**ERC32 single chip**) Rad hard SPARC single chip processor**
TSC21020F (*)	**Rad Hard 32-bit floating point DSP**
T79055 (**)	**(**AGGA2**) Advanced GPS/GLONASS ASIC**

(*) Standard Microprocessors products **(**) Not in catalogue, but available with ESA authorisation**

Standard ASICs and microprocessors (2/2)

Under development (ATMEL 0.18µm and STMicroelectronics 65nm) :

AT7913E	(SpW-RTC) **SpaceWire-Remote Terminal Controller**
XXXXXX (**)	(SCOC3) **Spacecraft Controller on a Chip (protos Q4-2009)**
XXXXXX (**)	(FFTC) **Fast Fourier Transform Coprocessor (protos Q4-2010)**
XXXXXX (**)	(HSSL) **High Speed Serial Link ASIC (protos Q3-2010)**
XXXXXX (**)	(CWICOM) **CCSDS Image Compression ASIC (Q4-2011)**
XXXXXX (**)	(NGMP) **Next Generation Multi-purpose Processor (protos 2011)**
XXXXXX (**)	(AGGA4) **Advanced GPS/GALILEO ASIC (protos Q3-2011)**
XXXXXX (**)	**Next Generation DSP**

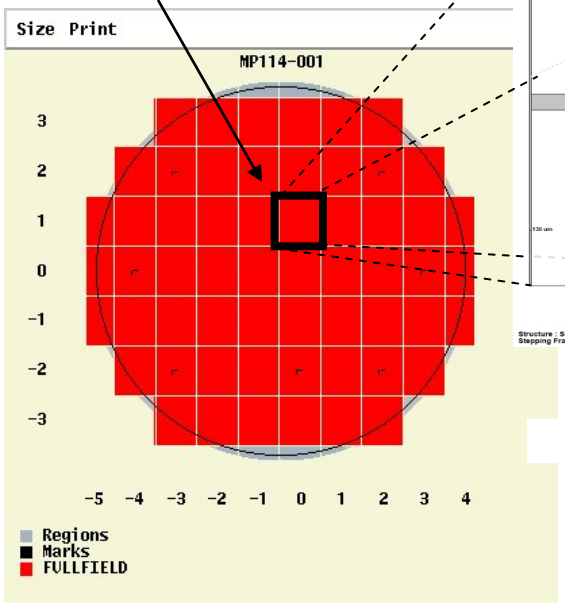
(*) Standard Microprocessors products **(**) Candidate for :"standard ASIC" not approved yet**

Space Multi-Project Wafer programme

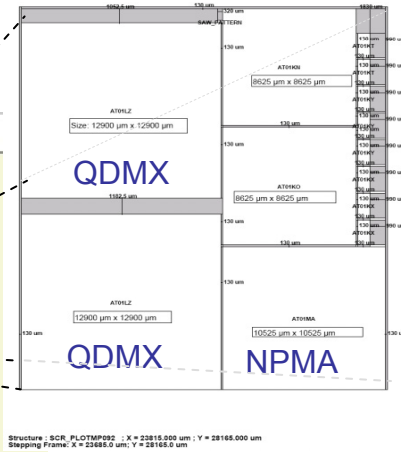
GOALS: share mask/wafer costs, encourage first users (ESA funds the 4 first runs for 1.5M€)

ATMEL (F) ATC18RHA CMOS 0.18µm, based on commercial process, hardened std-cell libraries, characterized and ESCC qualified with ESA and CNES support.

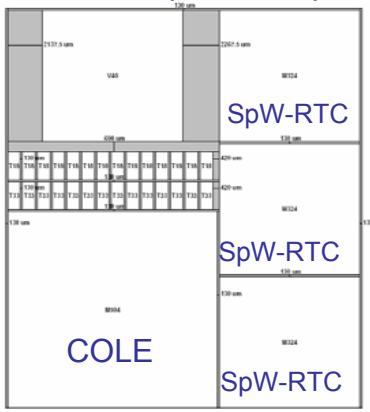
Several chips per wafer reticule



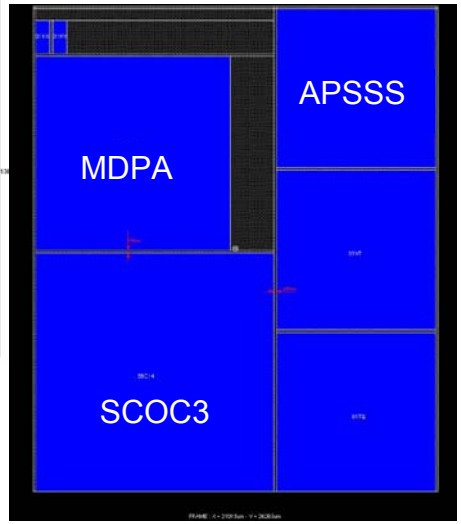
Validation run (Oct 04)



1st run (Dec 07)



2nd run (Jan 09)

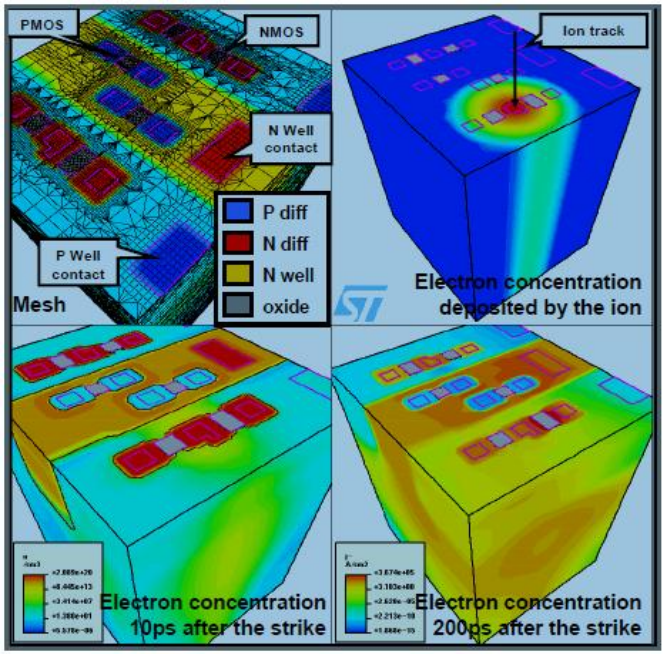


3rd run (Mar 10) & 4th run (Mar 2011)

Radiation Effects in Deep Sub Micron (DSM) CMOS

- **GOAL:**
  Simulation Framework toolkit for IC designers to characterize impact of radiation effects on DSM ICs. Characterization by theoretical analysis and 3D simulation of SEE and TID, and new effects and trends in DSM. Chosen DSM tech to analyze is **UMC 90nm**.

- **CONTRACTORs:** Qinetiq(UK), Atmel(F), University of Vienna(A)
- **Cost:** 300K€
- **Start:** August 2009
- **Expected duration:** 24 months



space FPGAs

	XILINX®	Actel®	ATMEL
	• SRAM-based 0.35 µm-65 nm	• Anti-fuse (ONO and M2M) 0.8 – 0.15 µm	• Hardened SRAM-based 0.35 – 0.18 µm
Weaknesses	• More SEU sensitive • Hardening by design needed at various levels • **MCGA packages not space qualified yet**	• Can be programmed only once • ITAR applies (RTAX) • Parts Cost	• Small capacity (40K) available until 2008 • New technology not used yet
Strengths	• Unlimited easy reprogramability • Many hard-macros included (DSP, mC, SERDES)	• Rad Hard • Higher level of Space Qualification • Space Legacy	• Unlimited easy reprogramability • Non ITAR, fabricated in EU • SEU-hardened SRAM/FF/CLK/RST

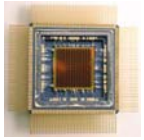
Radiation resilience of space FPGAs

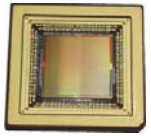
vendor	XILINX	Actel	ATMEL
Device type datasheet	**QPro™ Virtex™-II**	**RTAX-S/SL**	**AT40KEL040**
TID (Krads(Si))	200	300	300
SEL (MeV/mg/cm2)	> 160	> 117	80
SEU sat cross section (cm2/bit) Or GEO (Errors/Bit-Day)	GEO upsets < 1.5E-6 per device day (with TMR+ SRAM scrubbing)	< 1E-10 Worst-Case GEO	2.5E-8 (*) 2.5E-7 (**)
SEU LETth (MeV/mg/cm2)		>37	16 (*) 15 (**)
SET		No Anomalies up to 150 MHz	As MH1RT ASICs

(*) SRAM used for configuration logic

(**) SEU hard flip-flops

ESA support to European space FPGAs:






Today, ESA missions use mainly FPGAs from ACTEL. **Xilinx** FPGAs are used seldom, in “non critical” applications. Atmel space FPGAs are starting to be used, and expected to grow in capacity.

CNES and ESA are supporting European reprogrammable space FPGA developments, based on ATMEL expertise and technology, but also with JAXA/HIREC/OKI support

- 40K & 280Kgates FPGA DK capabilities evaluation (for ESA IP Cores) (ESA Funding)
- 450 Kgates FPGA/SOI Validation Phase (ATMEL/OKI/HIREC) (CNES Funding)
- 280 Kgates FPGA + 4 Mbit EEPROM in one package (CNES Funding)
- Reprogrammable Computer in one package:
  LEON2 AT697F + 280 Kgates FPGA in one package (CNES Funding)
- FPGA 280Kgates ESCC Evaluation (ESA Funding)
- FPGA/SOI 450 Kgates development (JAXA/CNES/ATMEL/OKI/HIREC) (CNES + JAXA Funding)

- **Next Challenge:** **>1Mgates European space reprogramable FPGA**. Based on ex-**Abound Logic** IP and Atmel RHbD technology. Negotiations at different levels on-going. (Abound Logic has recently split into several new companies)

SAFE use of reprogrammable space FPGAs

ESA supports developments of new tools and to help making safe use of reprogrammable space FPGA (Atmel and Xilinx), with internal research and R&D contracts

- **FLIPPER:** fault injection and analysis in configuration logic of **XILINX** FPGA (INAF, I)
- **SUSANNA, JONATHAN**: fault injection and analysis in configuration logic of **ATMEL** FPGA (ESA, P di Torino, I)
- **RORA, STAR**: SEU-protection-aware synthesis, P&R in **XILINX** FPGA (P di Torino, I)
- **FT-UNSHADES:** fault injection and analysis in users logic of **any IC netlist** (U o Sevilla, E)
- Fault-tolerance, space exploration and system **reconfiguration of multi-FPGA systems** (XILINX, RAPTOR; ESA, P di Milano, LuxSpace, TWT(D), AST-UK)
- Radiation Tests of **ACTEL-proASIC** (FLASH) (ESA, Pdi Torino, I)

Workshop on Fault Injection & Fault Tolerance in space FPGAs, Sept 09:
http://www.esa.int/TEC/Microelectronics/SEMV57KIWZF_0.html

Validating the Mitigation Techniques

verifying that the protection logic is there and that the nominal functions still work as expected

1 - Structural and formal verification

- Check presence of triple FF, correct wiring of the three clock/reset domains
- Parsing netlist with intelligent search scripts , graph-based algorithms

2 - Fault simulation (SEU emulation in SW)

- Forcing values at memory elements with CAD simulation tools
- Adding fault-injection control and observability logic

3 - Fault injection (SEU emulation in HW)

- HW emulation of SEU using SRAM-FPGA and reconfiguration
- Pulsed Laser fault injection

4 - Ground-based radiation testing

Validating the Mitigation Techniques

SEU emulation, simulation and mitigation analysis tools overview

Tool Name	Developer	Tech	SEU injection	SEU sim at SW speed	SEU emu at HW speed	Monitor fault propagation	SEU weak areas finding	Recognize & check TMR	SEU in FPGA Conf mem	Improve P&R of SRAM-FPGA
FT-UNSHADES	U. Seville (E)	**all**	yes		yes	yes	yes		yes	
SST	ESA (NL) / U. Antonio Nebrija (E)	**all**	yes	yes		yes	yes			
FLIPPER	INAF (I)	**Xilinx FPGA**	yes		yes	yes	yes		yes	
STAR/VPLACE /RoRA	P. Torino (I)	**Xilinx FPGA**					yes		yes	yes
INFAULT	ESA (NL)	**all**					yes	yes		
SUSANNA/ JONATHAN	P. Torino (I) / ESA (NL)	**Atmel FPGA**					yes		yes	yes

Validating the Mitigation Techniques

SEU emulation, simulation and mitigation analysis tools overview: more info

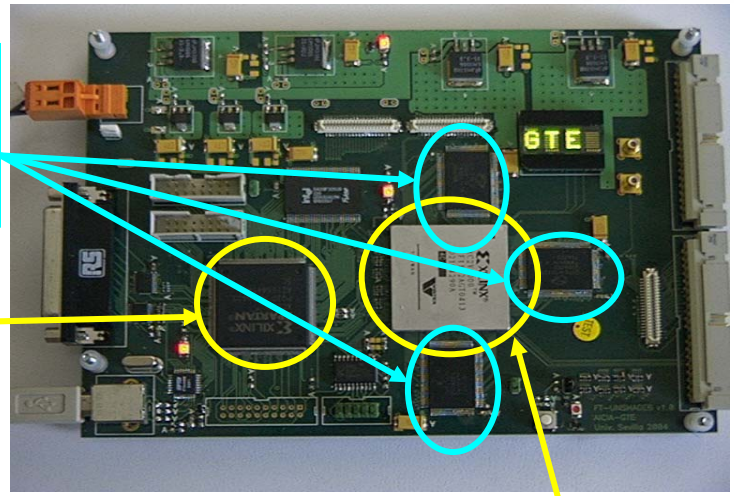
Tool Name	Developer	More Info
FT-UNSHADES	University of Seville (E)	http://walle.us.es/ftunshades/index.html http://microelectronics.esa.int/finalreport/FT-UExcutiveSummary.pdf
SST	ESA (NL) / University Antonio Nebrija (E)	http://www.esa.int/TEC/Microelectronics/SEMQ1WU681F_0.html http://www.nebrija.es/~jmaestro/esa/
FLIPPER	INAF (Italian National Institute for Astrophysics) (I)	http://microelectronics.esa.int/techno/Flipper_ProductSheet.pdf http://www.iasf-milano.inaf.it/Research/high-rel_computing_rg.html http://cosy.iasf-milano.inaf.it/flipper_index.htm
STAR / VPLACE / RoRA	Politecnico di Torino (I)	www.cad.polito.it
INFAULT	ESA (NL)	http://microelectronics.esa.int/papers/SimonSchulzInFault.pdf
SUSANNA / JONATHAN	P. Torino (I) / ESA (NL)	www.cad.polito.it

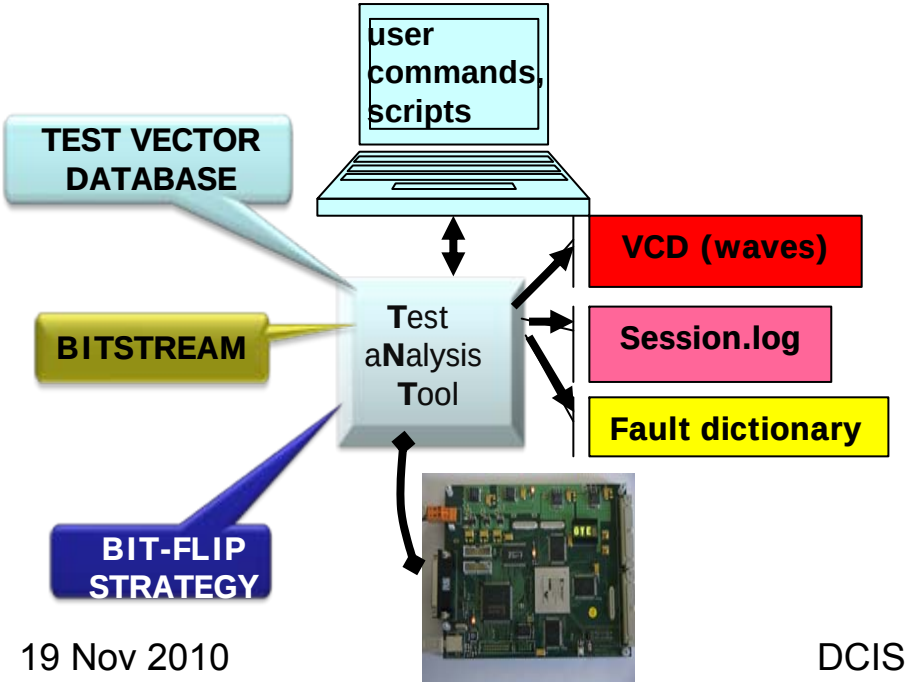
FT-UNSHADES

Fault **T**olerance- **U**niversity Of **S**evilla **H**ardware **D**ebugging **S**ystem

WHAT IS IT?

•Fault injection tool to emulate and analyze SEU effects in ICs during dynamic operation at HW speed.
•"GOLDEN" and "DUT" designs, inside "system" Xilinx FPGA.
•SEU emulation based on FPGA partial reconfiguration.
•Non-intrusive approach: we need IC "netlist" & test-benches (VHDL, waveform inputs).
•PC+SW + "control FPGA" apply stimuli stored in external memories, inject faults and monitor results.

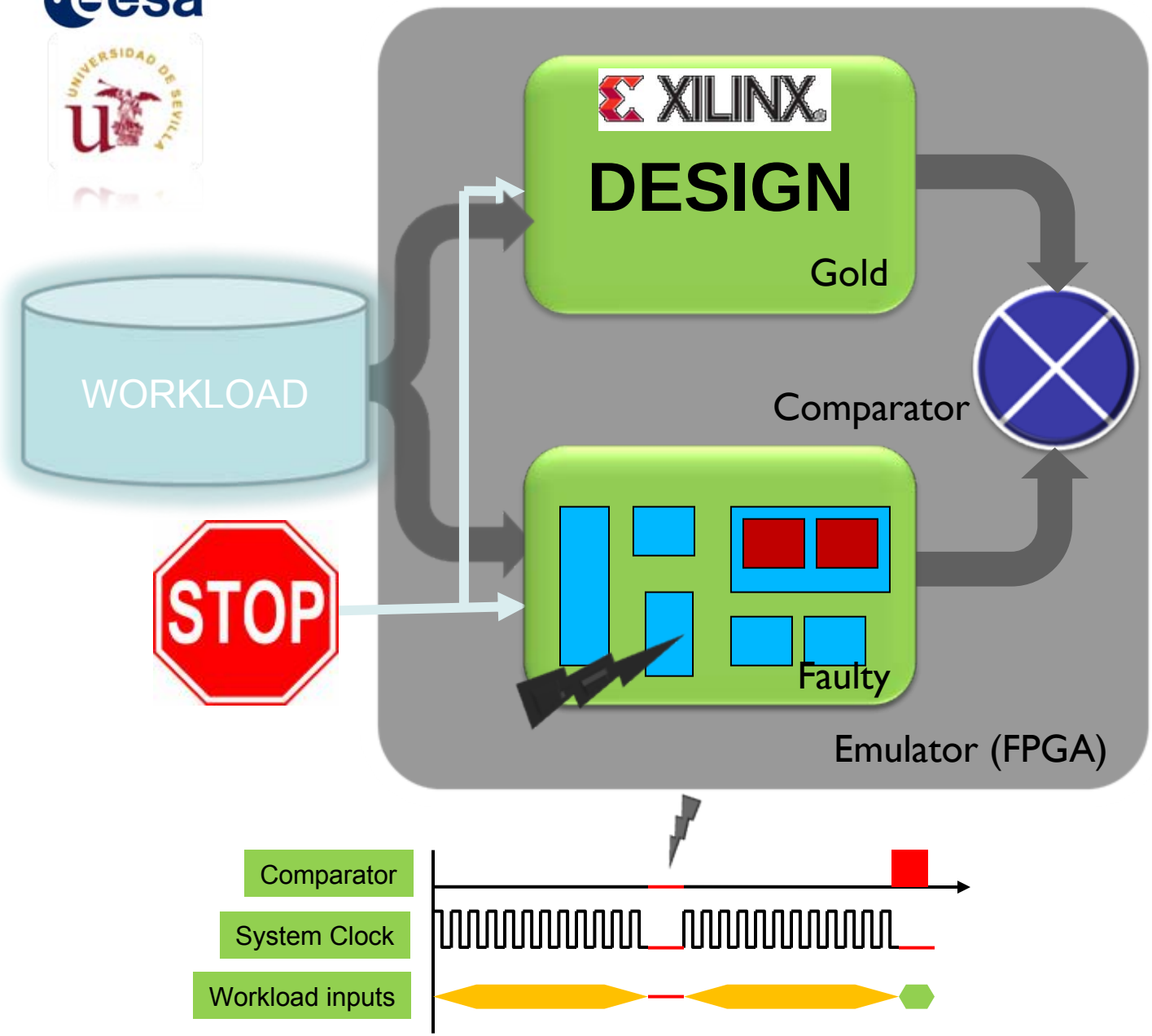




WHAT CAN IT DO?

•Analyze effects of SEUs in IC internal registers and outputs (IC netlist for ASIC or FPGA !!).
•Assess efficency of SEU protections.
•Predict and explore potential SEU weak points.
•SEU injections, at chosen locations & times (specific, random, windows, systematic sweeps)
•Cycle-to-cycle internal fault propagation analysis is possible.
•Remote access/use of FT-U thru internet possible.

FT-UNSHADES



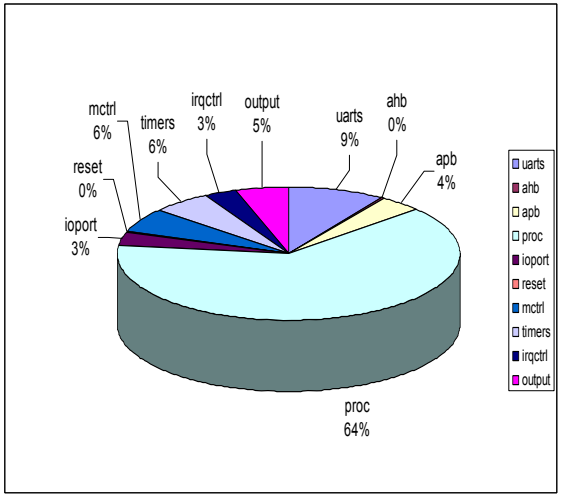
Basic Execution Model

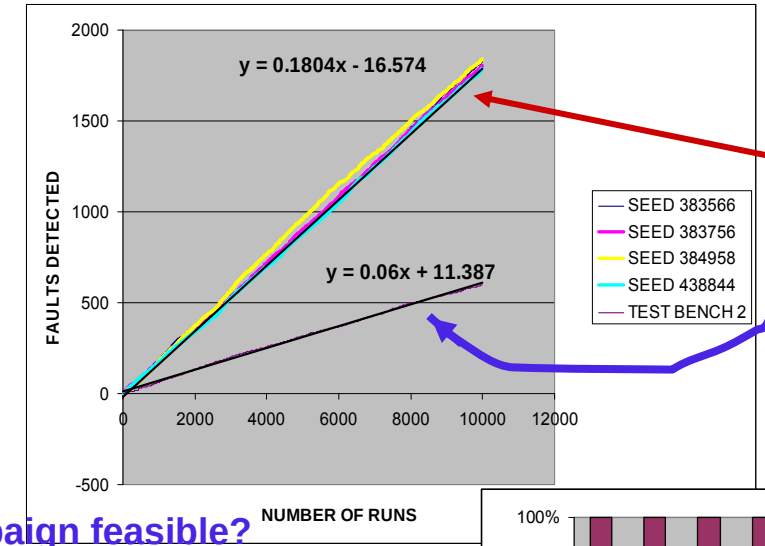
- Two identical instances of IC design implemented: “GOLD” & “FAULTY” (DUT)
- Input vectors stored in external memories (workload)
- System clock is common to both instances, which run in parallel
- Injection is only done to the “FAULTY” instance. The “GOLD” always shows good internal states and outputs
- Register targets found using bitstream information provided by Xilinx tools.
- Run→Stop CLK → Inject → resume CLK→run & compare

FT-UNSHADES: LEON2FT tests

2559 registers

ahb	apb	proc	ioport	reset	mctrl	timers	irqctrl	output
5	86	1440	74	8	131	127	64	115





Different testbenches give diff max "SEU sensitivities" :
TB_FULL: 18%
TB_FUNC_32: 6%

87% of errors
RESET: *Very sensitive*
Only 8 Registers

An exhaustive injection campaign feasible?

CLK CYCLES in the Testbench= 369,848 = "1 RUN"
Average time per RUN (with 1 SEU injected)= 0.26 sec
NEEDED RUNs: 946,441,032 → **2848 days**!!!

Actual chosen injection tests conditions

- #RUNs per test campaign ~10,000
- 1 SEU x RUN
- RANDOM locations and times

1.4% of errors
IOPORT: *Insensitive*
74 Registers

"Normalized" SEU sensitivity per block (20 injections per register)

FT-UNSHADES

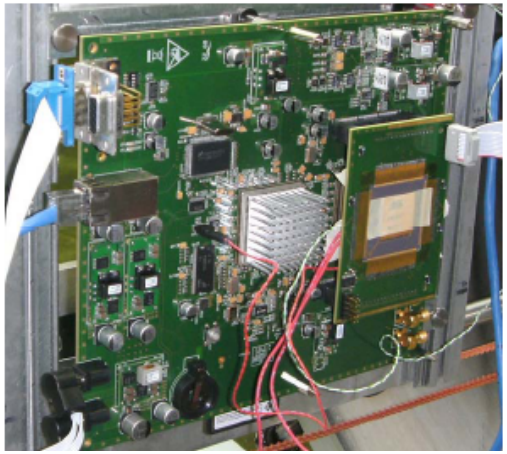
Other designs tested:

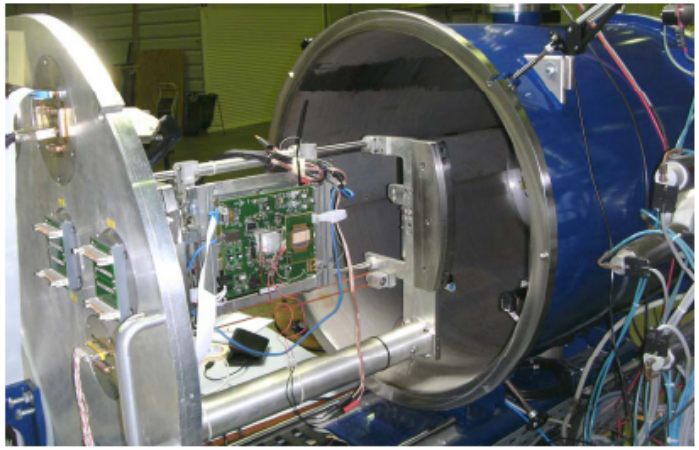
- **Leon, Leon2 and Leon3**
- **MicroBlaze**
- **8051**
- **Cordic 18x18x18**
- **PicoBlaze**
- **RENASER RadTest device**
- **Other ESA benchmarks...**

New version under development today: larger capacity, based on Virtex5 (more # gates, #IO pins, test vectors), higher test speed (x10-100) doing more test control from “control FPGA” and less with PC-SW (avoiding USB comm bottlenecks) , easier board scalability. New system expected for Q4-2011.

Validating the Mitigation Techniques

- ***Radiation Facilities in use by ESA*** https://escies.org/ReadArticle?docId=230
  - Co-60 at ESA/ESTEC, Netherlands (total dose)
  - Californium-252 at ESA/ESTEC, Netherlands
  - Paul Scherrer Institut (PSI), Switzerland: proton irradiation
  - Louvain la Neuve (UCL), Belgium: heavy ions and protons
  - Jyväskylä University, Finland: heavy ions and protons





France : IPN, *Italy :* LNL, *UK :* AEA Harwell , *USA :* BNL, …	HI : E < 10 MeV/n (Tandem Van de Graaff)
Belgium : UCL , *Japan :* TIARA, *Swizterland :* PSI (OPTIS), *USA :* LBL, UCD…	HI : E ≥ 10 MeV/n p+ : tens of MeV (88-inch cyclotrons)
Canada : TRIUMF, *Finland :* JYFL, *France :* GANIL, *Germany :* GSI, *Japan :* JAERI, *Switzerland :* PSI (PIF), CERN, *Russia :* DUBNA, PNPI, *USA :* IUCF, NSCL, TASCC, TAMU…	HI : tens of MeV/n p+ : hundreds of MeV (cyclotrons, synchrotrons)

Summary

- Several teams in ESA working in Microelectronics & Rad Effects
- Radiation effects in ICs can damage on-board experiments or entire satellite
- Space radiation can cause temporary and destructive effects in ASICs and FPGAs. SEL, TID, SEU, SET….
- Many possible countermeasures, at various levels (system, netlist, layout of cells, etc).
- Two examples of mitigation techniques: Skewed-clocks TMR and RHbD memory cells
- Multiple ESA rad hard ASIC and FPGA activities: Mitigation techniques handbook, RHBD libraries with Atmel, STM and IMEC-UMC, Atmel MPW, Standard ICs, IP Cores, mitigation verification test tools, rad effects on DSM…
- Space FPGAs: ACTEL (OTP), Xilinx (reprogrammable). Many efforts to create new European solutions, based in Atmel and ex-Abound Logic IP
- Validating Mitigation Techniques is important: analysis, fault injection at SW and HW level (one example: FT-UNSHADES), ground-based radiation tests

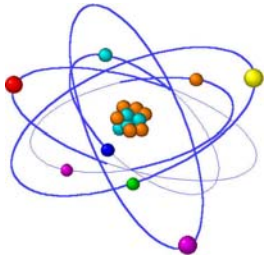
More info:

ESA Microelectronics Section

http://www.esa.int/TEC/Microelectronics/index.html

ESCC: European Space Components Coordination https://spacecomponents.org
ECSS: European Cooperation for Space Standardization http://www.ecss.nl/
ESCIES: European Space Components Information Exchange System https://escies.org/

THANK YOU



Questions?

Analogue, mixed-signal space ASICs

ESA has organized 3 **AMICSA** workshops (2006, 2008 & 2010) to share know-how and experiences. Dispersion of efforts, same concerns, little reuse…

Rad Threats

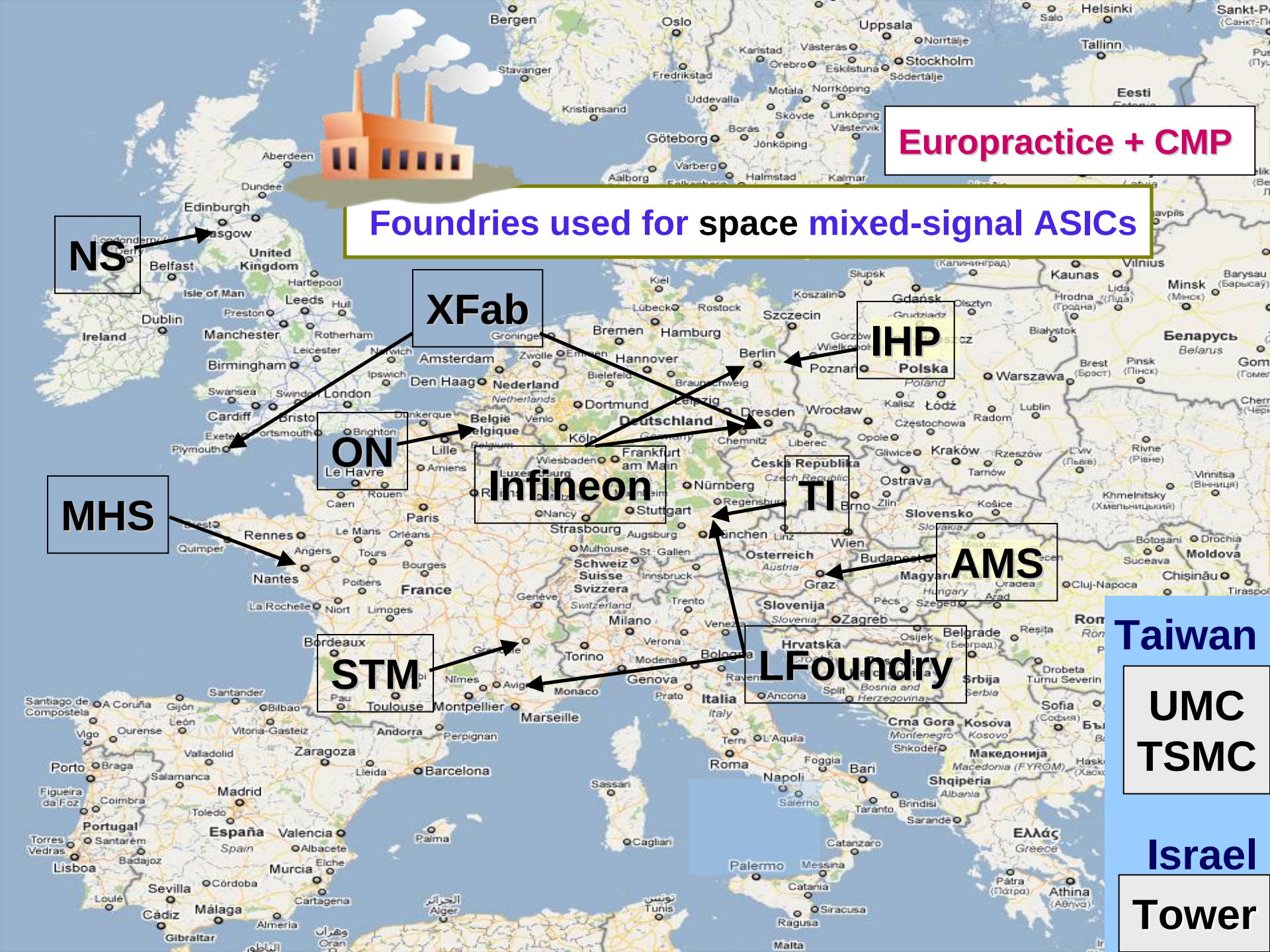
(TID, SEE)

- high leakage currents
- Vth shifts
- parasitic transistors/ latch up
- gate rupture
- data corruption (bit flips)
- transient pulses
- gain degradation

Mitigation Techniques

(technology and function dependent)

- enclosed/bigger transistors, H-shape
- guardband rings / STI / LOCOS
- avoid diffusion resistors in favour of oxide R
- epi layer / hetero-epi
- buried-layers
- low gain artificially provoked parasitic transistors
- DRC isolation rules + waving to allow ELT
- SOI
- thinner field oxide, thicker gate oxide
- hardened libraries (re-size, cell-topology)
- ADC offset auto-zeroing (analogue and digital correction)
- architecture hardening (open vs closed loop)
- redundancy and voting/comparing
- self-powering functions (reducing SEL options)
- cyclic reset to prevent SEE accumulation
- SET glitch filtering
- Epitaxial N-pockets
- Minimize use of NMOS transistors


Europractice + CMP
Foundries used for space mixed-signal ASICs
NS
XFab
IHP
ON
Infineon
TI
MHS
AMS
STM
LFoundry
Taiwan
UMC
TSMC
Israel
Tower