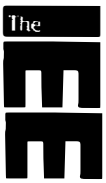

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SEE Analysis and Mitigation for FPGA and Digital ASIC Devices

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Introduction

- ***The Technical and Quality Management Directorate***
  - http://www.esa.int/techresources/index.html
- ***The Space Environments and Effects Section***
  - Analysis of space environments and their effects on space systems
  - http://space-env.esa.int/index.html
- ***The Radiation Effects and Analysis Techniques Section***
  - Analysis at component level and radiation testing
  - https://escies.org/public/radiation/esa/
- ***The Microelectronics Section***
  - Availability of appropriate technologies and development methods
  - Availability of space-specific standard components and IP
  - Development support to projects
  - Analysis and mitigation of SEE at design level
  - http://www.estec.esa.nl/microelectronics/

SEU Emulation and Simulation Tools

- ***FT-UNSHADES***
  - SEU Validation of ASIC designs by fault injection into user flip-flops and user memory using an SRAM based FPGA
  - http://www.estec.esa.nl/microelectronics/finalreport/FT-UExcutiveSummary.pdf
- ***FLIPPER***
  - SEU Validation of designs targeting Xilinx Virtex II reprogrammable FPGAs (RFPGA) by fault injection into the configuration memory and reconfiguration logic registers
  - http://www.estec.esa.nl/microelectronics/techno/Flipper_ProductSheet.pdf
- ***The SEUs Simulation Tool (SST)***
  - A set of Perl and tcl scripts, which allows injecting SEU like faults into HDL and netlist simulations
    - » http://www.estec.esa.nl/microelectronics/asic/asic.html

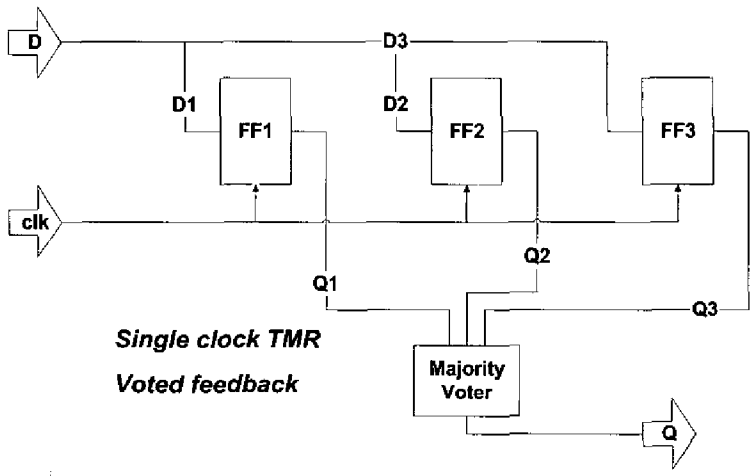
SEU mitigation in reprogrammable FPGA

- ***SEE mitigation by design for commercial RFPGA***
  - Functional Triple Modular Redundancy (FTMR) – a method to implement combinatorial and sequential triplication and voting in VHDL source code and to conserve it through synthesis
  - http://www.estec.esa.nl/microelectronics/techno/reprofpga.html
  - Future projects TBD: evaluate Xilinx XTMR, design a scrubbing controller IP
- ***Xilinx Europe SEE Consortium***
  - "A voluntary group of organizations that have a mutual interest in the evaluation of reconfigurable FPGAs for Aerospace Applications"
  - http://www.cad.polito.it/research/consortium.html
  - http://www.xilinx.com/products/silicon_solutions/market_specific_devices/aero_def/capabilities/see.htm
- ***Development of SEE hardened reprogrammable FPGA***
  - Atmel AT40KEL and the next generation 200K FPGA under CNES contract
  - http://www.atmel.com/dyn/products/product_card.asp?part_id=2766
  - Xilinx RT Virtex (ITAR...?)

SEU mitigation in cell-based digital ASIC

- ***Hardening of on-chip SRAM***
  - EDAC to detect and correct errors: impact on control state machines
  - For redundant data (caches): error detection by parity bits sufficient
  - Parity covers only limited #upsets in a data word: → scrubbing required
- ***Hardening at layout level: SEU hardened library flip-flops***
  - HIT cell used in the DARE (Design Against Radiation Effects) library
  - http://www.estec.esa.nl/microelectronics/finalreport/DareExecutiveSummary_V3.pdf
  - Other hardened libraries around the world:
    - » **ATMEL in their 0.35 and 0.18 technologies** http://www.atmel.com/
    - » **MRC Microelectronics on TSMC (0.35/0.25), UTMC/AMI, HP, NSC, Peregrine** http://parts.jpl.nasa.gov/mrqw/mrqw_presentations/S4_alexander.ppt
    - » **HIREC/JAXXA** http://www.hirec.co.jp **- Fujitsu 0.18, OKI 0.15 SOI (NSREC2005)**
- ***Hardening by Triple Modular Redundancy (TMR) flip-flops***
  - Triplication of flip-flops and combinatorial voting
  - Implemented in the RTL source code, by netlist editing or by synthesis tool
  - Overhead x3 on flip-flops, x2 on typical designs (50% combinatorial logic)
  - Impact of voting on the speed of the design

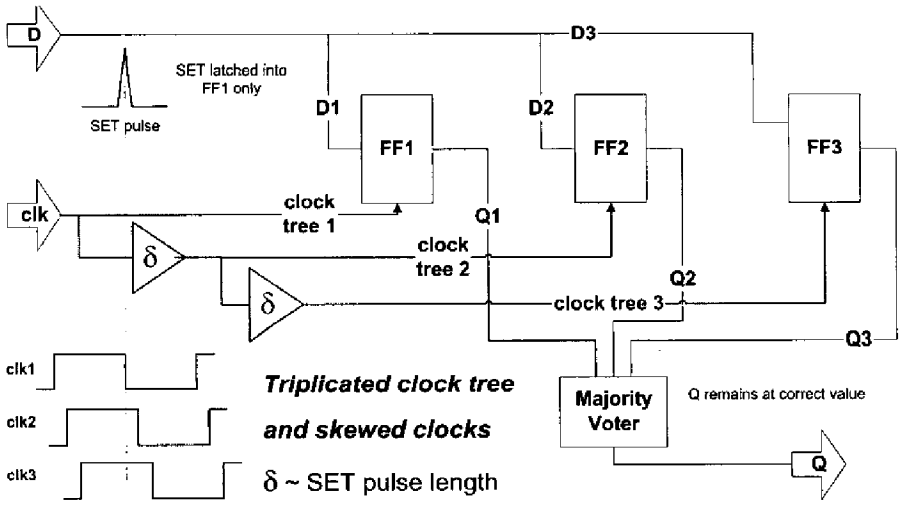
TMR Flip-Flop with voter



Single Event Transients (SET)

- ***Collision induced carrier generation in PN junctions***
  - Propagate as glitches in combinatorial logic
  - Latched into storage cells when arriving at data input during clock edge
  - → Upset rate increases with the clock frequency
  - Effects observed already on 0.5 µm technology (ERC32 processor)
  - … they are definitely a concern in 0.18 µm and below
- ***Analysis of SET effects in simulation and radiation tests***
  - SET pulse length and amplitude are most important parameters
  - Specific test structures to catch and characterise the pulse
  - CNES contract with Atmel on SET effects in the 0.18 µm technology
- ***Mitigation of SET effects***
  - http://www.mrchsv.com/docs/Vanderbilt/Circuit%20and%20layout%20Issues.pdf
  - "Dual Stream": Propagation of complementary logic levels
  - Using stronger drivers and higher capacitive loads
  - Temporal Vote: Triple skewed clocks in conjunction with the TMR flip-flop
  - Triplication of nets (e.g. for clocks and resets)

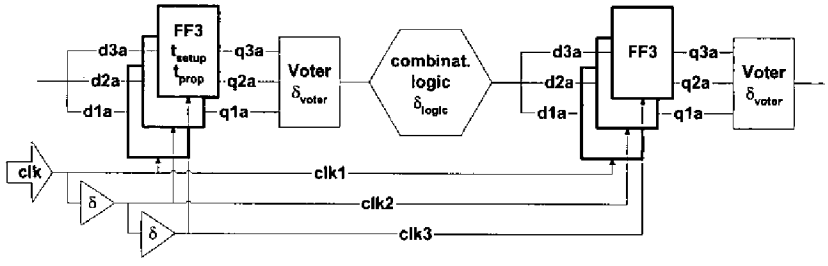
SET-tolerance by skewed clocks

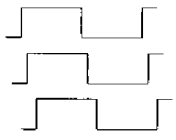


Impact of SEU mitigation on the design flow

- ***Insertion of SEE protected flip-flops to the design***
  - In HDL source code for dedicated space designs
  - Netlist post-processing for 3rd party IPs
  - Synthesis constraints selectively using hardened flip-flops
- ***Increased complexity affects the design flow and –results***
  - Large netlists with higher cell and node count
  - Increased run-time or even crashes of EDA tools
  - Desin optimisation is less efficient
- ***Synthesis tools try to remove redundancy***
- ***Timing issues***
  - TMR voting and clock skewing reduces maximum speed
  - Increased area leads to higher interconnect delay
  - Clock skewing can be removed by hold-time fix
- ***Verification and test issues***
  - TMR and formal verification (1 FF in RTL → 3 FF at gate level)
  - TMR (= redundancy) affects testability in scan testing
  - Implementation of protection has to be verified at netlist level

TMR Timing Issues

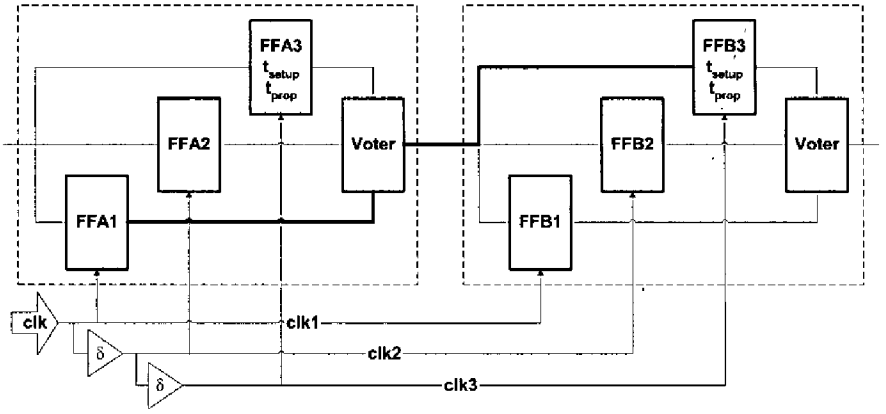




$$\text{Cycle Time } T >= t_{prop} + \delta_{logic} + t_{setup} + \delta_{voter} + 2\delta$$

TMR voters and clock skewing reduce operating frequency

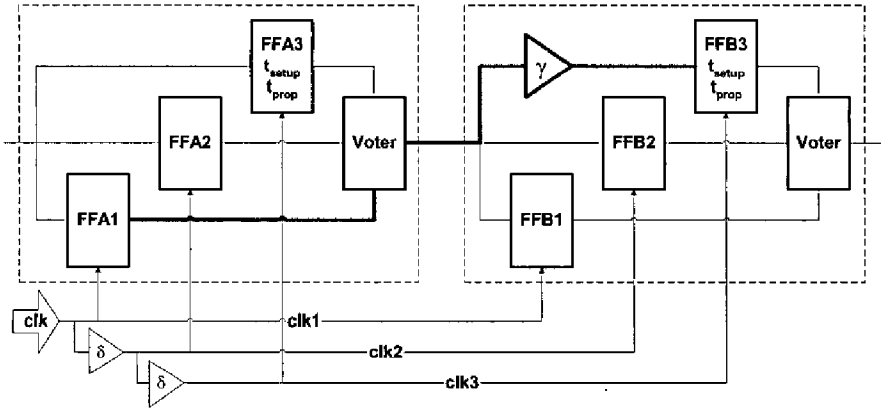
Hold violations with skewed clocks



When propagation delays $(t_{prop}$, voter$) < (2\ \delta)$ *clock skew*

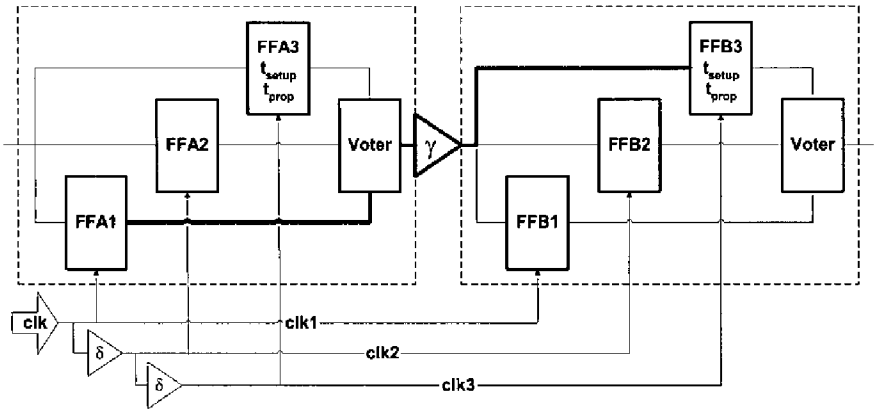
⇒ hold violation FFA1 → FFB3

Wrong hold fix by EDA tool



Automatic buffer insertion by fix-hold of synthesis tool compensates clock skew → and spoils SET protection

Correct hold fix



Inserting delay buffer between two entire TMR flip-flops...

➔ SET protection through clock skew conserved

Future perspectives

- ***SEU protected flip-flops available for many technologies***
  - ... but SET protection is currently in experimental stadium
- ***SEU and SET protected flip-flopd as library cells***
  - ... nice to have, but
- ***... if not available - workaround: build SET flip-flop as macrocell***
  - Compose TMR with temporal voting out of standard library cells
  - Generate appropriate front-end synthesis library for the TMR cell
  - Script-replace TMR cells by standard cell triplet in the gate-level netlist
  - Group and freeze the macrocells for timing fix and hold-fix
  - Place and Route with standard foundry design flow
- ***Advantages***
  - Can be implemented with a standard vendor library
  - No need to modify design at source code level
  - Avoids many problems with design flow and tools
- ***Issues***
  - Constraints on backend flow
  - Hardening of clock and reset trees to be considered

Conclusion

- ***SEU and SET protection possible with commercial ASIC libraries***
- ***Price in form of performance, complexity, power consumption***
- ***Pitfalls in the design flow with commercial EDA tools***
  - Requires workarounds, scripting and proper constraining
- ***Hardened flip-flops easier to use than building TMR in source code***
  - Hardened library cells, fixed Macrocells composed of commercial library cells
  - But there will always be a price to pay (speed, area, power…)
- ***Is full SEU protection always necessary?***
  - Determine upset rate of a given design (sub-function) in a given orbit
  - Determine the impact of an upset at system level
  - Apply selective use of SEU protection
- ***What about LATCHUP?***
- ***Questions? – Contact us…***
  - http://www.estec.esa.int/microelectronics
  - Roland.Weigand[at]esa.int