HIVAC - VASP1 ASIC

Contract 4200019872

Final presentation

Sept 2014

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THALES ALENIA SPACE

European Space Agency
Agence spatiale européenne

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Agenda

- Introduction on HIVAC contract
  - HIVAC Activity
  - VASP0 ASIC development
- VASP1 ASIC development
  - Specification
  - Design
  - Manufacturing
  - Electrical test
  - Radiation test
- VASP1 datasheet
- VASP1 application
- FM production
- Conclusion

- **Introduction on HIVAC contract**
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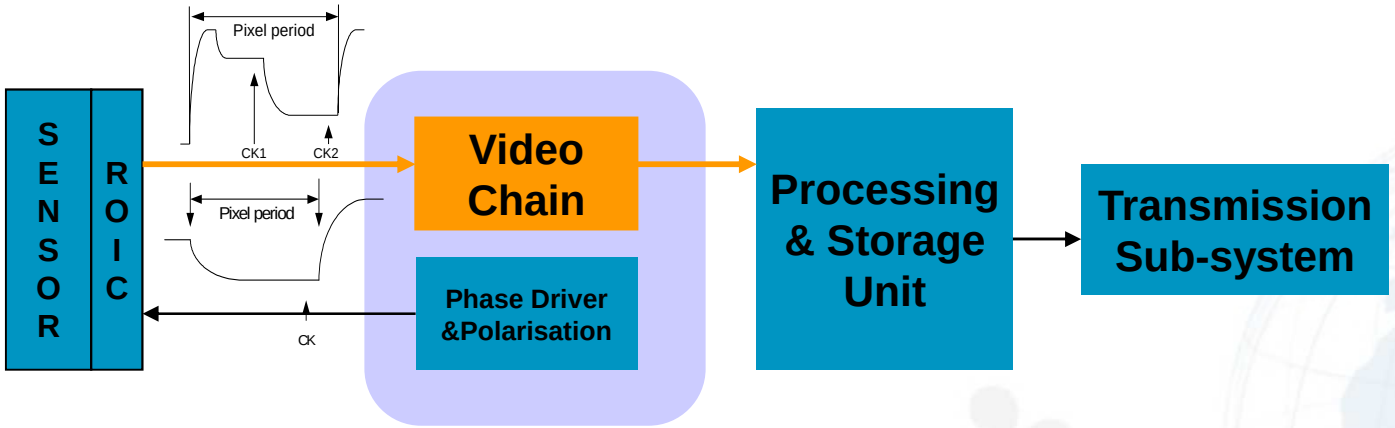
Project Context

- Optical satellite instruments, Earth observation and avionics units :[4]
  - use widely Charge Coupled Devices and CMOS Active Pixel Sensors
  - Need a specific conditionning of the analog signals from the read-out circuits before processing and storage, including :
    - Amplification and filtering
    - Analog to digital conversion
  - Challenging constraints
    - Performance : Noise reduction, sensitivity maximisation, power dissipation
    - Environment : temperature range, radiation, lifetime
    - Increase the integration level



HIVAC Activity

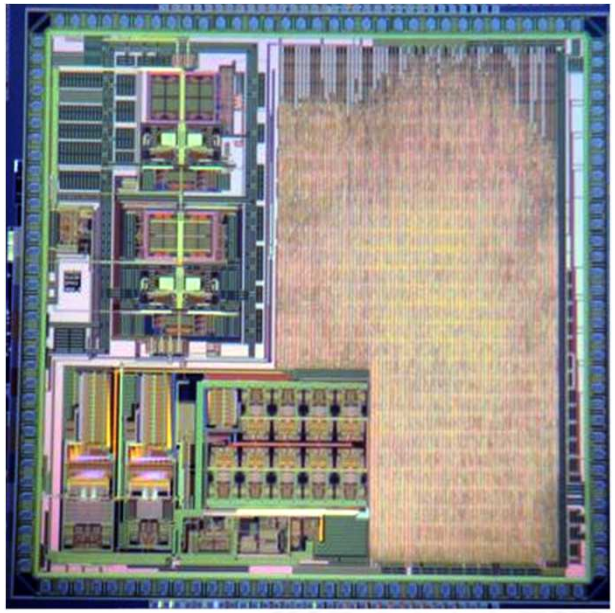
- **ESA has initiated the HIVAC activity (07/2006)**
  - **H**ighly **I**ntegrated **V**ideo **A**cquisition **C**hain
  - Contract n°4200019872
  - Thales Alenia Space granted as Prime contractor
  - Design and validation of a video acquisition IC :

    VASP = CDS + ADC

VASP0 development

- **In the frame of HIVAC contract, VASP0 ASIC has been developed**

- **VASP0 Activities :**
  - Detailed design Layout and simulations
  - Foundry / prototypes manufacturing
  - Test bench design and manufacturing for functional tests
  - VASP functional tests on all prototypes
  - Performance characterization
  - Radiation tests (TID)



- **Sub-contractor withdrawn after ADC block design**
- **TAS-F finalized the VASP0 design up to top level**

VASP0 specifications

Technology	**0.35µm**
Power Supply	**3.3V**
Power dissipation	**350 mW**
Analog functions	**CDS or single sampling** **PGA 1 to 8 by step of 1** **ADC**
Pixel frequency	**From 100 khz to 3 Mhz**
Input signal type	**CCD and CMOS compatibility**
ADC resolution	**16 bits**
Noise	**< 2 Lsb**
ENOB	**> 14 bits**
DNL	**< 1 Lsb**
INL	**< 3.5 Lsb**
TID	**50 krad**
Latchup immunity	**> 70 MeV.cm²/mg**
Operational temperature range	**-55℃ to 125℃**
Full performance temperature range	**0℃ to 30℃**

VASP0 results

- **100% functions validated from -30℃ to +80℃**

- **Very good electrical performances**
  - Excellent noise
    - Observed degradation in some modes (reference stability issue)
  - Excellent linearity on the 16-bit ADC
    - Observed calibration overflow
    - Observed test bench limitations for accurate measurements
  - PGA not necessary: all the video chain is integrated

- **Radiation test**
  - Analog hardening working well
  - Digital not yet hardened

Special thanks for very good VASP0

- **CHIPIDEA :** Jorge GUILHERME (ADC designer)
- **TAS-France :** Didier CHEFDEVILLE (project leader)
  Claude NEVEU (video chain expert)
  Philippe Ayzac (VASP0 responsible)
  Fabien TAUZIAC (VASP0 testing)
- **TAS-Italy :** Edoardo TADDEI (VASP0 testing)
- **ESA :** Wahida GASTI (VASP0 technical officer in ESA)

And the many other people !

VASP1 upgraded development contents

- **Digital library hardening**
  - Creation of ~50 hardened cells (schematic, layout)
  - Verification of the design
  - Characterization of timings and library generation
- **Analog design upgrade**
  - Voltage reference improvement
  - Completion of hardening (< 10% of analog part)
- **Foundry, packaging, tests**
- **Qualification in full compliance to ECSS-Q-ST-60**

Additional improvements

- **Initiated by TAS during VASP upgrade design with ESA approval**
  - Remove the PGA
  - Review the calibration algorithm to remove the overflow
  - Increase of the ADC working frequency from 3 to 4 MHz
  - Integrate the low noise, high speed reference buffers
  - Integrate a clamp function
  - Integrate a pixel bus tri-state interface

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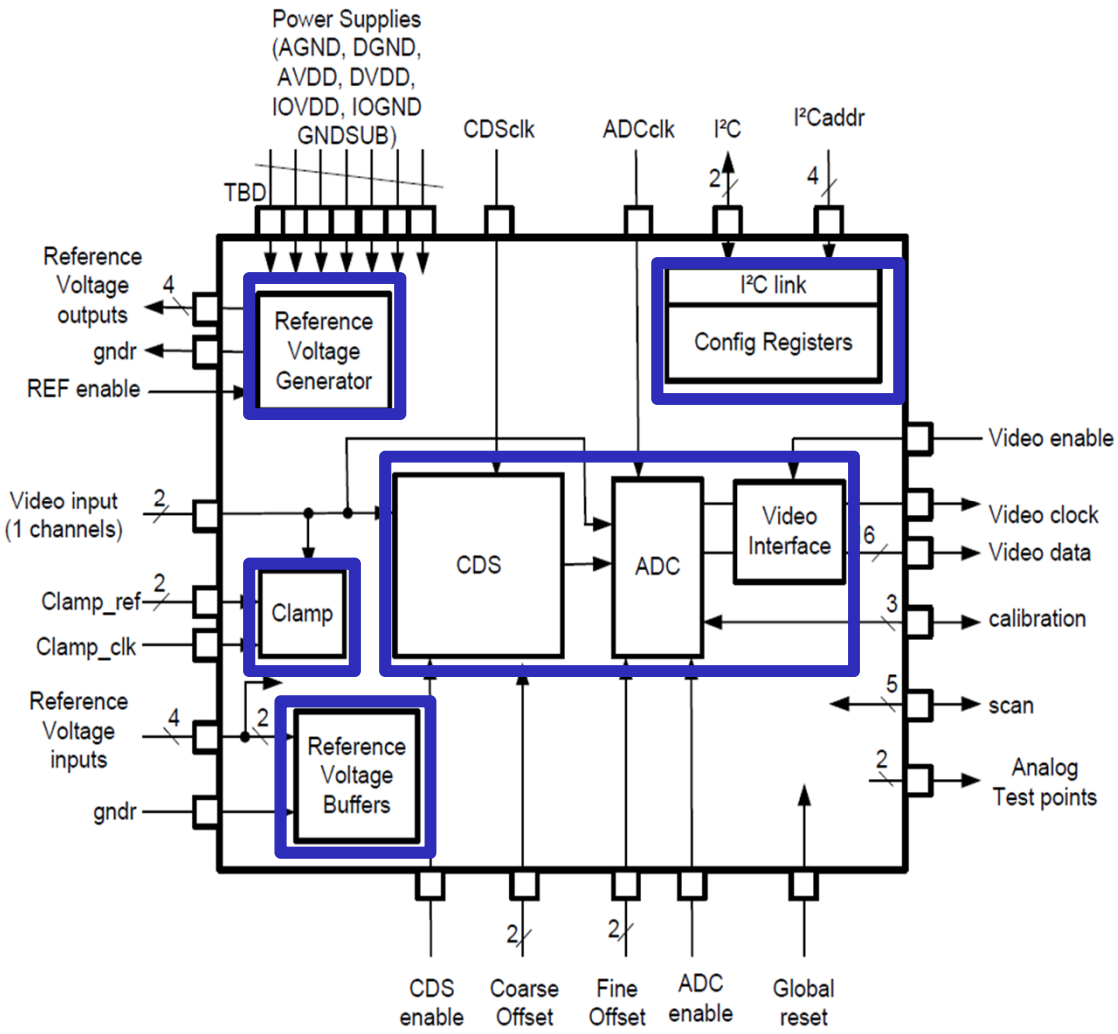
VASP1 specification / architecture

- High performances CDS and 16-bit ADC, both running up to 4 MHz
- Multi-sampling per pixel capability
- Clamping circuit to manage detector DC voltage.
- Bandgap and VCM voltages generation. External references can also be used.
- Serial interface for configuration
- Internal reference buffering



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VASP1 detailed design

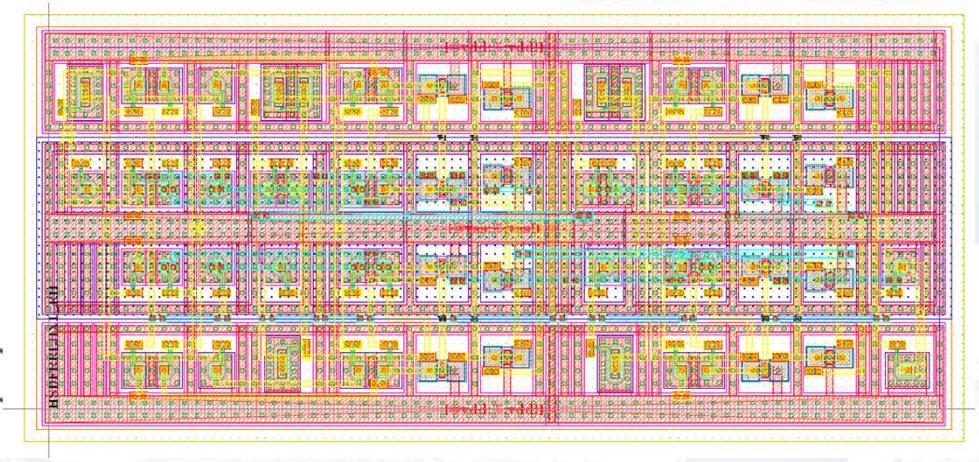
- Radiation hardening of digital library
- Voltage reference review
- Analog hardening completion
- PGA removal
- Calibration algorithm review
- Increase of the ADC working frequency from 3 to 4 MHz
- Integrate the low noise, high speed reference buffers
- Integrate a clamp function
- Integrate a pixel bus tri-state interface

Radiation hardened digital Library

- 56 logic cells, 14 layout cells, 5 digital I/Os

- **Radiation Hardening By Design**
  - TAS internal rules for schematic and layout
  - DICE register creation
  - Cell improvements to maintain the timing performances

- **Drive CAD company for complete characterization**
  - Functionality check
  - Arc timing extraction
  - Generation of digital tool format

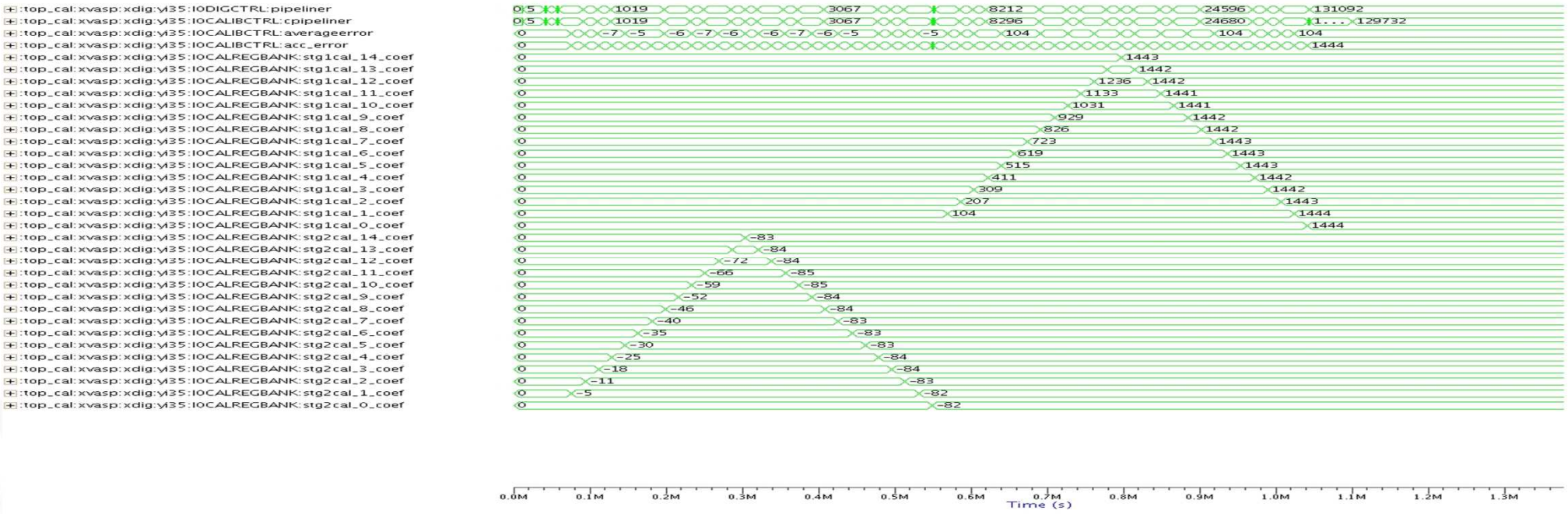


Voltage reference review

- **Review stability of the core circuit (banggap)**
- **Allow the use of external references**
  - Separate generator output pins from buffer input pins
- **Review the trim capability**
  - Band-gap temperature slope
  - Common mode absolute value
  - VREF absolute value

Linearity calibration algorithm

- **Find an improvement in the algorithm**
  - Need to take into account ADC amplifier offset
  - Improved algorithm, derived from the existing one
  - Improved algorithm simulated in mixed-mode simulation

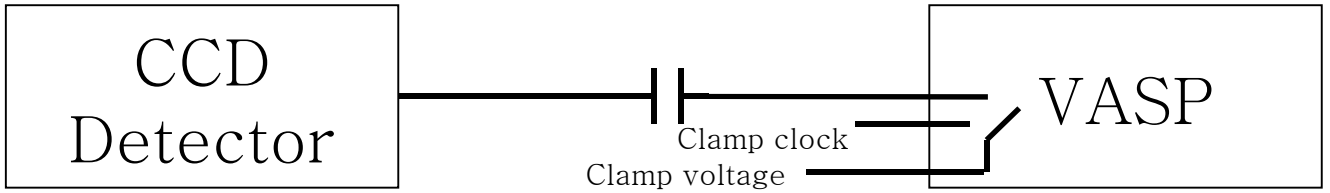


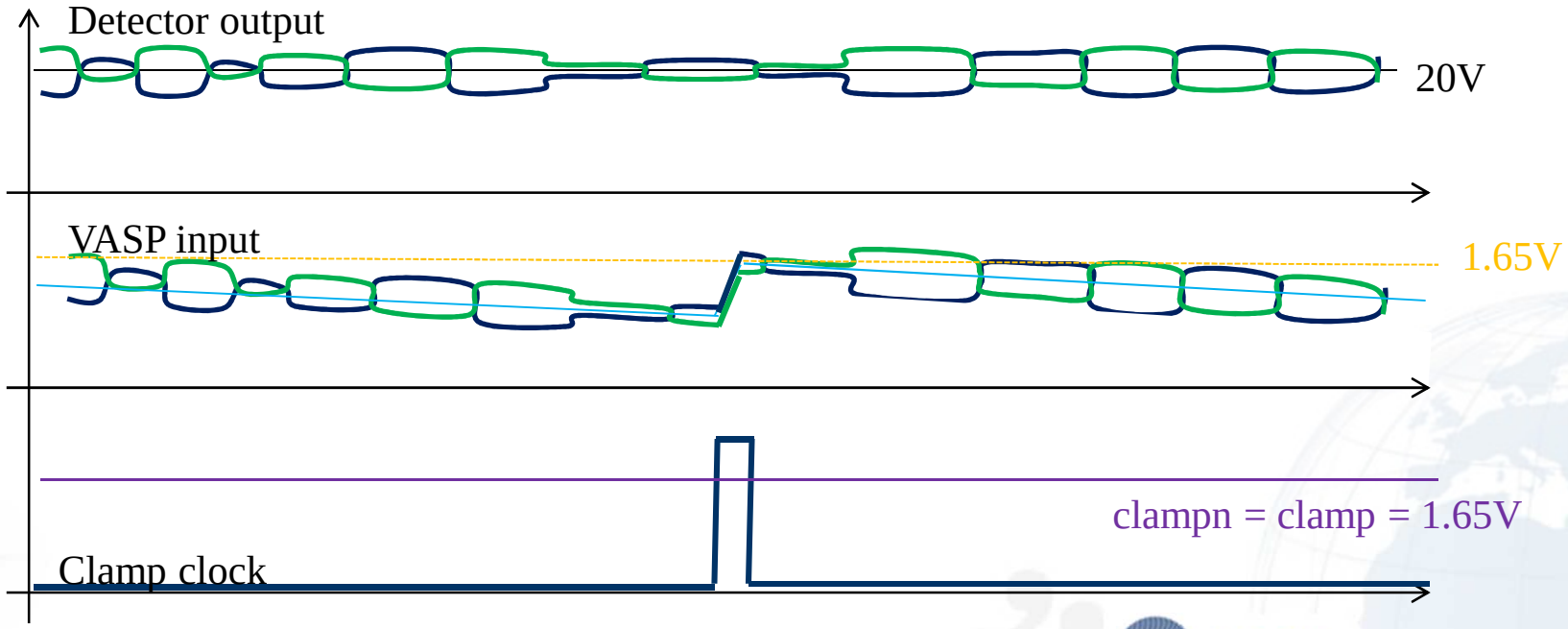
Reference internal buffering

- **Reference need to be buffered for CDS, ADC use**
- **Specifications**
  - Low consumption
  - Low noise
  - High gain and bandwidth
  - Large input and output dynamic range
- **Those differential buffers have been integrated**
- **Offset correction inputs (COC and FOC) have also been buffered**

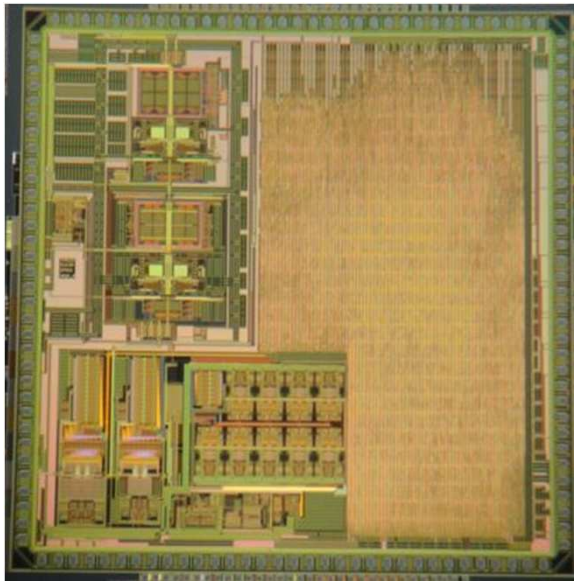
Clamp function

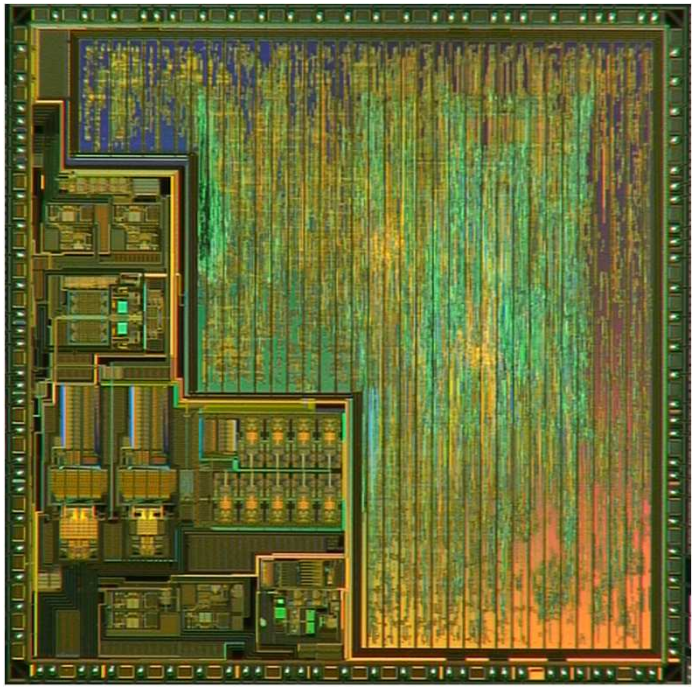
- The clamp is used with CDD detector to bias the decoupling capacitor that is needed to go from detector high voltage to VASP low voltage.





VASP evolution





VASP0 - 39mm² - 132 IOs

Hardening : Analog 90% - Digital 0%

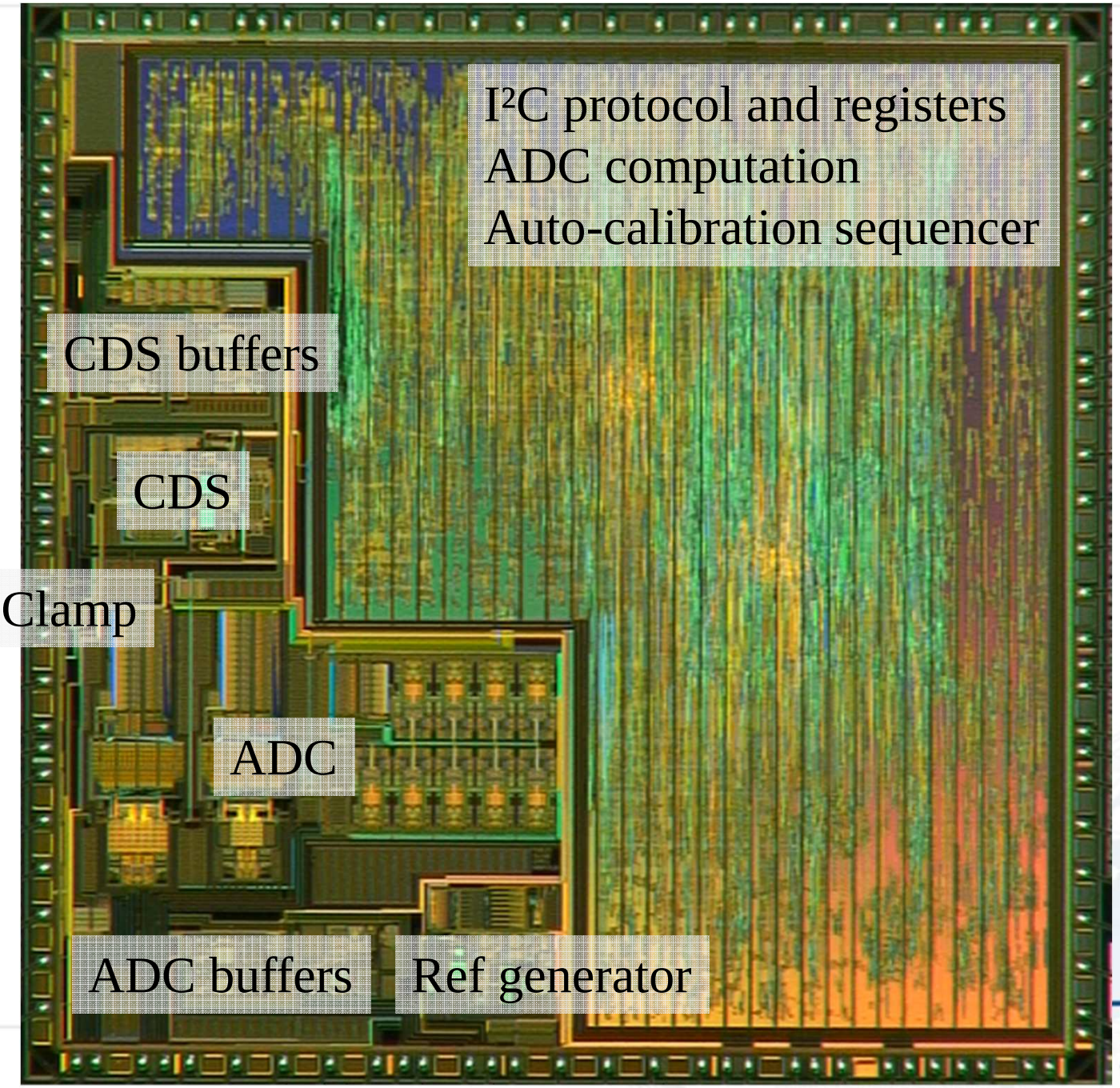
ADC only consumption : 35 mA typ

VASP1 - 81mm² - 108 IOs

Hardening : Analog 100% - digital 100%

ADC only consumption : 55 mA typ

Layout



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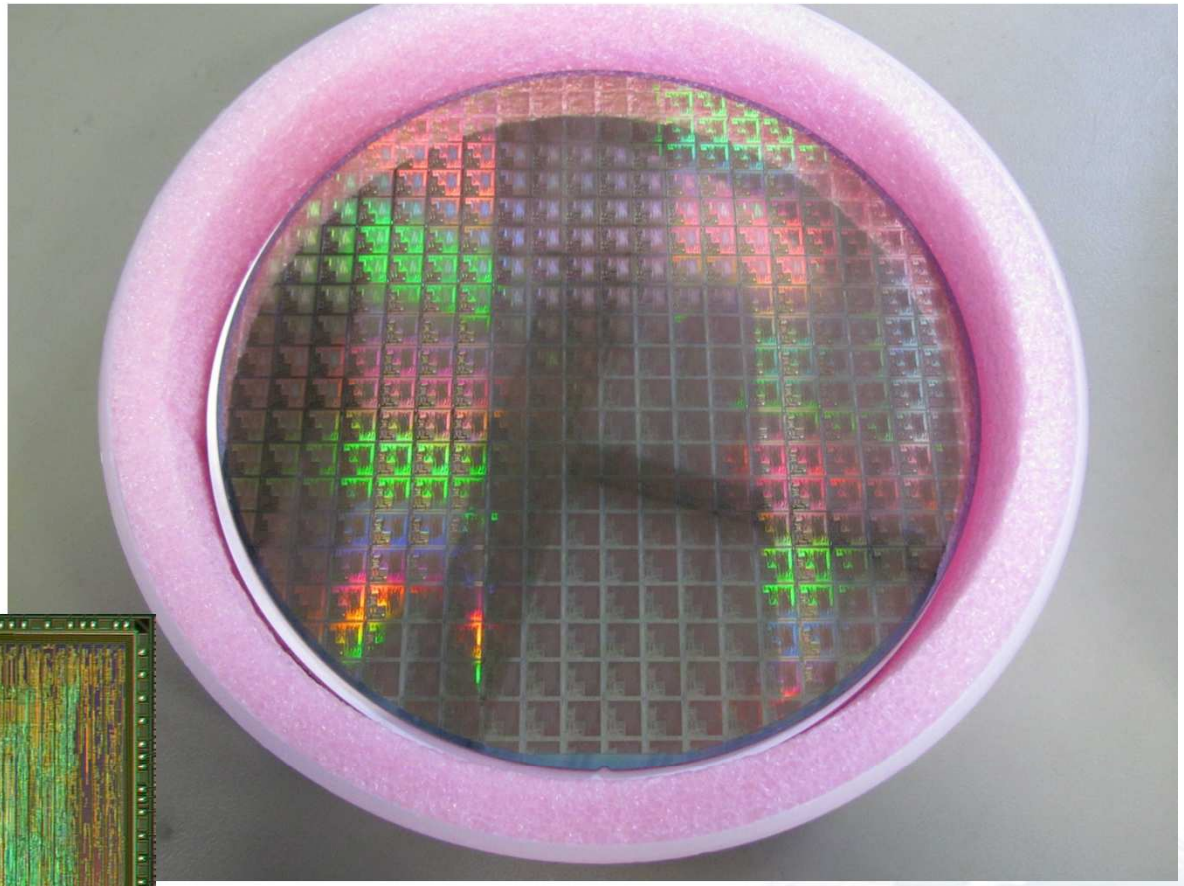
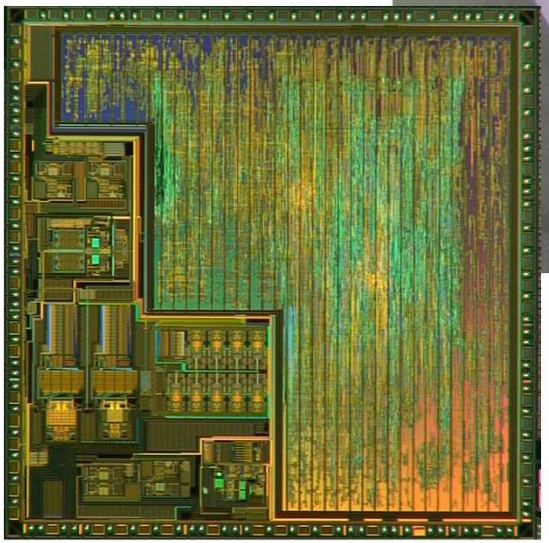
Wafer and Die

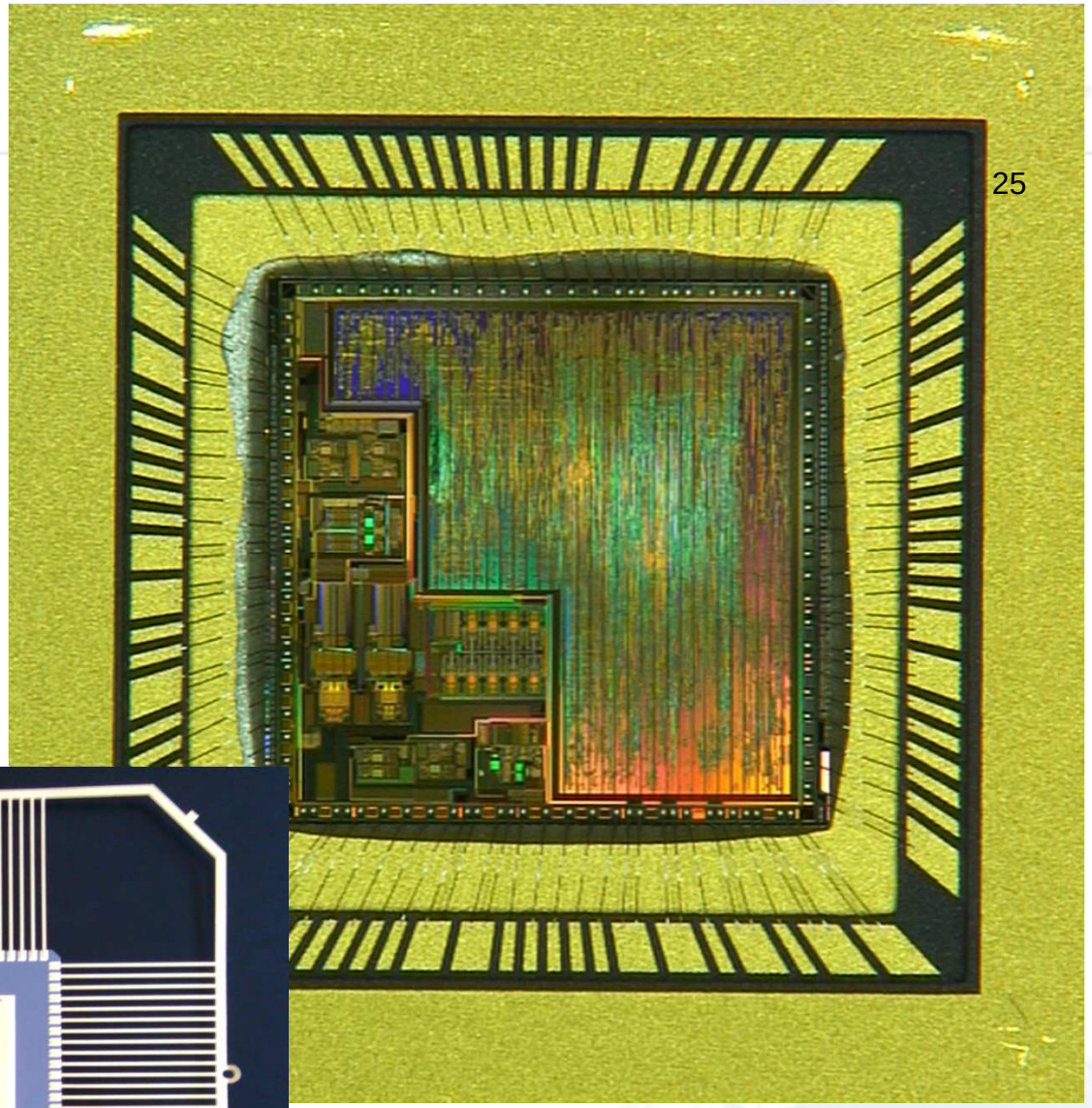
- **XFAB 0.35 µm CMOS**
  - 8’’ wafers
  - 250 VASP1 / wafer
  - 3 months manufacturing
  - Delivery on time
  - PCM available

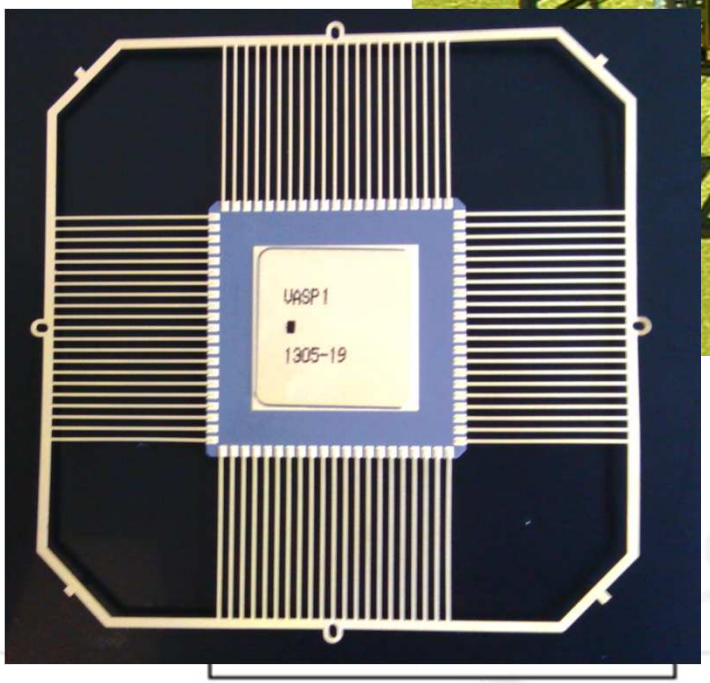




Package part

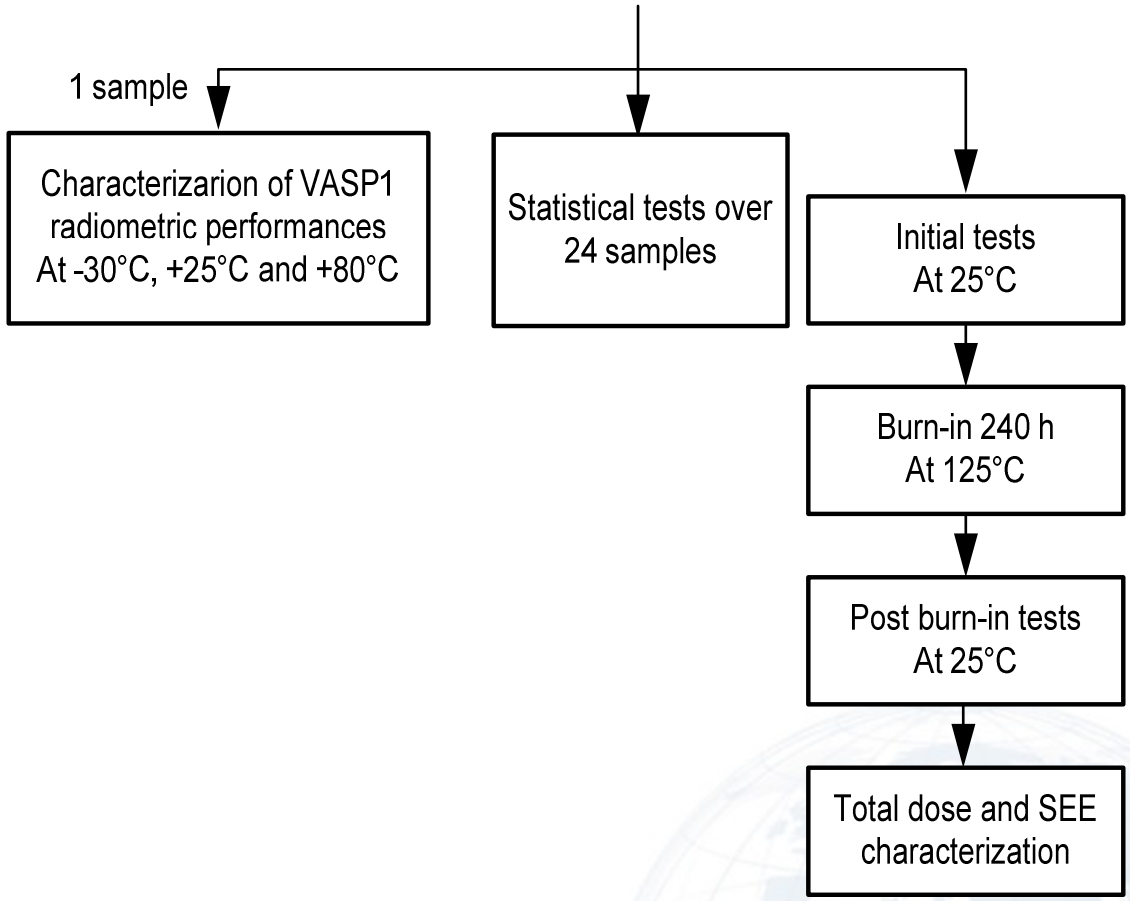
- **HCM assembly**
  - CQFP84
- **SERMA technology**
  - Wafer sort
  - Packaged electrical test
  - ESCC 9000 test





Validation plan

- **The test plan consists in :**
  - The full characterisation of one sample
  - Statistical tests on ~25 samples
  - Radiation tests (TID and SEE).



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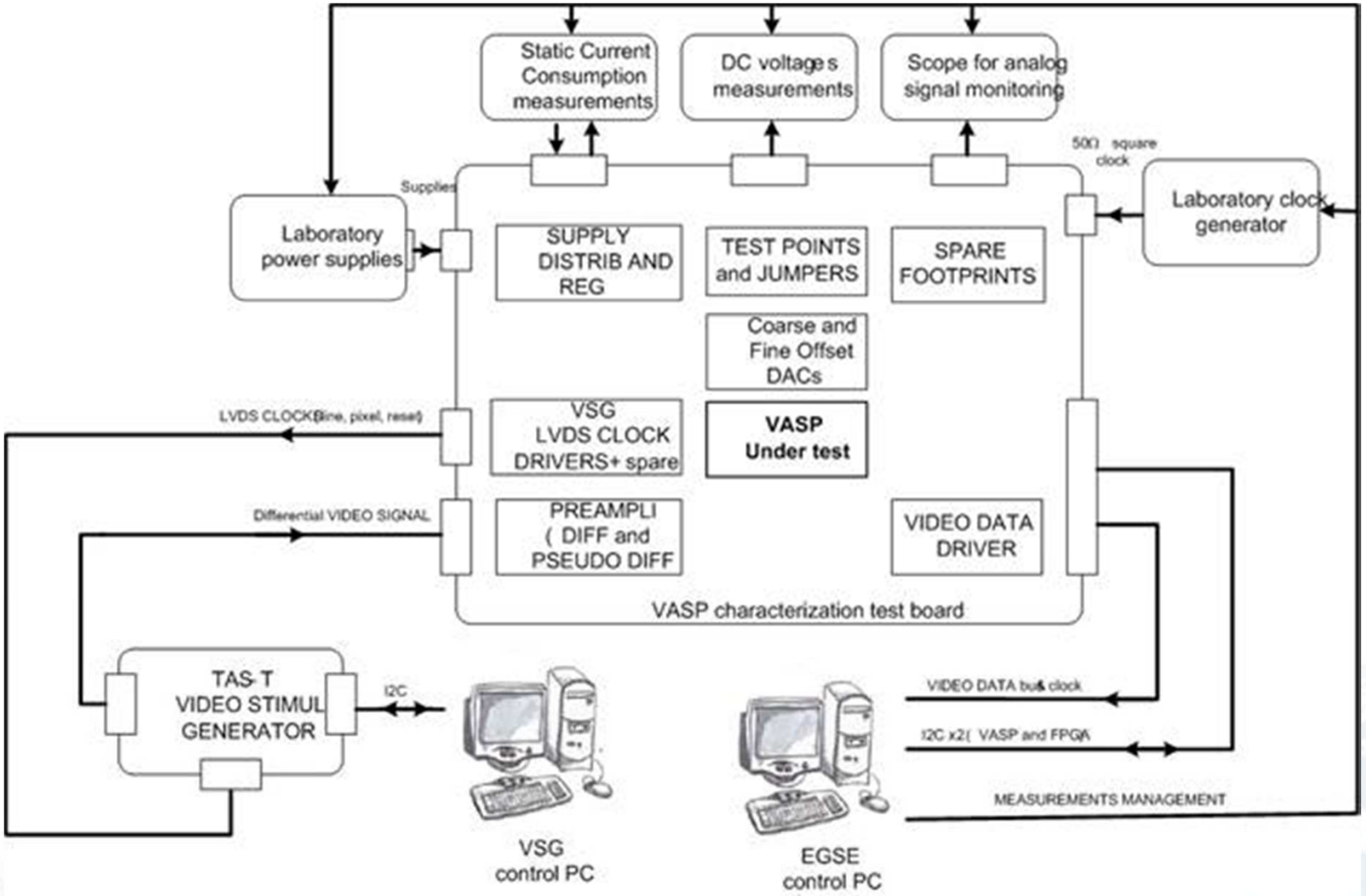
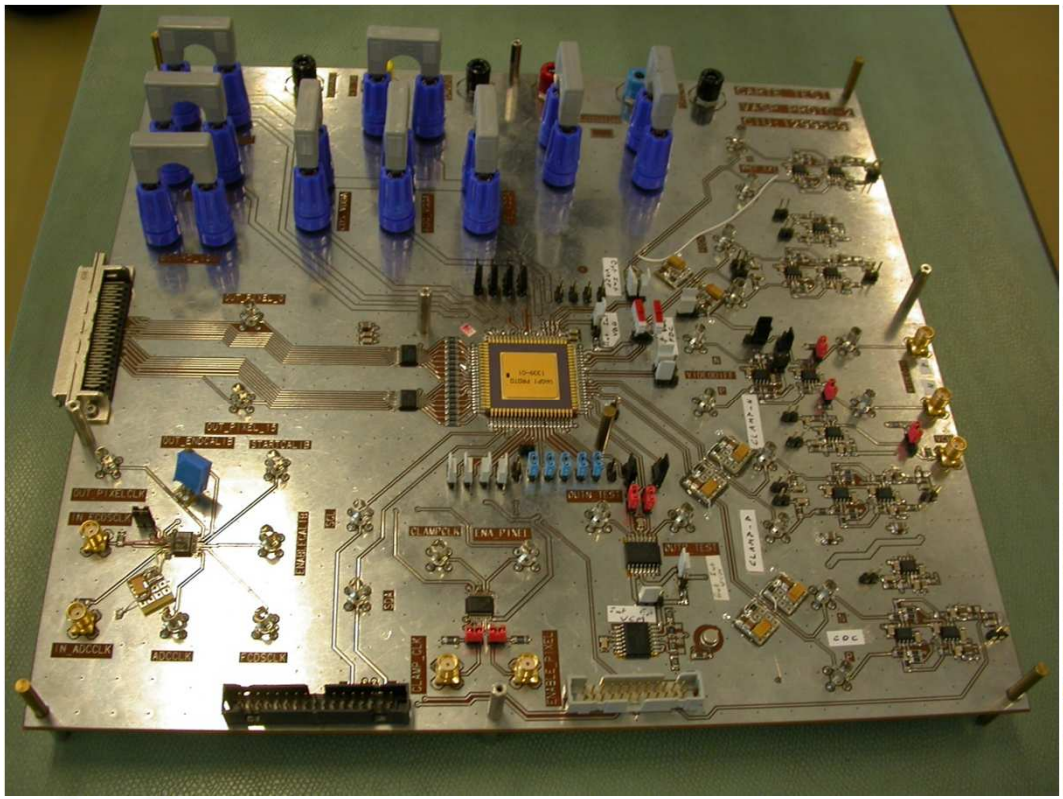
VASP1 EGSE

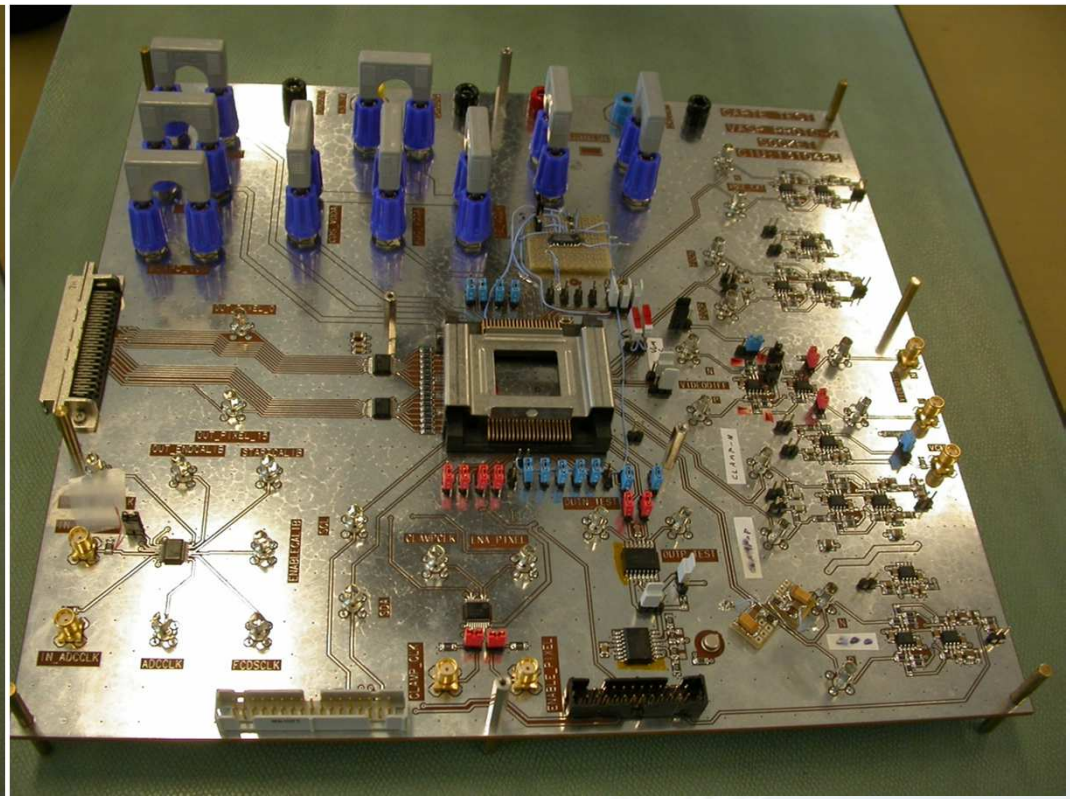

Static Current Consumption measurements
DC voltages measurements
Scope for analog signal monitoring
50Ω square clock
Supplies
Laboratory power supplies
Laboratory clock generator
SUPPLY DISTRIB AND REG
TEST POINTS and JUMPERS
SPARE FOOTPRINTS
Coarse and Fine Offset DACs
LVDS CLOCK(line, pixel, reset)
VSG LVDS CLOCK DRIVERS+ spare
VASP Under test
Differential VIDEO SIGNAL
PREAMPLI (DIFF and PSEUDO DIFF
VIDEO DATA DRIVER
VASP characterization test board
TAS-T VIDEO STIMUL GENERATOR
I2C
VIDEO DATA bus & clock
I2C x2 (VASP and FPGA
MEASUREMENTS MANAGEMENT
VSG control PC
EGSE control PC

VASP1 EGSE / Test Boards

VASP1 Characterization Test Board



VASP1 Statistical Test Board



VASP1 characterisation results (1/5)

Power consumption

- Power consumption (3,3V / at 4 MHz)

Idd VASP1	Measure (mA)
CDS+ADC Mode Voltage references activated	103
CDS+ADC Mode Voltage references deactivated	94
ADC Only Mode Voltage references activated	55
ADC Only Mode Voltage references deactivated	48

- @ 100 kHz, 12 mA reduction

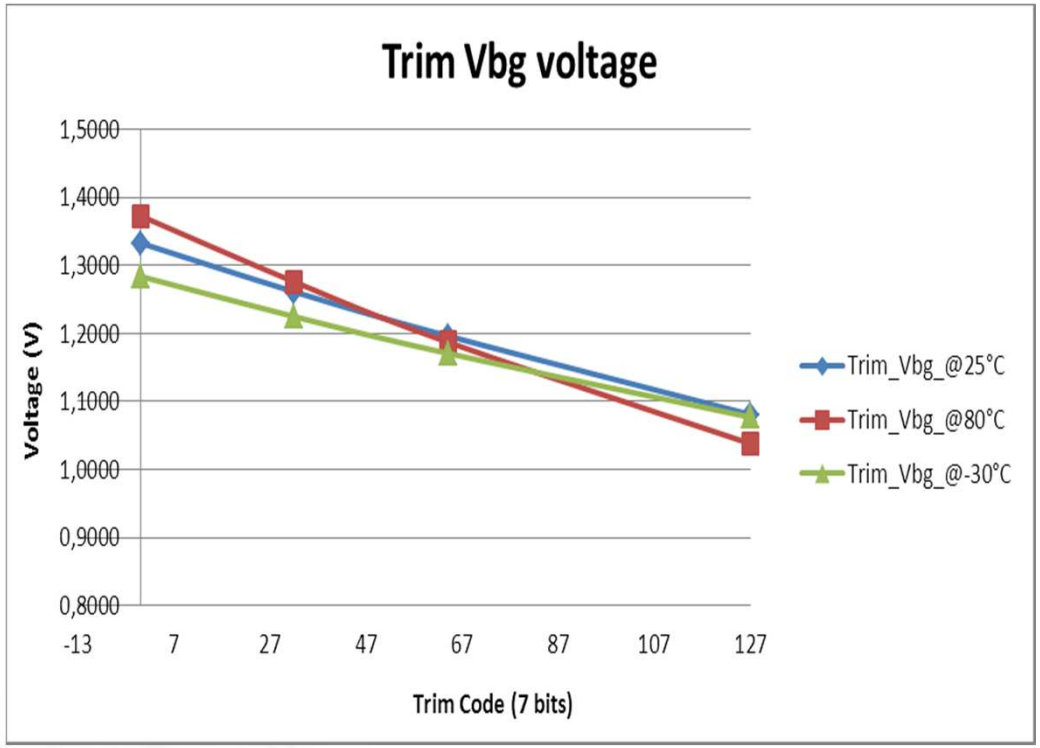
VASP1 characterisation results (1/5)

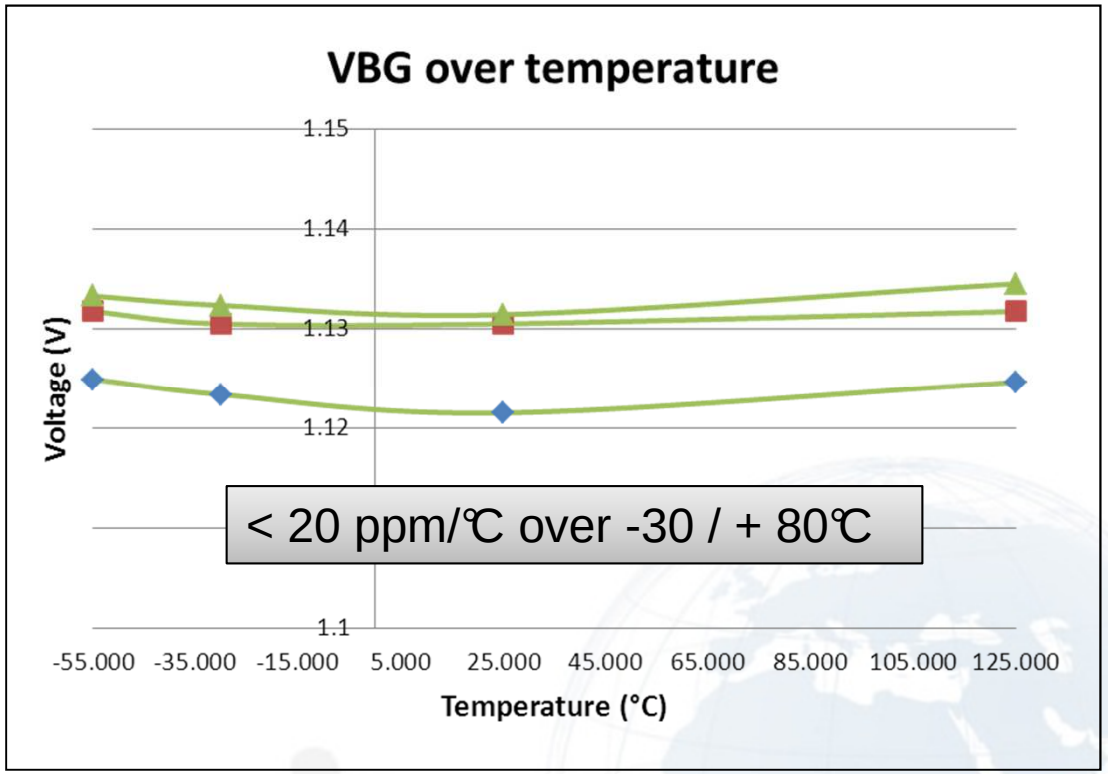
- **Digital**
  - All functionalities have been checked and are as expected
  - I/O parameters
    - Characteristics are as expected
  - I²C link has been validated up to 1 MHz
  - Digital scan ok

- **Clamp**
  - Functionality proven
  - Typ. ON resistance 70 Ohms

VASP1 characterisation results (2/5)

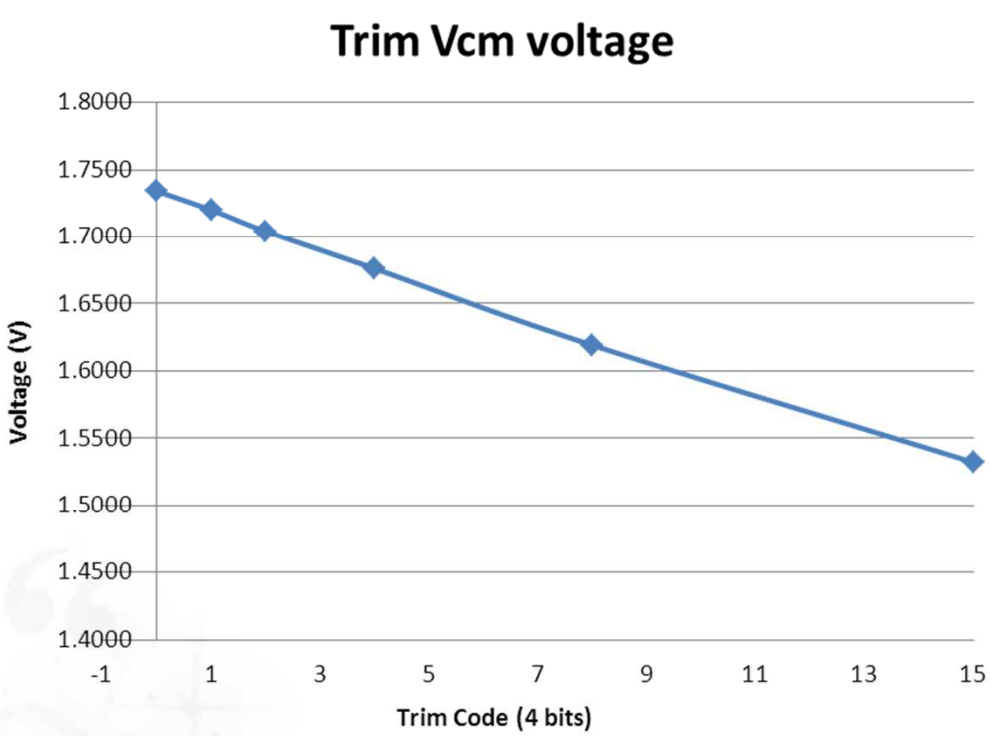
- Reference voltages
  - Temperature stability of VBG (bandgap) is programmable with a 7 bit word through I²C.

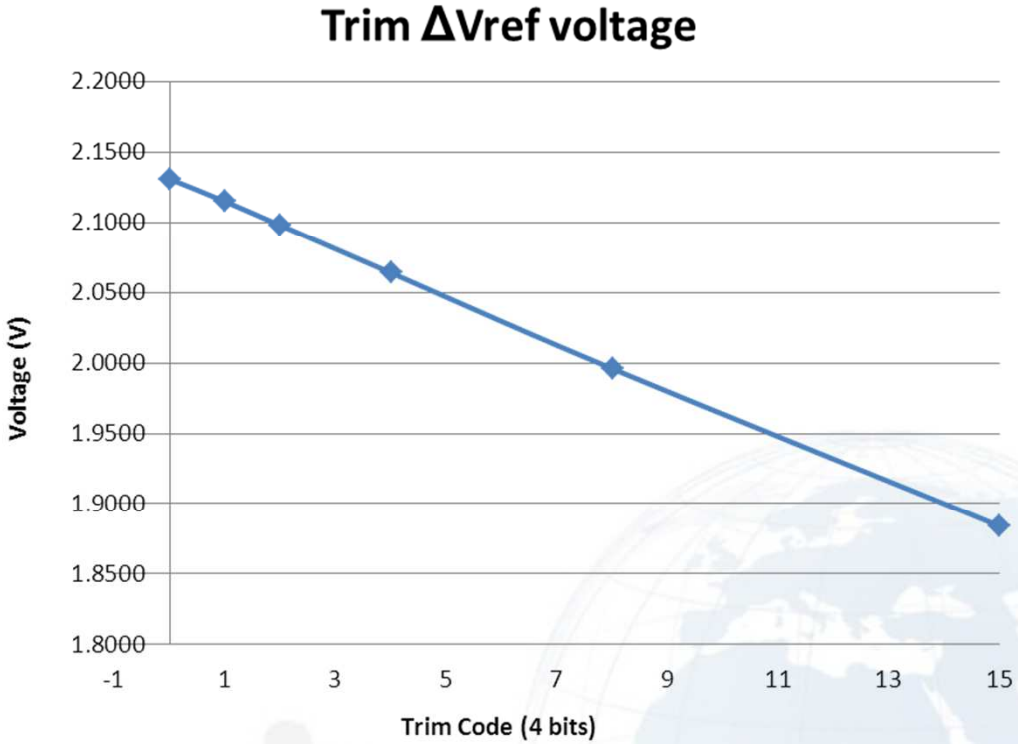




VASP1 characterisation results (2/5)

- Reference voltages
  - Reference voltages values (Vcm and Vref) are programmable with 7 bit words through I²C.



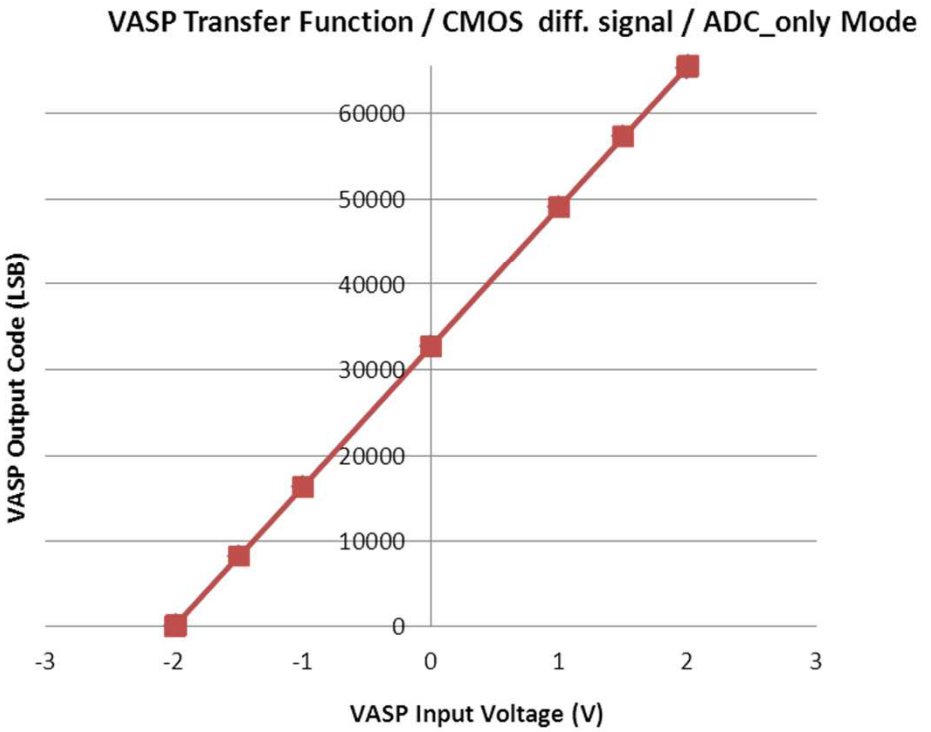


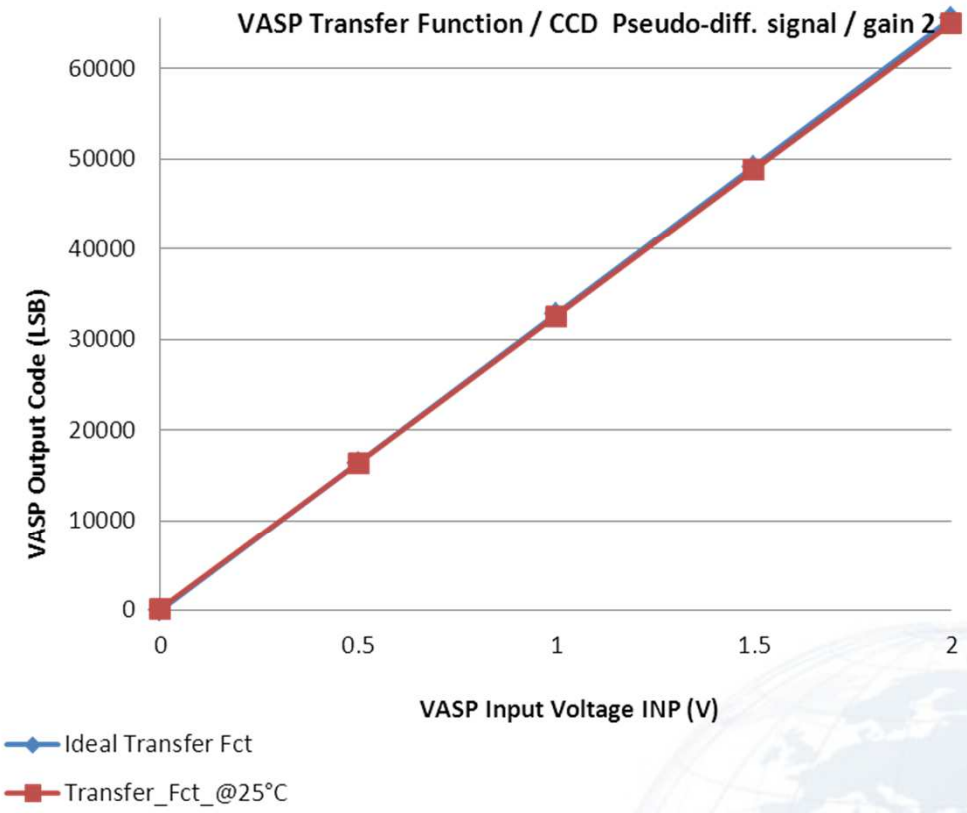
VASP1 characterisation results (2/5)

- **External reference**
  - Functionality proven
- **Internal buffers**
  - ADC and CDS reference voltage buffers validated
  - FOC and COC voltage buffers validated

VASP1 characterisation results (2/5)

Digital conversion transfer function





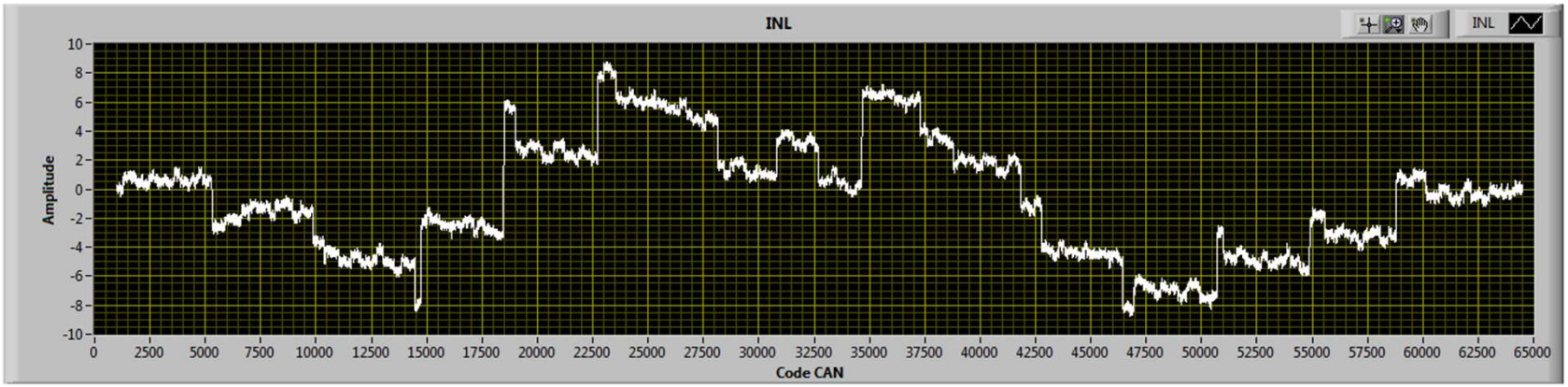
VASP1 characterisation results (3/5)

- Measured Input Referred Noise (LSB rms), at 4MHz

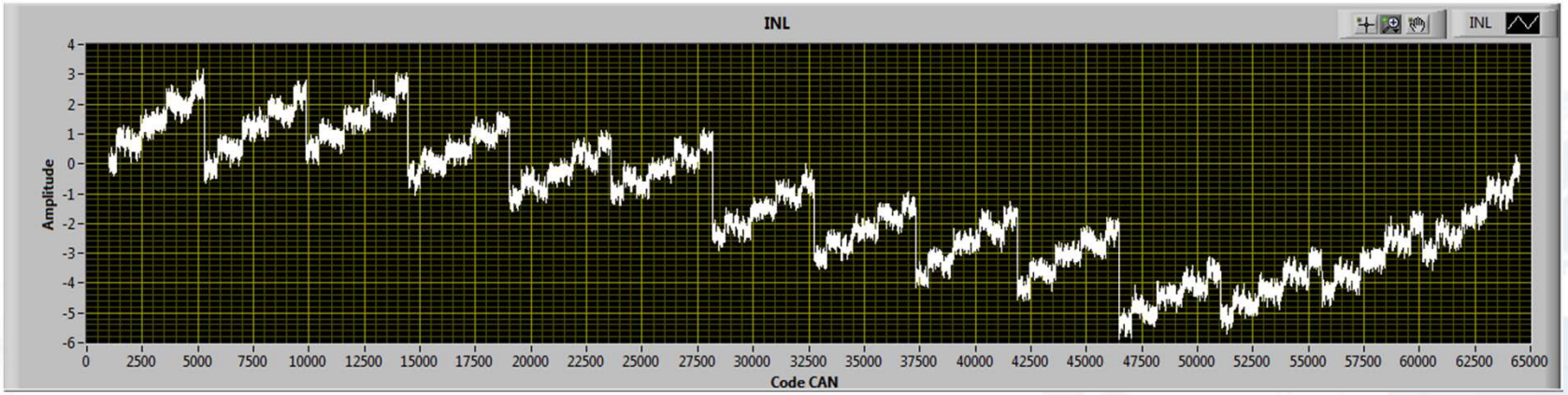
Temp	-30℃	25℃	80℃
CCD mode	2.3	1.9	1.9
CMOS mode	1.6	1.9	1.4
ADC only mode	0.7	0.8	0.85

VASP1 characterisation results (4/5)

- **Linearity calibration**, at 4MHz
  - **INL before calib (17.6 LSBpp)**

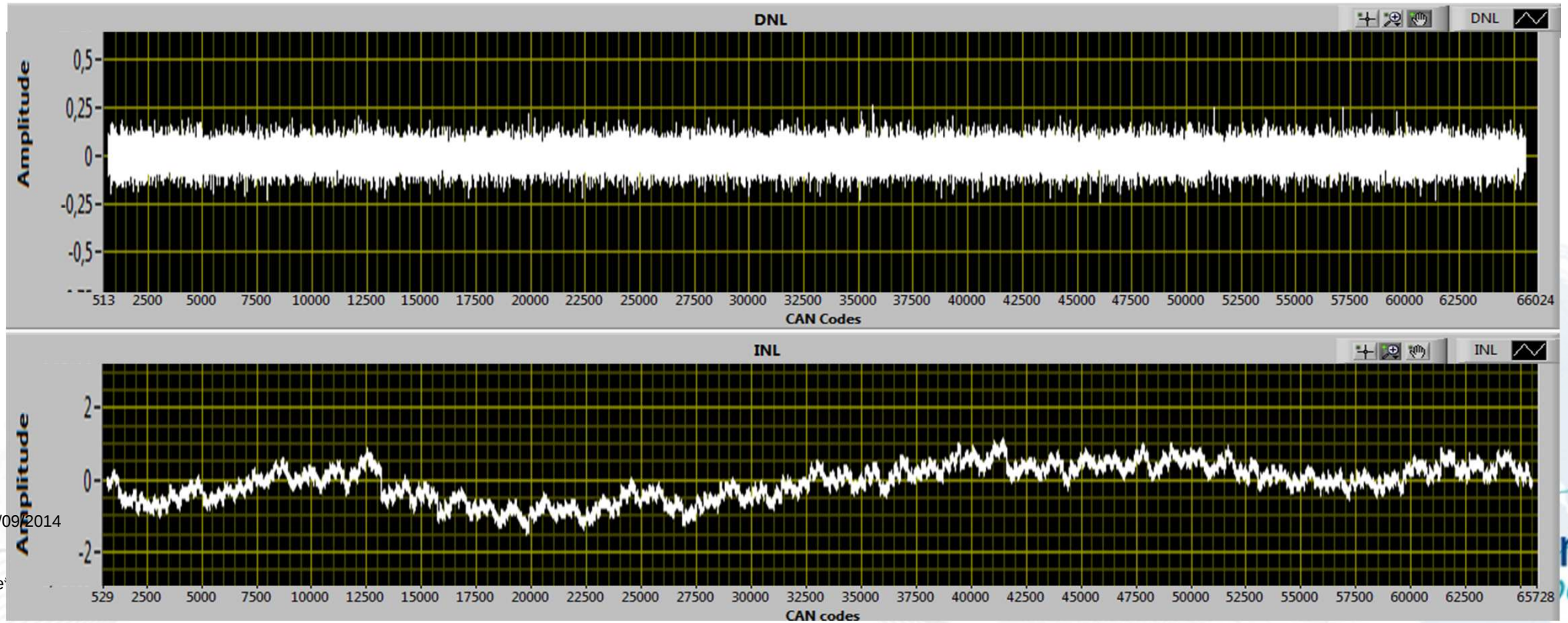


  - **INL after calib (9 LSBpp)**



VASP1 characterisation results (4/5)

- **ADC Linearity**, at 4MHz
  - ADC linearity has been measured on MTG bench with very good compensation of bench defaults.
  - Performance is measured after internal calibration
    - **Peak DNL is +0.26 Lsb and -0.26 Lsb** (< 0,5 Lsb expected)
    - **Peak to peak INL is 2.7 Lsb** (4 Lsb expected performance).



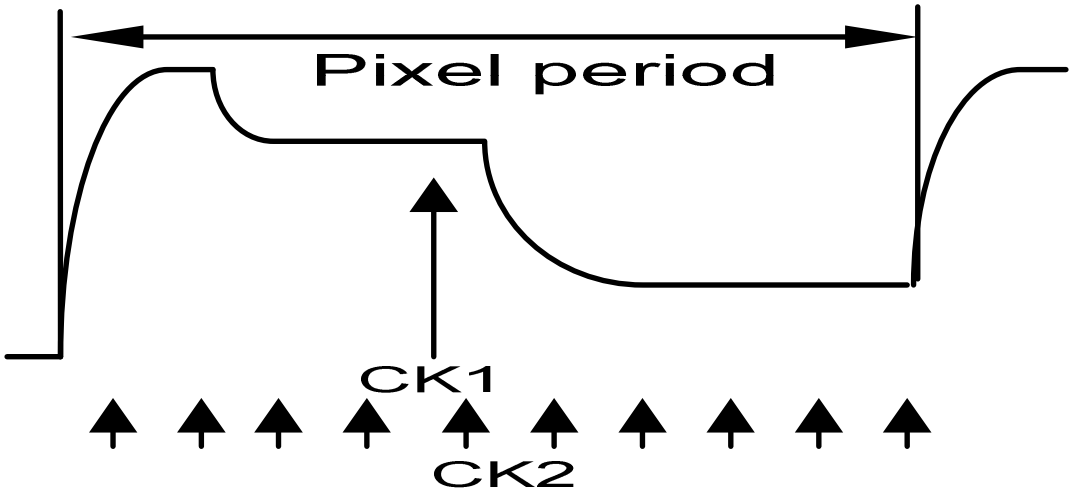
VASP1 characterisation results (5/5)

- **ADC Gain**
  - By principle, gain is exactly 2 x (Vrefp-Vrefn).
  - Gain stability is < 10 ppm/℃ after tuning (over 30 ℃ range)

- **Offset** (ADC only mode)
  - Offset < 50 Lsb
  - Offset stability : < 5 Lsb from -30℃ to +80℃ (ADC only mode)

VASP1 characterisation results (4/5)

- **Multi-sampling**
  - Allow noise reduction on low frequency pixel
  - Functionality proven



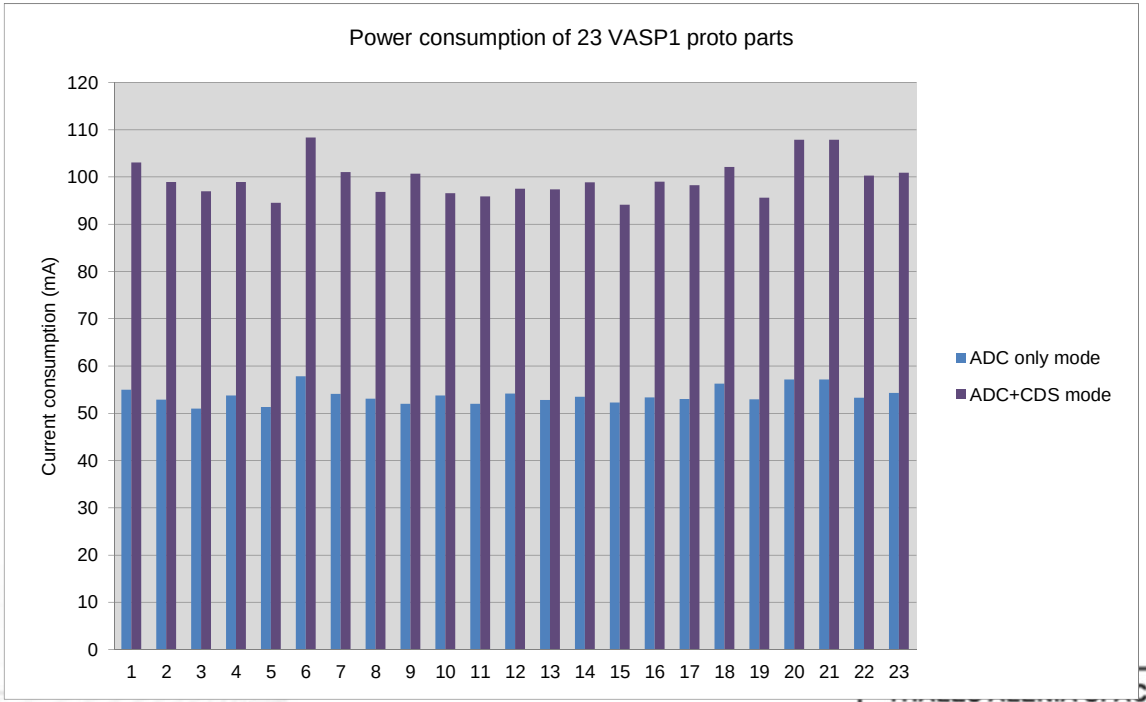
VASP1 characterisation results (4/5)

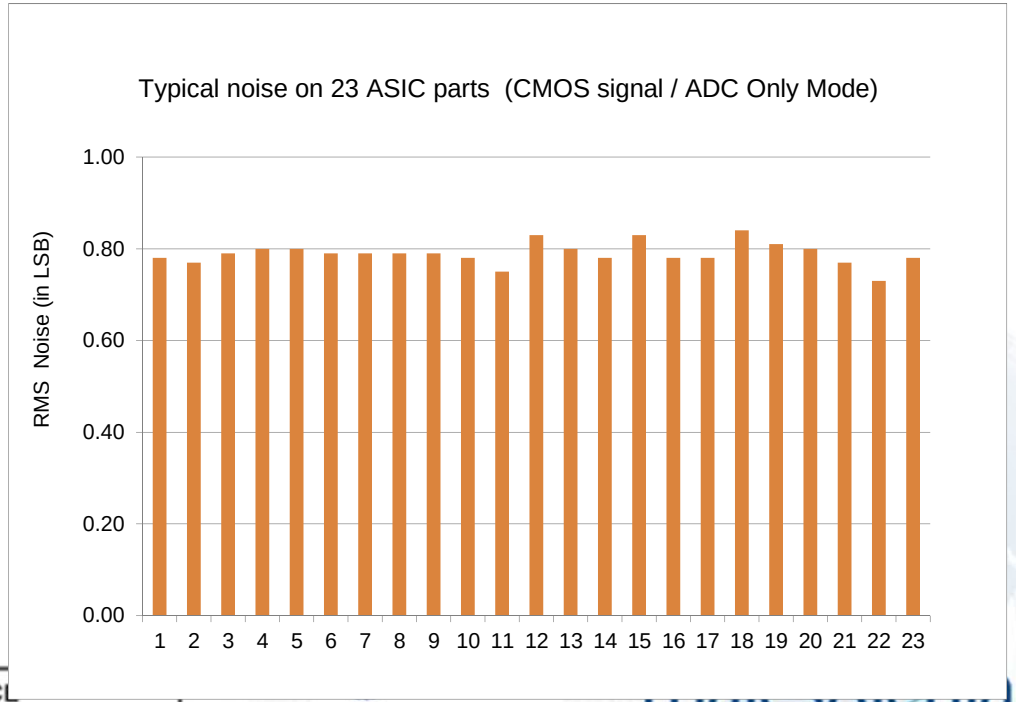
- **Offset correction inputs:**
  - Coarse offset correction (when CDS is used)
    - COCP-COCN injects a regular offset around 2V
    - The offset correction gain is one => ~ 16 LSB/mV
    - Functionality proven
  - Fine offset correction
    - FOCP-FOCN injects a regular offset around 0V (FOCP = FOCN = 1.65V)
    - The offset correction gain is one quarter => ~ 4 LSB/mV
    - Functionality proven

- **VASP1 intrinsic offset**
  - < 50 LSB
  - < 5 LSB variation over temperature range

VASP1 statistical results

- **VASP1 ASIC statistical tests are successful**
  - 23 of the 24 samples tested give OK result. (yield > 95 %)
    - The only sample NOK has manufacturing default. It is rejected only at this step because it was not tested by ASIC foundry.
  - Test results are very homogenous on all the samples tested are OK.





VASP1 characterisation synthesis

- The VASP1 validation tests confirmed
  - **functions and performances are compliant** to the ones described by its preliminary datasheet in the full frequency range and in the nominal temperature range.
  - Large margins are demonstrated by additional testing @ -30℃ and up to 5 MHz.

- Every good sample behaves the same way

VASP1 electrical validation is successful

- Introduction on HIVAC contract
  - HIVAC Activity
  - VASP0 ASIC development
- **VASP1 ASIC development**
  - Specification
  - Design
  - Manufacturing
  - Electrical test
  - **Radiation test**
- VASP1 datasheet
- VASP1 application
- FM production
- Conclusion

TID test

- **Board, program and measurement made by TRAD – Toulouse**

- **Dose**
  - ^{60}Co source
  - Steps : 0, 9, 23, 33, 43, 57, 72, 101 krad(Si)
  - ESCC 22900 Low dose rate : 210 rad(Si)/hour .

- **3 biasings**
  - ON with clock (4 parts)
  - ON without clock (3 parts)
  - OFF (3 parts)

- **Annealing**
  - 25℃ for 24h
  - 100℃ for 168h

TID results

- **Very few parameters drifted, within specifications**
  - Leakage current in the input digital IOs
  - Input current for pin having pull-up function activated
- **All others parameters are extremely stable**
  - Bandgap reference voltage (and associated voltages)
  - Chain offset
  - Consumption
  - ADC performances (Linearity, noise, offset)
- **Full recovery after annealing**

VASP1 is fully functional and specification compliant up to 100 krad(Si)

Heavy Ion tests

- **Board and program made by TRAD – Toulouse**
- **Measurement made by TRAD – UCL Louvain**

- **SEL** test monitoring of supplies

- **SET** test monitoring of :
  - Analog references
  - Erroneous digital conversion

- **SEU** testing monitoring of register map program and read back

- **SEFI** monitoring of abnormal behavior during test

Heavy Ion results

- **SEL**
  - **No SEL** @ LET=67.7 MeV.cm²/mg up to fluence of 1E7 ions/cm²
- **SEU**
  - Very low susceptibility of register : SEU LETth = 20.4 MeV.cm²/mg with ssat = 1E-06 cm²
  - Reset register sensitivity : LETth> 40.4 MeV.cm²/mg with ssat = 1E-07 cm²
  - **The probability of SEU is extremely low**
- **SET** :
  - **No SET observed on references** @ LET=67.7 MeV.cm²/mg
  - **ADC output code error** (criterion > 64 Lsb16) : LETth=10.2 MeV.cm²/mg with ssat = 6E-05 cm²
- **SEFI**
  - **No SEFI detected in any condition**

Conclusion on VASP1 design

- Based on the very good VASP0, we managed to complete the design of a Video Acquisition Signal Processor.

- Many thanks to the core team

  Philippe Ayzac, Anthony Berne, Jorge Guilherme, Claude Neveu, Jean-Marie Saveres, Franck Mariannie, Denis Lagarde, Marc Medard, Michel Carquet, Charly Bonnet, Sylvain Claireux, Michael Laine

- Many thanks to the whole team

  Jean-Marie Garigue, Sophie Di Santo, Emmanuel Liegeon, David Le Du, Laurent Venturini, Laurent Carre, Raoul Velazco, Kholdoun Torki

  and many other contributors…

- Many thanks to Wahida Gasti for her exigency and trust despite all challenges

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VASP1 datasheet

- VASP1 datasheet is available :
  - Title :

    VASP1 DATASHEET

  - Ref : 100535705O
    - issue 3.2
    - date 2014-07-04
- It provides full functional and performance information.

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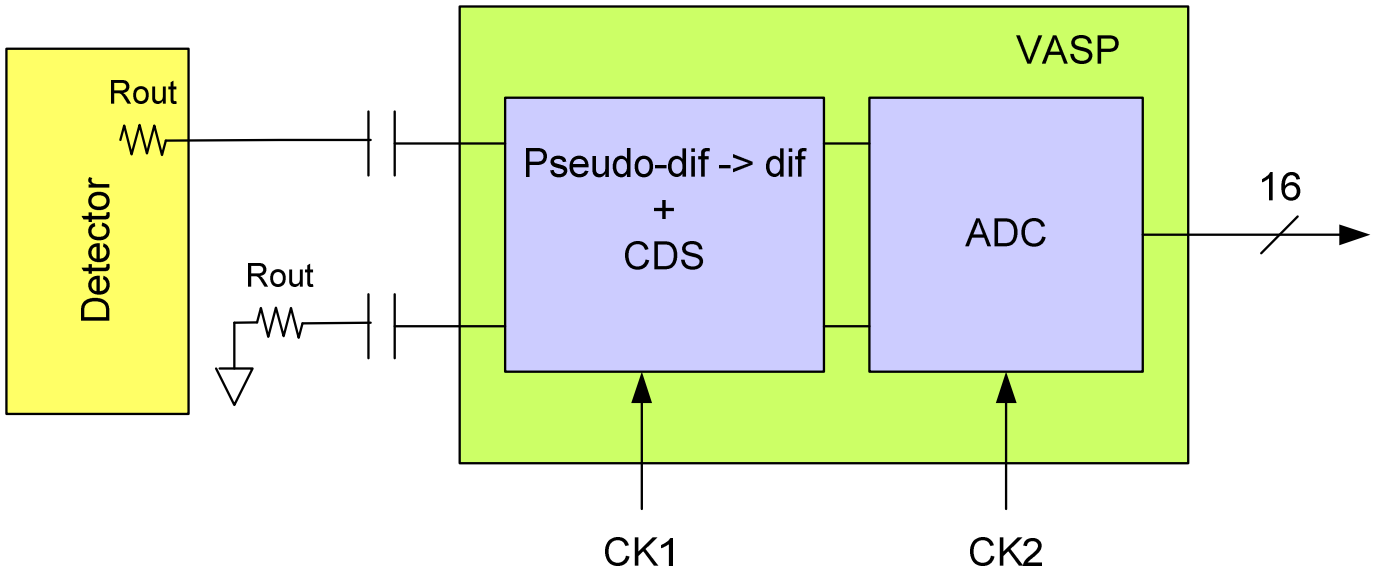
VASP1 application

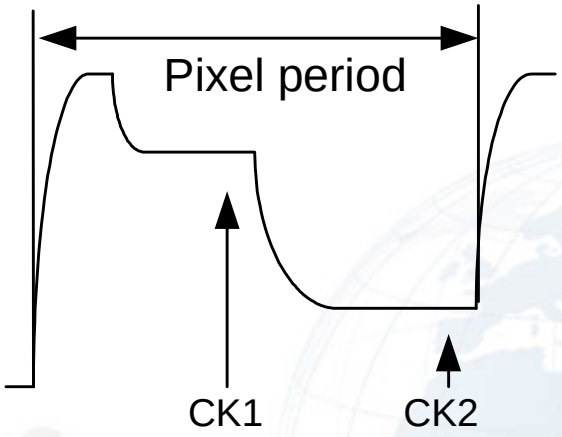
- VASP1 is designed to be used with CCD and CMOS detectors
- VASP is compatible of numerous video processing chain architectures, which depend on :
  - Type of detector, CCD or CMOS
  - Pixel frequency
  - Detector proximity, power and size constraints
- Most usual architectures are shown in the following slides.

CCD – Low pixel frequency – Detector proximity

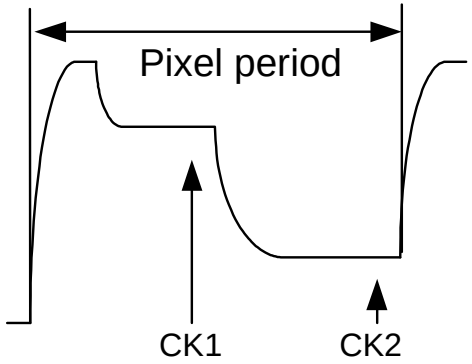


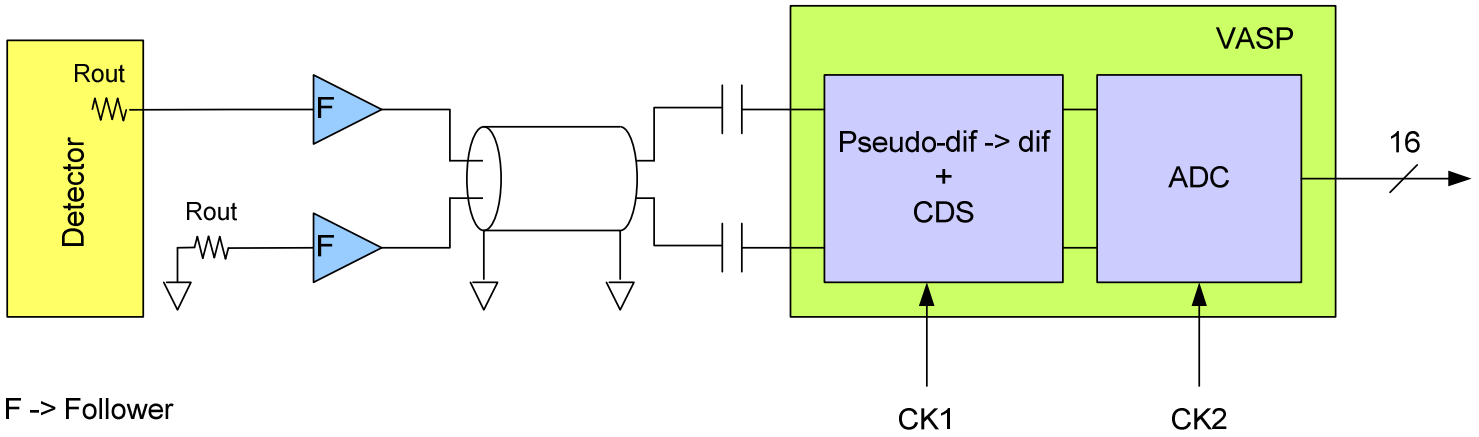
Example of potential applications :

- Sensors

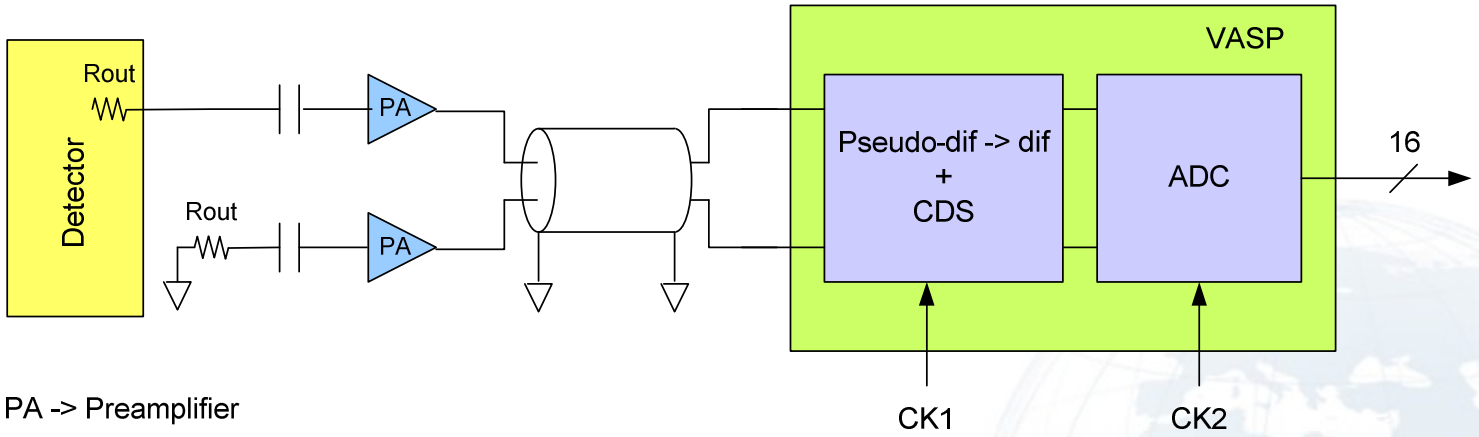


CCD – High pixel frequency – Remote video processing





F -> Follower

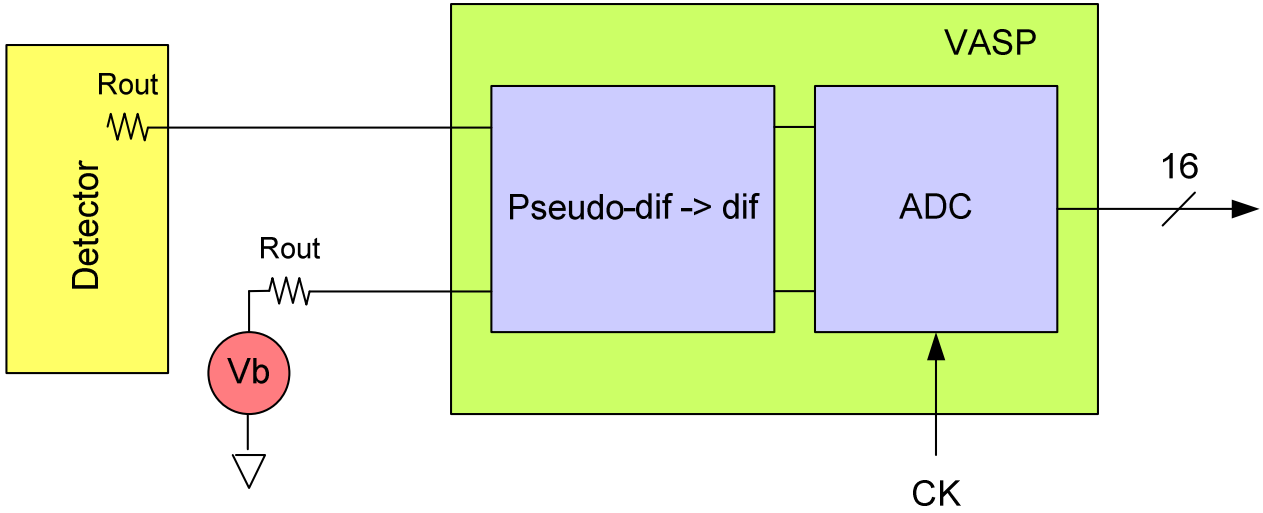


PA -> Preamplifier

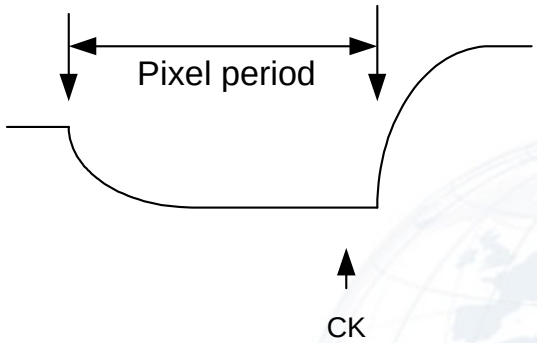
Example of potential applications :

- Earth observation
- Scientific mission

CMOS – Low pixel frequency – Detector proximity



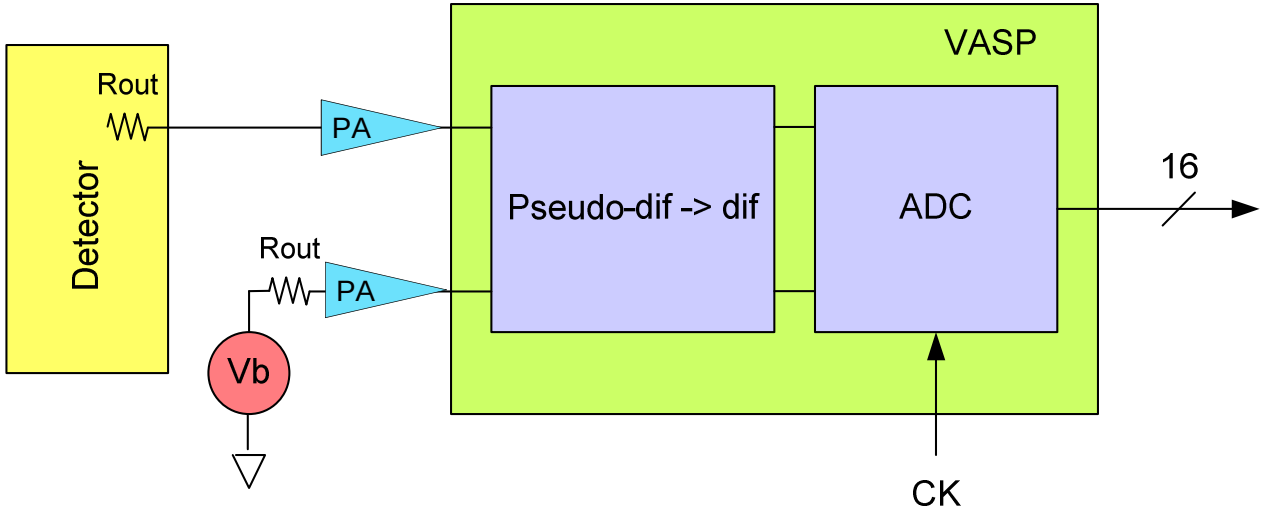
Vb -> Black pixel pedestal



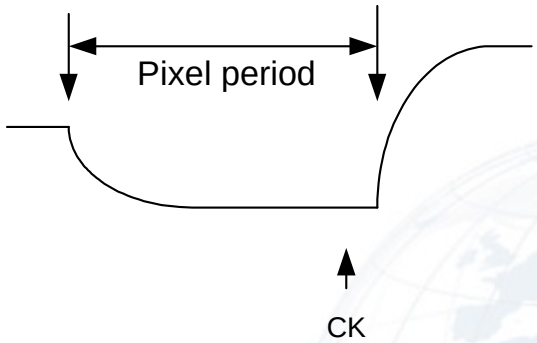
Example of potential applications :

- Sensors

CMOS – High pixel frequency – Detector proximity



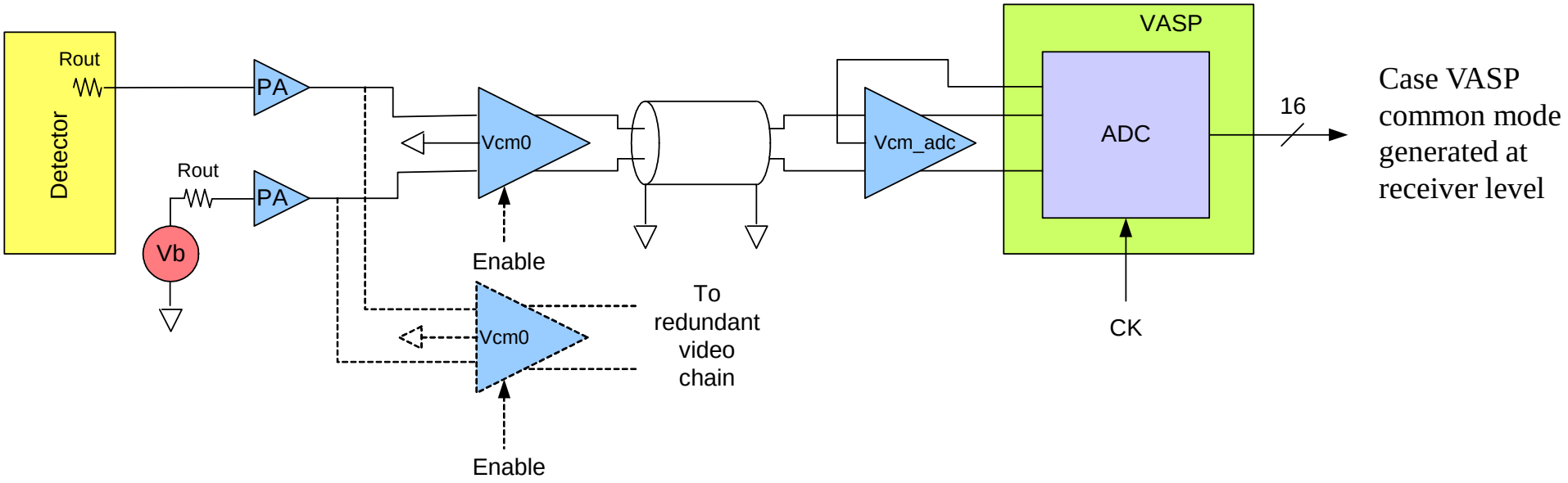
Vb -> Black pixel pedestal



Example of potential applications :

- Sensors

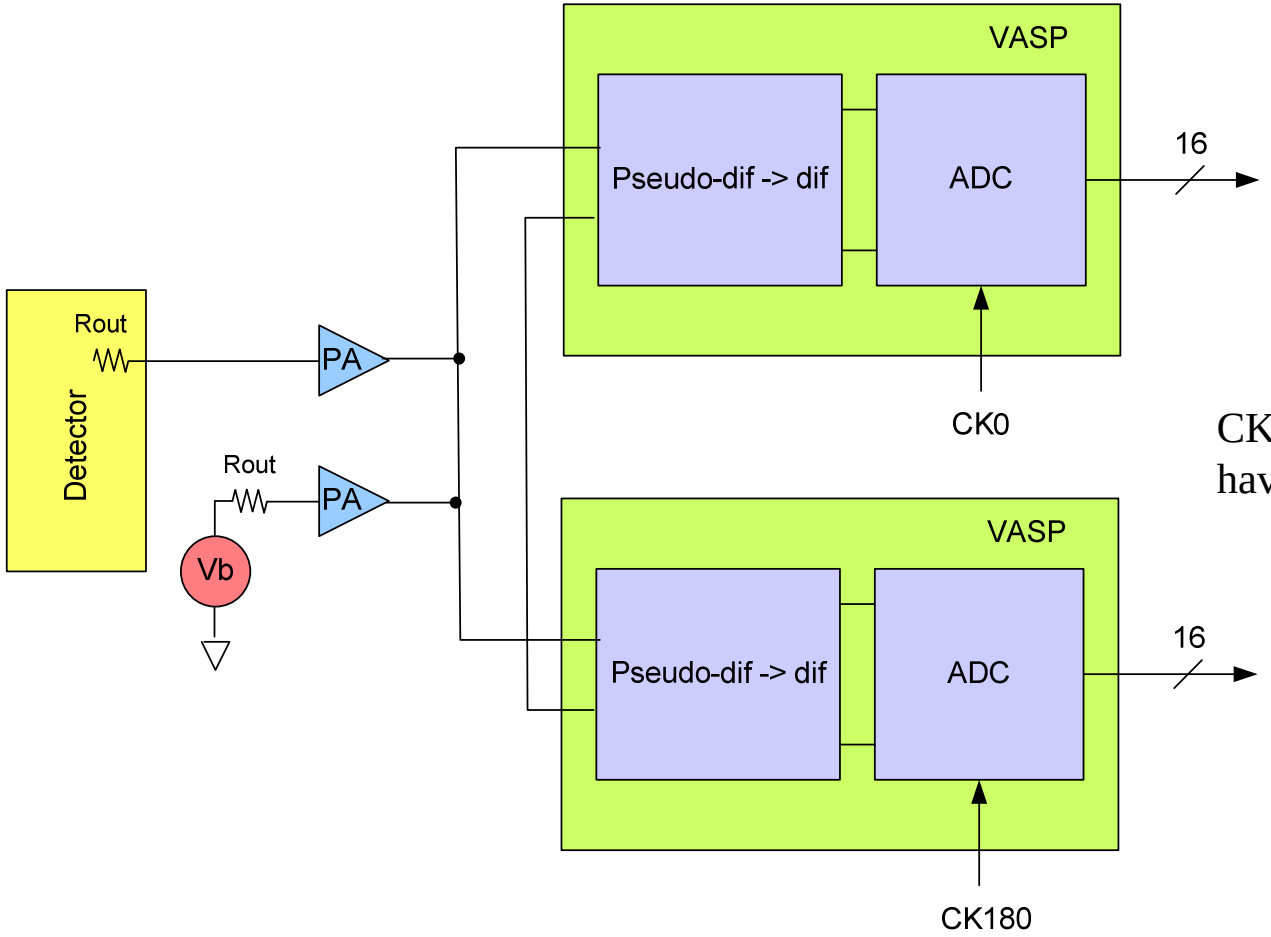
CMOS with redundancy on video processing



Example of potential applications :

- SEN2/MSI
- MTG/FCI
- Most of high performance, high reliability IR imagers

2 VASP1 for increasing sampling frequency up to 8 MHz



CK0 and CK180
have opposite phases

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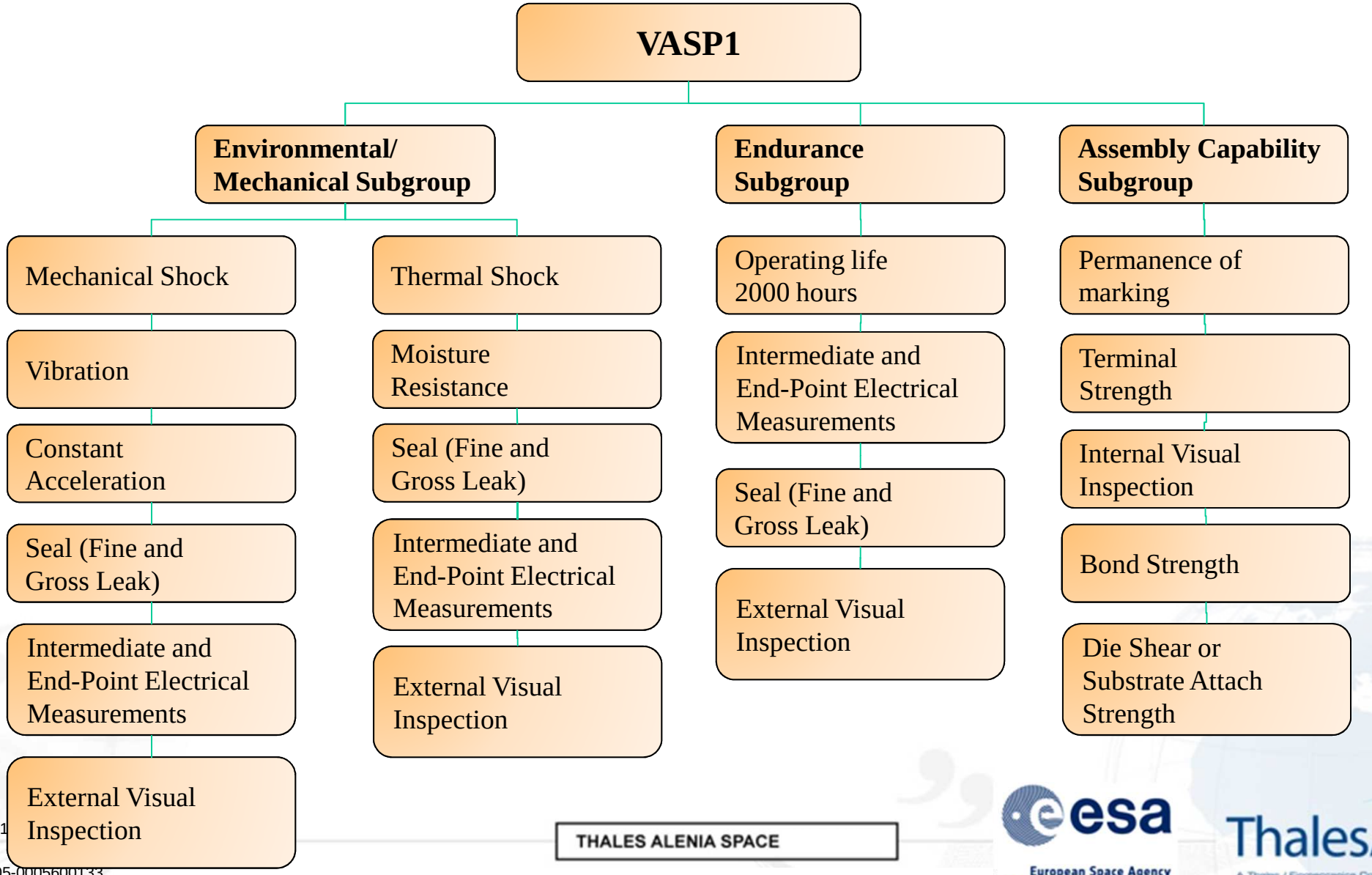
FM qualification

- Consistent with ESCC Generic Specification No. 9000 (chart F4)



Industrial organization for FM qualification and production :

- **Foundry**
  - XFAB
  - ISO 9001:2000/2008
  - Automotive referential : ISO TS 16949:2002/2009
  - Lot PCM
  - Customer alert via automated email

- **Back-end activities**

ESCC Generic Specification No. 9000

  - Partners selected to cover all the activities :
    - Packaging : HCM-Systrel
    - FM production and qualification : SERMA Technologies

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Conclusion

- **Objective of a highly integrated video analog front-end is 100% validated**
  - CDS, clamp and buffers
  - ADC and buffers
  - Internal references

- **Outstanding performances of 16-bit ADC with minimum power consumption**
- **TAS radiation hardening design rules** allow to stand a high level of hardness, for TID and SEE as well.
- **VASP1 Qualification has been performed in full compliance to ECSS-Q-ST-60**
- **FM production of this complex mixed ASIC** for space application is on-going.

VASP1 FM available in Q2 2015

Questions ?

Let’s try VASP1 !