VASP1
DATASHEET

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CHANGE RECORDS

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1.1	2012-03-19	Change the mode names	Lhuillier X.
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2.4	2013-06-28	Typo	Lhuillier X.
2.5	2013-07-02	Typo	Lhuillier X.
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2.9	2014-04-14	Completion of some chapters	Lhuillier X.
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3.1	2014-06-10	Update radiation results and I2C practice Addition of Pixel bus Enable time	Lhuillier X.
3.2	2014-07-04	Reference comments and section 17.3	Lhuillier X.

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1. INTRODUCTION

1.1 Purpose

This document is the datasheet of VASP1 ASIC.

1.2 Abbreviations

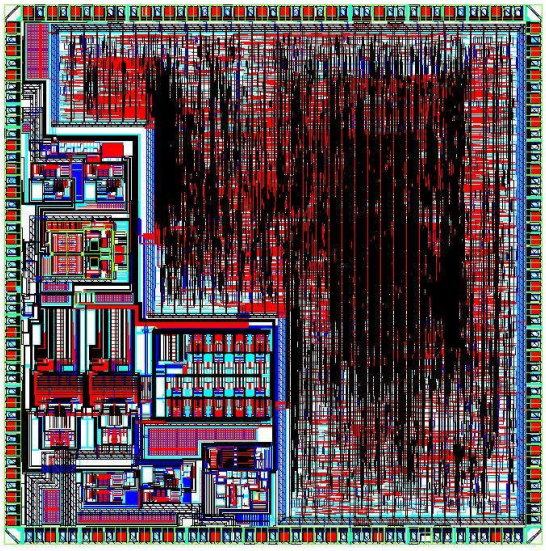
In this paragraph, all the abbreviations used in the document are noted and defined. They could be removed in a future edition of the document after verification that they have been properly integrated into the glossary.

Table 1: abbreviations

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxyde-Silicium technology
COC	Coarse Offset Correction
FOC	Fine Offset Correction
IC	Integrated Circuit
I/O	Input / Output
LSB	Least Significant Bit
MSPS	Mega Sample Per Second
NA	Not Applicable
RMS	Root Mean Square
TBC	To Be Confirmed
TBD	To Be Defined
TID	Total Integrated Dose
VASP	Video Acquisition Signal Processor
VL	Low voltage clock level
VH	High voltage clock level

2. FEATURES

- CCD and CMOS signal processor with 16-bits ADC
- Frequency range from 100kHz to 4MHz
- 4Vpp differential input range
- Differential/Single-ended capability
- 2 Programmable Gains 1V/V and 2V/V
- Multi-sampling per pixel capability
- Clamp signal inputs and clock for DC biasing of video inputs
- Fine and Coarse analog offset inputs
- Internal or external references
- ADC digital calibration of linearity
- ADC Typical INL < 2 LSB and DNL < 0.5 LSB
- 0.8 LSB typical ADC noise
- 0.6V to 2.7V input range
- 3.3 V ± 5% Analog Power Supply Operation
- 3.3 V ±10% Digital Power Supply Operation
- Low Power 0.35µm CMOS technology
- Flexible Power down modes
- I^2C interface up to 1 MHz
- CQFP84 package
- Radiation tolerant up to 101krad
- Latchup free up to 67.7 MeV.cm²/mg^{-1}
- No SEFI up to 67.7 MeV.cm²/mg^{-1}



3. VASP1 PROTOTYPE DESCRIPTION

VASP1 includes a complete analog front-end with A/D conversion for CCD or CMOS signal processing, with a Correlated Double Sampler (CDS) and a 16-bit ADC, both running up to 4 MHz

The 16-bit ADC is based on a fully differential high-speed low-power pipeline core. Its architecture uses 11 multi-bit pipelined stages to achieve low-power dissipation with high sampling rates. It provides a calibration capability to reach high performance linearity.

VASP1 can be configured in two modes : CDS + ADC mode for CDD/CMOS detector types, ADC ONLY mode for CMOS detector types. If the application works with low pixel rates, both modes can be sequenced for multi-sampling per pixel to reduce further the noise.

The reference voltages necessary for the analog blocks are internally generated and decoupled externally. External references can also be used.

Power down mode capability is included for extremely low power dissipation in stand-by mode.

An I2C interface with read/write access is provided to control all the IC functions.

4. APPLICATIONS

The VASP1 is a highly integrated CCD and CMOS signal processor for digital camera applications:

- *Star tracker heads,*
- *smart sensors,*
- *video monitoring cameras,*
- *Optical instruments for science,*
- *Observation and meteorology.*

5. FUNCTIONAL DIAGRAM

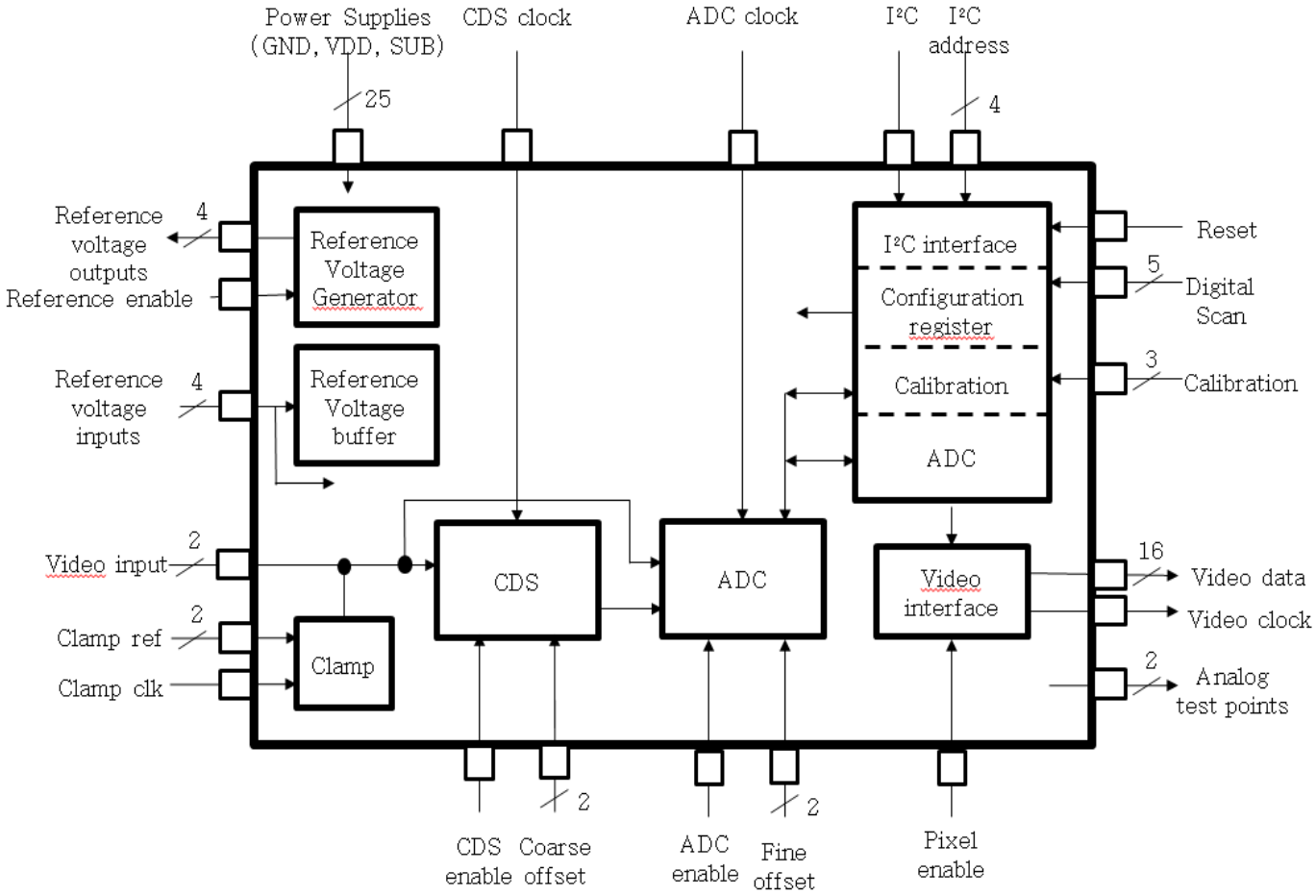


Figure 1: VASP1 functional diagram

6. ABSOLUTE MAXIMUM RATINGS

Table 2: Absolute maximum ratings

Symbol	Parameter	MIN	MAX	Unit
AVDD	Analog Supply voltage	-0.5	+5	V
DVDD	Digital Supply voltage	-0.5	+5	V
Vin	Voltage on any input	-0.5	VDD + 0.5	V
Vout	Voltage on any output	-0.5	VDD + 0.5	V
IpadA	DC current per analog output pad (electro migration)		30	mA
IpadD	DC current per digital output pad (electro migration)		30	mA
Vhbm	Static Discharge (HBM)		1	kV
Tj	Junction temperature	-55	+150	ºC
Ts	Storage Temperature	-55	+150	ºC
Rth	In CQFP 84 on space qualified PCB		20	°C/W
Pd	Device dissipation (Tj=150°C, Tpcb=80°C using Rth max)		700	mW

Stresses above listed parameters under absolute maximum ratings may cause permanent damages to the devices. This is a stress rating only, functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied.

7. RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended operating conditions

Parameter	Conditions	MIN	TYP	MAX	Unit
Power Supplies					
AVDD Analog Supply voltage	3.3 V +/- 0.15	3.15	3.3	3.45	V
VDDIO and DVDD Digital Supply voltage	3.3 V +/- 0.3	3	3.3	3.6	V
Operating conditions					
Temperature at junction	Full functional	-55		+125	ºC
	Full parameters	-30		+80	ºC
Temperature drift range	T0 from –30°C to +50°C	T0		T0+30	ºC
Latch up immunity				67.7	MeV.cm²/mg
Total Ionization Dose				101	krad
LET threshold for SEU		20.4			MeV.cm²/mg
Saturated device Cross Section for SEU	At 67.7 MeV.cm².mg^{-1}		1E-6		cm²
SEFI		SEFI Free up to 67.7 MeV.cm²/mg			

8. PERFORMANCES

Defaut conditions are VDD = 3.3 V, T_A = 30 ºC, ADC Sample rate = 4MHz, internal references, unless otherwise noted.
The typical values are an average value of measurements on samples. The maximum values are estimated from the measurement spread and a specific analysis and/or simulations.

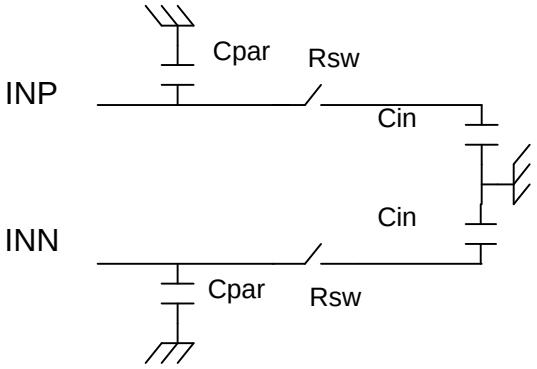
Table 4: Performances

Parameter	Conditions	MIN	TYP	MAX	Unit
Power Supplies					
Current consumption: AVDD + DVDD	CDS+ADC mode @ 4 MHz See note 1		100	115	mA
Power dissipation			330	380	mW
Current consumption: AVDD + DVDD	ADC ONLY mode @ 4 MHZ See note 1		54	60	mA
Power dissipation			180	198	mW
Power down consumption				100	µA
Analog inputs					
Analog input voltage		0.0		AVDD	V
CDS+ADC input impedance	See Note 2				
ADC input impedance	See Note 3				
External biasing current injection	If internal reference current is disabled (ISEL bit) Flowing from AVDD to pin IREF		20		µA
Fine offset voltage	ADC range	-6.25		+6.25	%
	ΔFOC	-500		+500	mV
	focp focn inputs	vcm_in -0.25		vcm_in +0.25	V
Coarse offset voltage	+50% of ADC	0		+32767	LSB
	ΔCOC	0		2	V
	cocp input	vcm_in		vcm_in +1	V
	cocn input	vcm_in –1		vcm_in	V

Note 1 : The consumption is reduced by about 12 mA at 100 kHz.
The consumption is reduced by about 2 mA at – 30°C and increased by about 10 mA at 80°C.

Note 2: The two possible VASP1 input network are given in CDS+ADC mode: CMOS or CCD. The user can used those networks to calculate the system bandwidth based on the RC bandwidth : $f_{-3dB} = 1 / (2.\pi.R_{eq}.C_{eq})$

- Model of CDS+ADC mode input capacitance (SIGNAL = 1 - CMOS)



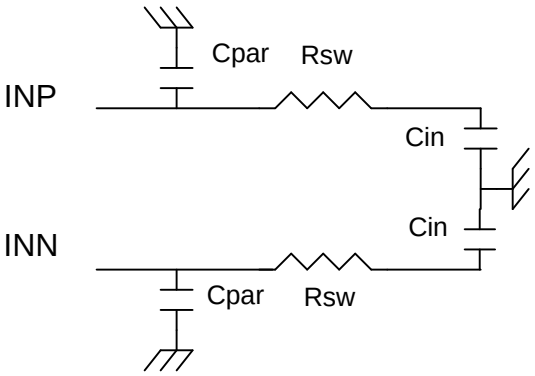
Phase 1 (Rsw is closed)

Cpar = 6 pF ± 1 pF
Rsw = 115 ± 65 Ohms
Cin = 16 pF ± 16%

Phase 2 (Rsw is opened)

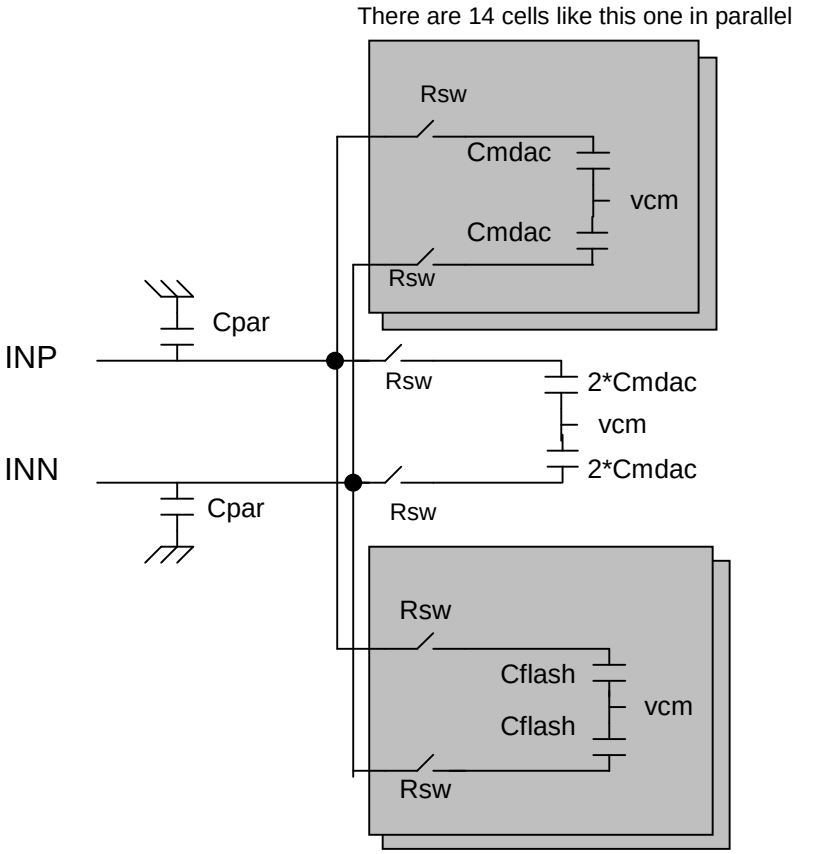
Cpar = 6 pF ± 1 pF

- Model of CDS+ADC mode input capacitance (SIGNAL = 0 - CCD)



Cpar = 6 pF ± 1 pF
Rsw = 115 ± 65 Ohms
Cin = 16 pF ± 16%

Note 3: The VASP1 input network is given in ADC only mode. The user can used this network to calculate the system bandwidth based on the RC bandwidth : $f_{-3dB} = 1 / (2.\pi.R_{eq}.C_{eq})$



Phase 1 (Rsw is closed)

Cpar = 6 pF ± 1 pF
Rsw = 1245 ± 475 Ohms
Cmdac = 1 pF ± 16%
Cflash = 250 fF ± 16%

Phase 2 (Rsw is opened)

Cpar = 6 pF ± 1 pF

Note 4 : all pads (analog/digital) have a parasitic capacitance of 6 pF ± 1 pF to ground.

Table 5: Performances (continued)

Parameter	Conditions	MIN	TYP	MAX	Unit
Digital inputs					
Digital input voltage		0.0		VDDIO	V
Digital logic family			CMOS		
Vil	Input low voltage			0.3 * VDDIO	V
Vih	Input high voltage	0.7 * VDDIO			V
Vth+	Schmitt Trigger pos_threshold		1.6		V
Vth-	Schmitt Trigger neg_threshold		1.2		V
Iih	Input high current Vin=DVDD	-1		1	µA
	Input with pull down Vin=DVDD		30		µA
Iil	Input low current Vin=0V	-1		1	µA
	Input with pull up Vin=0V		-30		µA
Digital input slope	10-90% rise and fall			4	ns
Digital outputs					
Digital output voltage		0.0		VDDIO	V
Digital logic family			CMOS		
Voh	Output high voltage	0.8* VDDIO			V
Vol	Output low voltage			0.4	V
Iol	Output current capability at low level		6		mA
Ioh	Output current capability at high level		6		mA
Output Bus	Pixel Bus Enable Time		15		ns
Digital output slope	10-90% rise on 50pF load		6.3		ns
	10-90% rise on 5pF load		1.6		ns
	10-90% fall on 50pF load		4.5		ns
	10-90% fall on 5pF load		1.4		ns
Output logic coding	Unsigned Binary:	Top Scale: FFFFh Bottom Scale: 0000h			
Digital 3-state					
Ioz	3-State Output Leakage current			1	µA

Table 6: Performances (continued)

Parameter	Conditions	MIN	TYP	MAX	Unit
Differential Input					
Input voltage range		0.6		2.7	V
Differential input range		-2		2	V
Pseudo-Differential Input					
Input voltage range		0.6		2.7	V
Gain					
CDS Gain accuracy	gain 1 or gain 2			0.3	%
ADC gain accuracy	After ΔVref and internal VBG trim	-0.3		0.3	%
ADC Gain drift for a temp range 0ºC to 30ºC	Based on the use of the internal and trimmed VBG (see note 5)			10	ppm/°C
Internal Voltage references					
Reference voltage	ΔVref = VREFP-VREFN After trim (see note 6)	1.994	2	2.005	V
Common mode voltage	VCM after trim (see note 6)		1.65		V
Bandgap voltage	VBG after trim (see note 6)		1.25		V
Common mode voltage programming step			12		mV
Common mode voltage programming range		-100		+100	mV
Bandgap temperature slope	Programmable	-450		450	ppm/°C
Reference voltage variation for a temp range 0ºC to 30ºC	After trim (see note 5)			10	ppm/°C
Static PSRR		60			dB
Output internal serial resistor	For vbg_out, vrefp_out, vrefn_out, vcm_out pins	4.3	5	5.7	kOhms
External Voltage References					
Reference voltage input	VREF = *vrefp_in - vrefn_in*		2		V
Bandgap voltage input	*vbg_in*	1.23	1.25	1.27	V
Common mode voltage input	*vcm_in*		1.65		V
Biasing					
Iref output biasing current	Flowing from AVDD to pin		20		µA

Note 5 : The temperature dependency of the internal VBG voltage is trimmed via VREFBG register. For the optimal temperature stability, the absolute value of the internal VBG might lead to a ΔVref slightly below 2 V.
Note 6 : The different reference trim (VREFBG, VREFCM, VREFREF) should be used to find these absolute value. Note that the temperature stability might not be reached for these absolute value. See chapter 17.3

Table 7: Performances (continued)

Parameter	Conditions		MIN	TYP	MAX	Unit
Video chain						
Number of bits				16		bit
Output data latency	CDS+ADC mode			8.5		adcclk cycles
	ADC ONLY mode			8		
Pixel rate			0.1		4	MHz
ADC sample rate	Multiple of pixel rate		0.1		4	MS/s
ADC differential input range			-2		+2	V
ADC LSB	$2*\Delta Vref / 2^{16}$			61		µV
OFFSET (After ADC calibration)	All modes			1	12	mV
				15	200	LSB
Input Common Mode Rejection	CMOS signal			50		dB
	CCD signal			70		dB
CCD synchronous noise rejection	CDS+ADC mode 0.1MHz			91		dB
	CDS+ADC mode 4MHz			80		dB
Linearity in CDS+ADC mode after calibration (worst case of CCD and CMOS signals)						
DNL	@ 4 MHz	peak		0.9	<1	LSB
INL measured (note 7)	@ 4 MHz	peak		10		LSB
INL estimated	@ 4 MHz	peak		5	<10	LSB
Linearity in ADC ONLY mode after calibration						
DNL	@ 4 MHz	peak		0.5	0.7	LSB
INL measured (note 7)	@ 4 MHz	peak		4		LSB
INL estimated	@ 4 MHz	peak		2	3	LSB

Note 7 : INL performance measurement is limited by the test bench linearity. Test bench contribution to INL results is estimated to 50%.

Table 8: Performances (continued)

Parameter	Conditions	MIN	TYP	MAX	Unit
Noise with CMOS signal in CDS+ADC mode – Note 8					
RMS referred input Noise	@ 4 MHz		1.9	2.3	LSB
	@ 3 MHz		1.8	2.1	LSB
	@ 100 kHz		1.6	2	LSB
Noise with CCD signal in CDS+ADC mode – Note 8					
RMS referred input Noise	@ 4 MHz		1.9	2.6	LSB
	@ 3 MHz		1.7	2.4	LSB
	@ 100 kHz		1.5	2.2	LSB
Noise in ADC ONLY mode					
RMS referred input Noise	@ 4 MHz, 3 MHz and 100 kHz		0.8	0.9	LSB
SNR	Note 9	88.2	89.2		dB
ENOB	Note 10	14.4	14.5		bits
Noise coupling – Note 11					
I²C peak coupling	CDS+ADC mode		25		LSB
I²C coupling ΔRMS noise			+0.5		LSB
I²C coupling RMS noise			1.6		LSB
I²C peak coupling	ADC ONLY mode		25		LSB
I²C coupling ΔRMS noise			+0.1		LSB
I²C coupling RMS noise			0.4		LSB

Note 8 : The noise measurement is static. The values are the RMS value of sample codes when a static input signal is provided.

Note 9 :SNR is calculated using :

$$SNR = 20 \times \log\left(\frac{\frac{2 \times \Delta Vref}{2\sqrt{2}}}{RMSreferredinputNoise}\right)$$

Note 10 : ENOB is calculated using :

$$ENOB = \frac{SNR - 1.76}{6.02}$$

Note 11 : I2C noise coupling figures are given for information. However, a good practice is to avoid I2C activity during useful pixel processing (see p.22).

Table 9 : Performances (continued)

Parameter	Conditions	MIN	TYP	MAX	Unit
Timing characteristics					
Pixel Rate		0.1		4	MHz
ADC Sample Rate	ADC clock = sampling rate	0.1		4	MS/s
ADC Clock duty cycle		48	50	52	%
Power up time	after settling of internal voltage references			100	ms
Pixelclk rise time (tr1)	load capacitance 5 pF	0.4	0.8	2	ns
Pixelclk fall time (tf1)	load capacitance 5 pF	0.4	0.8	2	ns
adcclk Falling edge to sampling delay (tsd)		10	13	16	ns
adcclk Rising edge to valid data output (tod)		15	21	27	ns
adcclk to pixel edge Delay (tclkd)		12	18	24	ns
Delay between fcdsclk and end of CCD reference level (tckref)		2.0			ns
Delay between ADC clock rising edge and CDS clock falling edge			25		ns
Video Interface					
Delay between ena_pixel rising and effective pixel bus drive	t_{make} Pixel bus is the 16 pixel lines plus the pixel clock	6		13	ns
Delay between ena_pixel falling and effective pixel bus release	t_{break} Pixel bus is the 16 pixel lines plus the pixel clock	2		4	ns
Break-before-make non overlap	t_{make} - t_{break}	2			ns
I²C Interface					
Data Rate			0.4	1	Mbps
I²C slave address range		00h		0Fh	

9. PIN LIST

Table 10 : VASP1 pin list

Side	Pin	Pin Name	I/O/S	State during and after reset	Analog / Digital	Internal Pull-up (UP) Pull-down (DN)	Description
LEFT	33	outn_test	O	Hi-Z	A	-	Test negative output
	34	outp_test	O	Hi-Z	A	-	Test positive output
	35	FE_vdda_ref	S	-	FE VDD REF	-	Front-End 3.3V analog supply + Analog ESD rail
	36	FE_gnda_ref	S	-	FE GND REF	-	Ground for front-end references
	37	ena_cds	I	-	D	DN	CDS enable
	38	iref	I	-	A	-	ADC current reference input (optional)
	39	cocp	I	-	A	-	CDS offset correction positive signal
	40	cocn	I	-	A	-	CDS offset correction negative signal
	41	clampp	I	-	A	-	Clamp positive signal
	42	clampn	I	-	A	-	Clamp negative signal
	43	vdda	S	-	VDDA CORE	-	Front-End 3.3V analog supply + Analog ESD rail
	44	gnda_cds	S	-	GND CDS	-	Ground for CDS
	45	inp	I	-	A	-	Signal positive input from detector
	46	inn	I	-	A	-	Signal negative input from detector
	47	gnd	S	-	GND SUB	-	Substrate GND + Digital ESD rail
	48	focp	I	-	A	-	ADC Offset compensation positive signal
	49	focn	I	-	A	-	ADC offset compensation negative signal
	50	vrefn_in	I	-	A	-	Input for negative reference voltage
	51	vrefp_in	I	-	A	-	Input for positive reference voltage
	52	vcm_in	I	-	A	-	Input for common mode voltage
	53	vbg_in	I	-	A	-	Band-gap voltage reference input
BOTTOM	54	vdda_adc	S	-	VDD ADC	-	ADC 3.3V analog supply
	55	gnda_adc	S	-	GND ADC	-	Ground for ADC
	56	vrefn_out	O	Hi-Z	A	-	Output of negative reference voltage
	57	vrefp_out	O	90 kOhms to gnd	A	-	Output of positive reference voltage
	58	vcm_out	O	30 kOhms to gnd	A	-	Output of common mode reference voltage
	59	vbg_out	O	Hi-Z	A	-	Output of band-gap reference voltage
	60	gndr_ref	S	-	GND REF	-	Clean gnd for references
	61	ADC_gnda_ref	S	-	ADC GND REF	-	Ground for ADC reference
	62	ADC_vdda_ref	S	-	ADC VDD REF	-	Analog supply for ADC reference
	63	ena_adc	I	-	D	UP	Enable of the ADC
	64	adcclk	I	-	D	DN	ADC clock
	65	enacalib	I	-	D	DN	Enable ADC calibration sequence
	66	startcalib	I	-	D	-	Start ADC calibration sequence
	67	endcalib	O	0	D	-	ADC Calibration end signal
	68	vddd	S	-	VDD DIG	-	Digital 3.3V supply
	69	gndd	S	-	GND DIG	-	Digital ground
	70	ena_pixel	I	-	D	UP	Enable the pixel bus
	71	gndio	S	-	IO GND	-	IO buffer ground

	72	pixelclk	O	0	D	-	Pixel bus clock
	73	vddio	S	-	IO VDD	-	IO buffer 3.3V supply
	74	gndio	S	-	IO GND	-	IO buffer ground
	75	vddio	S	-	IO VDD	-	IO buffer 3.3V supply
	76	pixel<0>	O	0	D	-	Pixel bus net 0 - LSB
	77	pixel<1>	O	0	D	-	Pixel bus net 1
	78	pixel<2>	O	0	D	-	Pixel bus net 2
	79	pixel<3>	O	0	D	-	Pixel bus net 3
	80	pixel<4>	O	0	D	-	Pixel bus net 4
	81	gndio	S	-	IO GND	-	IO buffer ground
	82	vddio	S	-	IO VDD	-	IO buffer 3.3V supply
	83	pixel<5>	O	0	D	-	Pixel bus net 5
	84	pixel<6>	O	0	D	-	Pixel bus net 6
RIGHT	1	pixel<7>	O	0	D	-	Pixel bus net 7
	2	pixel<8>	O	0	D	-	Pixel bus net 8
	3	pixel<9>	O	0	D	-	Pixel bus net 9
	4	pixel<10>	O	0	D	-	Pixel bus net 10
	5	gndio	S	-	IO GND	-	IO buffer ground
	6	vddio	S	-	IO VDD	-	IO buffer 3.3V supply
	7	pixel<11>	O	0	D	-	Pixel bus net 11
	8	pixel<12>	O	0	D	-	Pixel bus net 12
	9	pixel<13>	O	0	D	-	Pixel bus net 13
	10	pixel<14>	O	0	D	-	Pixel bus net 14
	11	pixel<15>	O	0	D	-	Pixel bus net 15 - MSB
	12	gndio	S	-	IO GND	-	IO buffer ground
	13	vddio	S	-	IO VDD	-	IO buffer 3.3V supply
	14	scl	I	-	D	-	I2C clock
	15	sda	I/O	Hi-Z	D	-	I2C data
	16	rstz	I	-	D	UP	General reset (active low)
	17	gndd	S	-	GND DIG	-	Digital ground
	18	vddd	S	-	VDD DIG	-	Digital 3.3V supply
	19	I2C<3>	I	-	D	-	I2C address bit 3 – MSB
	20	I2C<2>	I	-	D	-	I2C address bit 2
	21	I2C<1>	I	-	D	-	I2C address 1
TOP	22	I2C<0>	I	-	D	-	I2C address bit 0 - LSB
	23	scanrstz	I	-	D	-	Scan reset (active low)
	24	scanmode	I	-	D	DN	Scan mode
	25	scanin	I	-	D	-	Scan input
	26	scanclk	I	-	D	-	Scan clock
	27	scanen	I	-	D	-	Scan enable
	28	scanout	O	0	D	-	Scan output
	29	gnd	S	-	GND SUB	-	Substrate GND + Digital ESD rail
	30	ena_vref	I	-	D	UP	Voltage reference enable
	31	fcdsclk	I	-	D	DN	Input for CDS clock
	32	clampclk	I	-	D	DN	Input for clamp clock

10. PACKAGING

The package is a CQFP 84 from Kyocera (Ref : PB-44795).

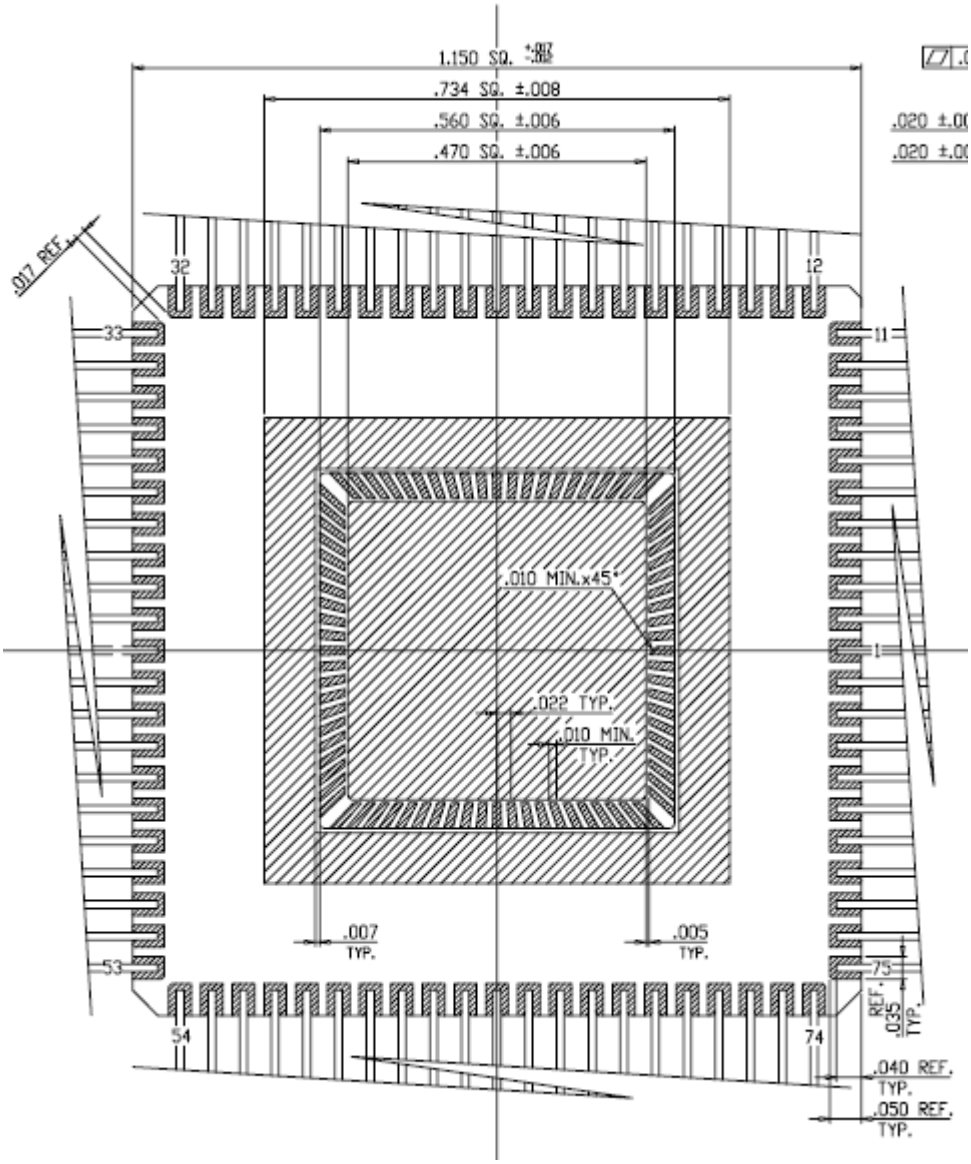


Figure 2 : Package top view

11. VASP1 FUNCTIONAL MODE

The VASP1 IC can be in 4 different modes.

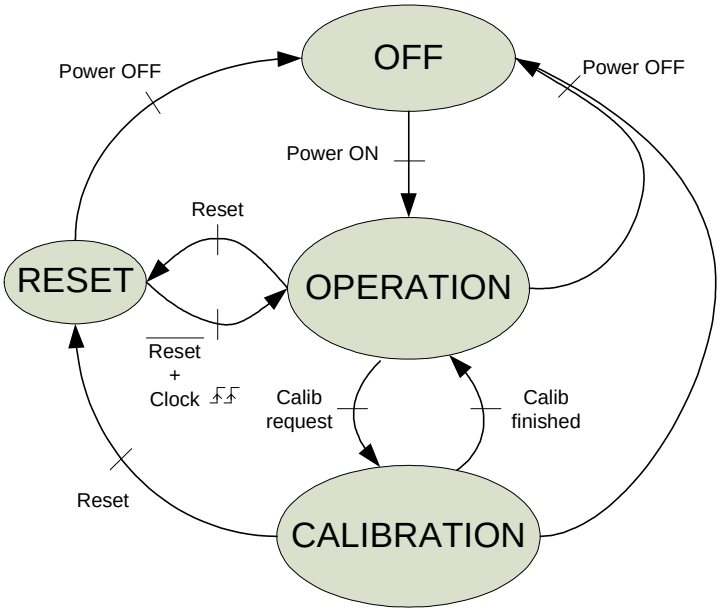


Figure 3 : VASP1 modes

- OFF
  In this mode, there is no power to supply the VASP1. The circuit is not functional.
- OPERATION
  In this mode, the VASP1 performs the signal processing depending on the block selected via the enable pins.
- RESET
  This mode is entered when RSTZ pin is low. There is no activity in this mode where all the digital gates are set in there default state.
- CALIBRATION
  This mode allows the self-calibration of the ADC linearity.

There are 4 independent enable lines that lead to the following configuration :

- ENA_ADC. This line is mandatory to start the digital and have the ADC working.
- ENA_CDS. This line turns on the CDS block and its output are used by the ADC (named CDS+ADC configuration). When off, the ADC is directly using the IC video inputs INP and INN (also named ADC only configuration)
- ENA_PIXEL. This line controls the video interface. At logic level one, the pixel bus is driven by the digital output. When off, the output pixel bus is not driven by the digital output and goes to high impedance state.
- ENA_VREF. This line turns on the internal voltage reference blocks.

The I2C configuration registers can be accessed at any time during operation mode. However, a good practice is to avoid such configuration change during a useful conversion of pixel because the digital activity would induce noise on the output code.

12. OPERATION MODE

12.1 Video processing

The VASP1 is a video signal processor. There are typically two types of input signal : CCD or CMOS signal and those signals can be either differential or pseudo-differential.

12.1.1 CCD differential

The CCD differential signal is described by the following figure.

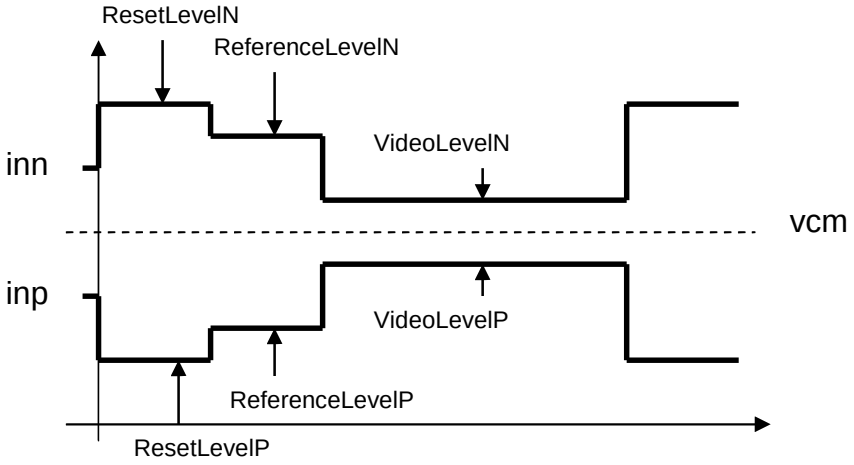


Figure 4 : CCD differential signal

When such input signal is used, the following equation applies:

VutileP = ReferenceLevelP - VideoLevelP
VutileN = ReferenceLevelN - VideoLevelN

Vutile = VutileP – VutileN

Note : For pixel rate lower than 2 MHz, there is a possibility to disable the CDS (ENA_CDS = 0) and measures the reference and the video levels by a proper ADC clock sequencing similar to a CMOS signal. Then, the extraction of the utile signal can be done in digital domain outside the VASP1. This configuration is detailed in following section.

The CDS is used with the SIGNAL bit set to zero. The CDS takes two correlated samples and makes the subtraction. Then the ADC converts the utile signal.

The output signal is

$$pixel<15:0>=\left\{\Delta COC-(CDS\_gain*Vutile)+\frac{\Delta Foc}{4}\right\}\times\frac{2^{16}}{2\times\Delta Vref}$$

If there is no video signal (VideoLevelP equals ReferenceLevelP and VideoLevelN equals ReferenceLevelN), then the Vutile is 0 V. On the other hand, the maximum video signal would be with a VutileP = -2V and VutileN = 2V, and thus the Vutile = -4V. In this case, the ΔCOC voltage needs to be -2V to shift without offset the Vutile into the ADC input range {-2 ;+2V}.

Note that the COCP (and COCN respectively) will always receive the high value voltage around 2.65 V (respectively low value voltage around 0.65V). To perform the negative sign, the COCINV register bit is set to zero.

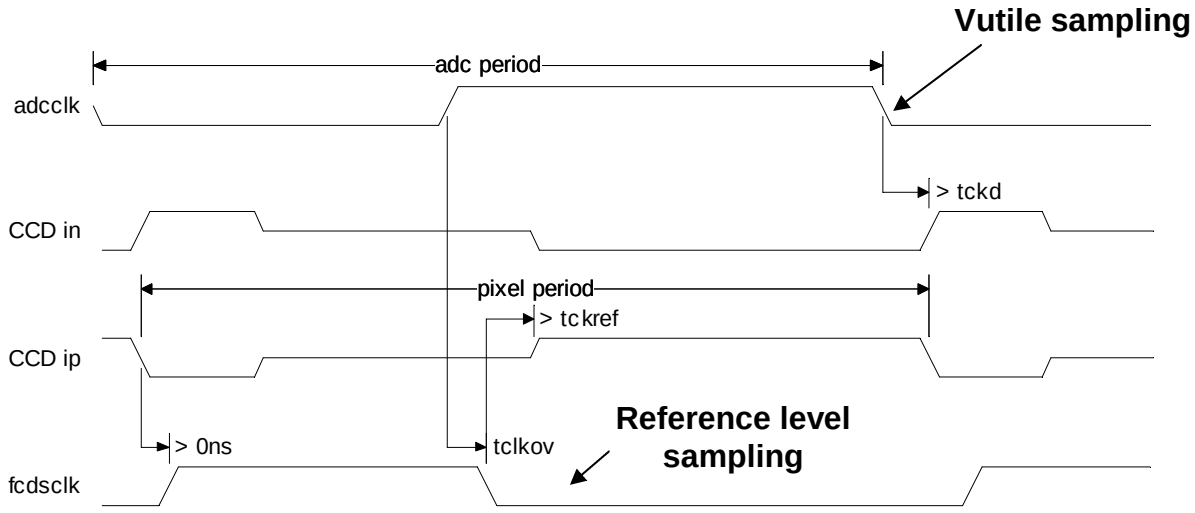


Figure 5 : Sequencing CCD signal

The clock have a duty-cycle of 50%. The FCDSCLK rising edge position is not critical and shall be placed after pixel start.

The latency between signal input and digital output is 8.5 ADC clock period. See chapter 13.

12.1.2 CCD pseudo-differential

The CCD pseudo-differential signal is described by the following figure.

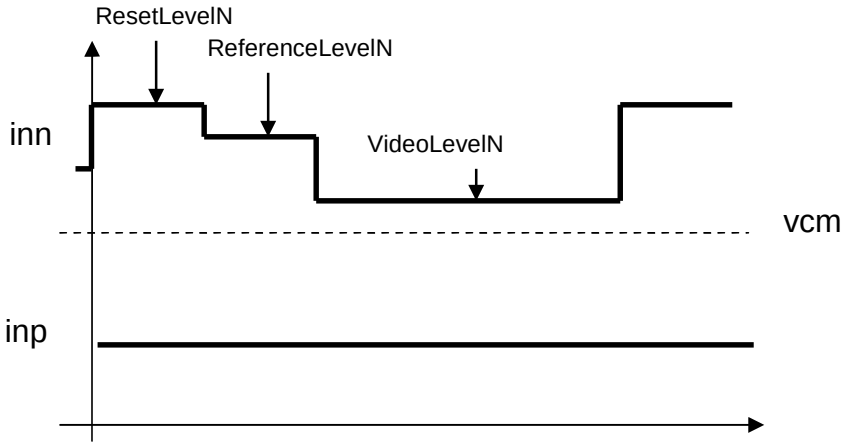


Figure 6 : Pseudo_differential CDD signal

When such input signal is used, the following equation applies:

VutileP = ReferenceLevelP – VideoLevelP = 0
VutileN = ReferenceLevelN - VideoLevelN

Vutile = VutileP – VutileN = – VutileN

The CDS is used with the SIGNAL bit is set to zero. The CDS takes two correlated samples and makes the subtraction. Then the ADC converts the utile signal.

The output signal is

$$pixel<15:0>=\left\{\Delta COC-(CDS\_gain*Vutile)+\frac{\Delta Foc}{4}\right\}\times\frac{2^{16}}{2\times\Delta Vref}$$

If there is no video signal (VideoLevelN equals ReferenceLevelN), then the Vutile is 0 V. On the other hand, the maximum video signal would be maximum with a VutileN = 2V, and thus the Vutile = -2V. The CDSGAIN (by default at 1 for a gain of 1) can be set to zero for a gain of 2, leading to the same output range than the differential case and thus optimizing the signal for the ADC input range. In this case, the ΔCOC voltage needs to be -2V to shift without offset the Vutile into the ADC input range {-2 ;+2V}.

Note that the COCP (and COCN respectively) will always receive the high value voltage around 2.65 V (respectively low value voltage around 0.65V). To perform the negative sign, the COCINV register bit is set to zero.

The same sequencing applies for the CDS and ADC clock as the differential CCD. The latency between signal input and digital output is 8.5 ADC clock period. See chapter 13.

12.1.3 CMOS differential

The CCD pseudo-differential signal is described by the following figure. Note that the VideoLevelP corresponding to inp input is above VideoLevelN corresponding to inn (inverted compared to CCD case).

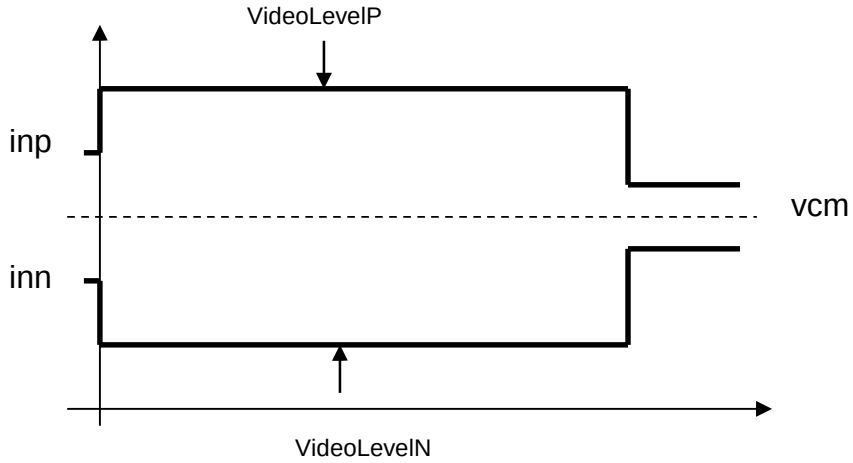


Figure 7 : Differential CMOS signal

When such input signal is used with CDS, the following equation applies:

Vutile = VideoLevelP – VideoLevelN

This signal can be processed directly by the ADC for minimal noise and power consumption, or goes through the CDS to benefit of the coarse offset inputs.

12.1.3.1 CMOS differential with CDS

The CDS is used with the SIGNAL bit is set to one. The CDS samples once the VrefP and VrefN as a pseudo reference level and then input signal. Then the ADC converts the utile signal.

The output signal is

$$pixel<15:0>=\left\{\text{CDS\_gain}*(\text{Vutile}-\Delta Vref)+\Delta COC+\frac{\Delta\text{Foc}}{4}\right\}\times\frac{2^{16}}{2\times\Delta Vref}$$

If there is no video signal (VideoLevelP equals VrefN and VideoLevelN equals VrefP), the Vutile is -2 V. On the other hand, if there is a maximum video signal (VideoLevelP equals VrefP and VideoLevelN equals VrefN), the Vutile = 2V. As the ΔVREF shifts down the dynamic range, the ΔCOC voltage needs to be 2V to shift back without offset into the ADC input range {-2 ;+2V}.

Note that the COCP (and COCN respectively) will always receive the high value voltage around 2.65 V (respectively low value voltage around 0.65V). To maintain the positive sign, the COCINV register bit is set to one.

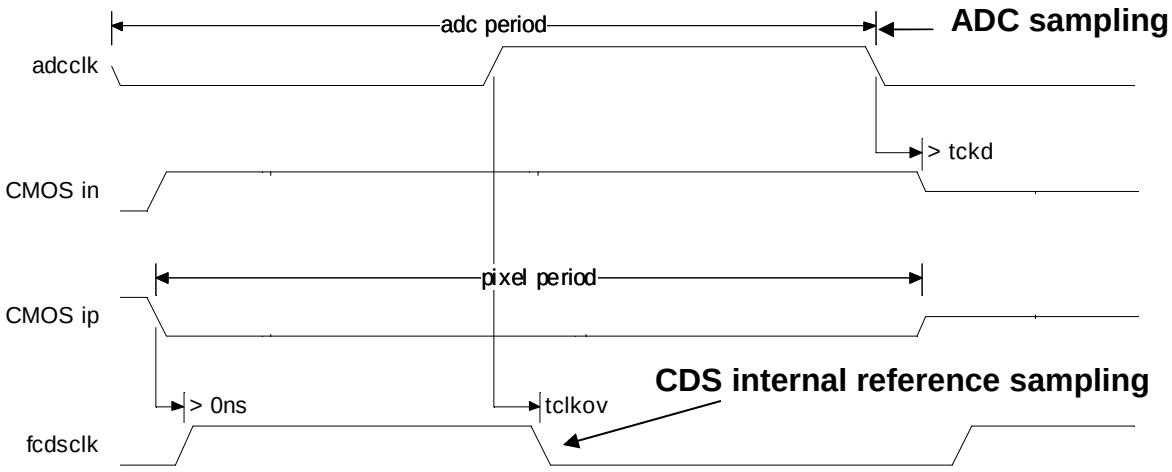


Figure 8 : Sequencing CMOS signal with CDS and ADC

The FCDSCLK rising edge position is not critical and shall be placed after pixel start.

The latency between signal input and digital output is 8.5 ADC clock period. See chapter 13.

12.1.3.2 CMOS differential with ADC only

The CDS is disabled.
The output signal is

$$pixel<15:0>=\left\{\text{Vutile}+\frac{\Delta\text{Foc}}{4}\right\}\times\frac{2^{16}}{2\times\Delta Vref}$$

If there is no video signal (VideoLevelP equals VrefN and VideoLevelN equals VrefP), the Vutile is -2 V. On the other hand, if there is a maximum video signal (VideoLevelP equals VrefP and VideoLevelN equals VrefN), the Vutile = 2V. The signal is thus in the optimum ADC dynamic range.

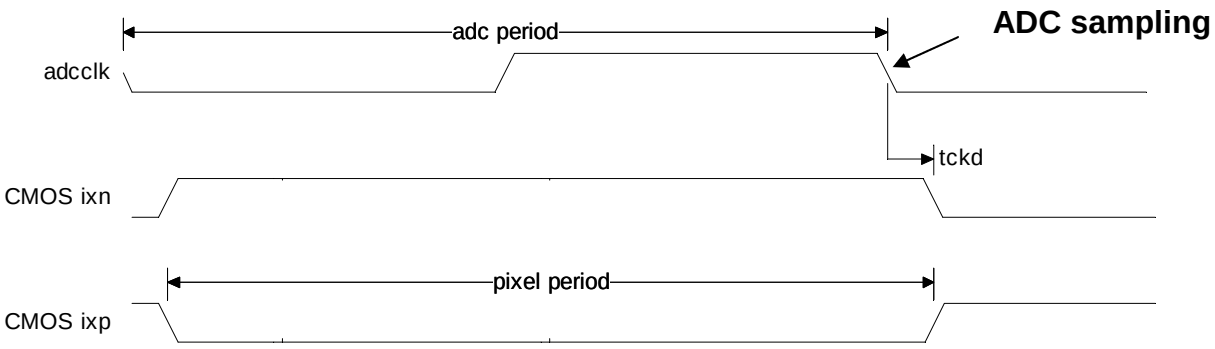


Figure 9 : Sequencing CMOS signal, ADC ONLY mode mono-sampling

The latency between signal input and digital output is 7.5 ADC clock period. See chapter 13.

12.1.4 Pseudo-differential CMOS signals

The CMOS pseudo-differential signal is described by the following figure. Note that the VideoLevelP corresponding to inp input is above VideoLevelN corresponding to inn (inverted compared to CCD case).

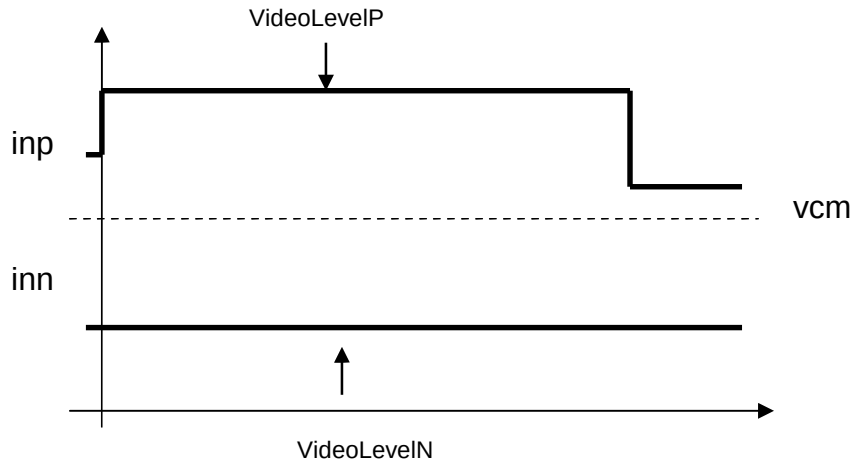


Figure 10 Pseudo-differential CMOS signal

When such input signal is used with CDS, the following equation applies:

$$Vutile = VideoLevelP - VideoLevelN$$

The CDS is used with the SIGNAL bit is set to one to create a differential signal for the ADC. The CDS samples once the VrefP and VrefN as a pseudo reference level and then input signal. Then the ADC converts the utile signal.

The output signal is

$$pixel<15:0>=\left\{\text{CDS\_gain}*(\text{Vutile}-\Delta Vref)+\Delta COC+\frac{\Delta\text{Foc}}{4}\right\}\times\frac{2^{16}}{2\times\Delta Vref}$$

If there is no video signal (VideoLevelP equals VideoLevelN), the Vutile is 0 V. On the other hand, if there is a maximum video signal (VideoLevelP equals VideoLevelN + 2V), the Vutile = 2V. The CDSGAIN bit can be set to 0 so as to get a CDS_Gain of 2 to maximize the signal to the ADC dynamic range. As the ΔVREF shifts down the dynamic range, the ΔCOC voltage needs to be 2V to shift back without offset into the ADC input range {-2 ;+2V}.

Note that the COCP (and COCN respectively) will always receive the high value voltage around 2.65 V (respectively low value voltage around 0.65V). To maintain the positive sign, the COCINV register bit is set to one.

The sequencing is identical to CMOS differential signal. The latency between signal input and digital output is 8.5 ADC clock period. See chapter 13.

12.2 ADC output

The ADC is working between –2V and 2V differential, giving a full range of 4V. The common mode is 1.65V, which leads to maximum 2.65 V on one side and minimum 0.65 V on the other. The ADC output is unsigned and the following codes are theoretically found on the pixel bus.

Table 11 Output code versus input signal on the ADC

Input signal (inp-inn)	Output code
-2V	0
0V	32767
2V	65535

The sampling rate of the ADC is defined by the frequency of the *adcclk* signal. The input signal is sampled on the falling edge of the *adcclk*, and the results are latched on the rising edge of *adcclk* in the output register 7.5 *adcclk* period later (8.5 period when the CDS is enabled). If the reading of the pixel bus is made on the falling edge of *pixelclk* then a latency of 8 *adcclk* periods is observed (9 periods if the CDS is enabled). The conversion timing is shown in next figure :

VideoLevelP inp

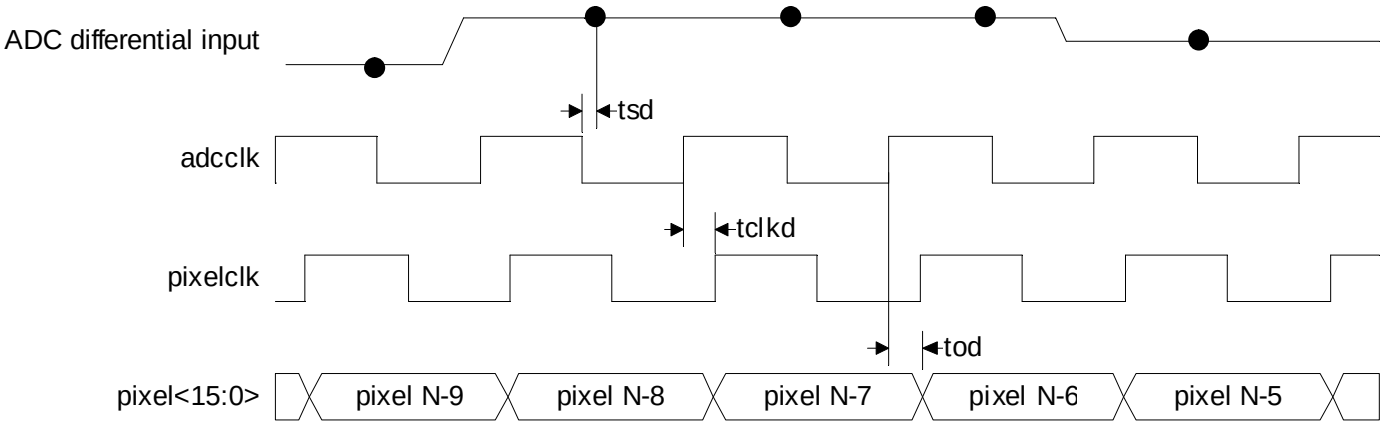


Figure 11 : ADC output sequencing

Note that the real sampling time is shifted from the adcclk falling edge by roughly 13 ns. This delay is based on the reference current. If using an external reference, this delay behavior over temperature will be linked to the VBG_IN variation.

12.3 Video interface

A ena_pixel pin can be used to enable/disable the pixel bus (*pixel<15:0>* and *pixelclk* outputs). When disable (ena_pixel = 0), the pixel bus is in high impedance state. When enable (ena_pixel = 1), the pixel bus is driven by the ADC output word.
A break-before-make technic is used on the pixel bus. It means that the time to release the pixel bus to high impedance state is always faster than the time to start to drive it. The non-overlap delay (t_{make} - t_{break}) is about 2-3 ns.

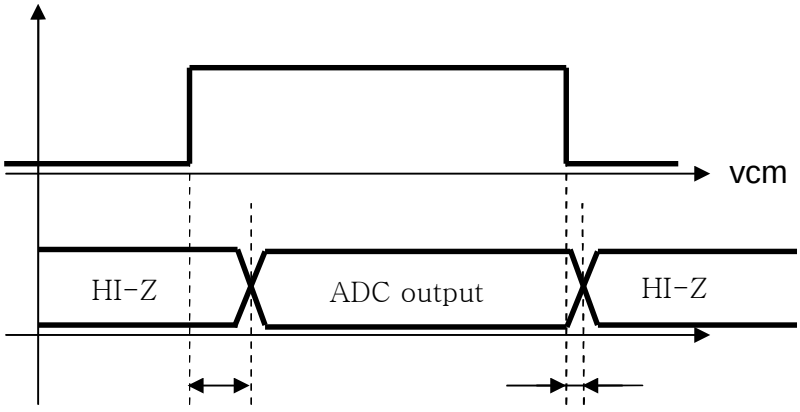


Figure 12 : Break-before-make on pixel bus enable

12.4 Multi-sampling

If the pixel rate is low enough, the VASP1 ADC can performe several acquisitions during a pixel period, allowing noise reduction in the following digital processing.

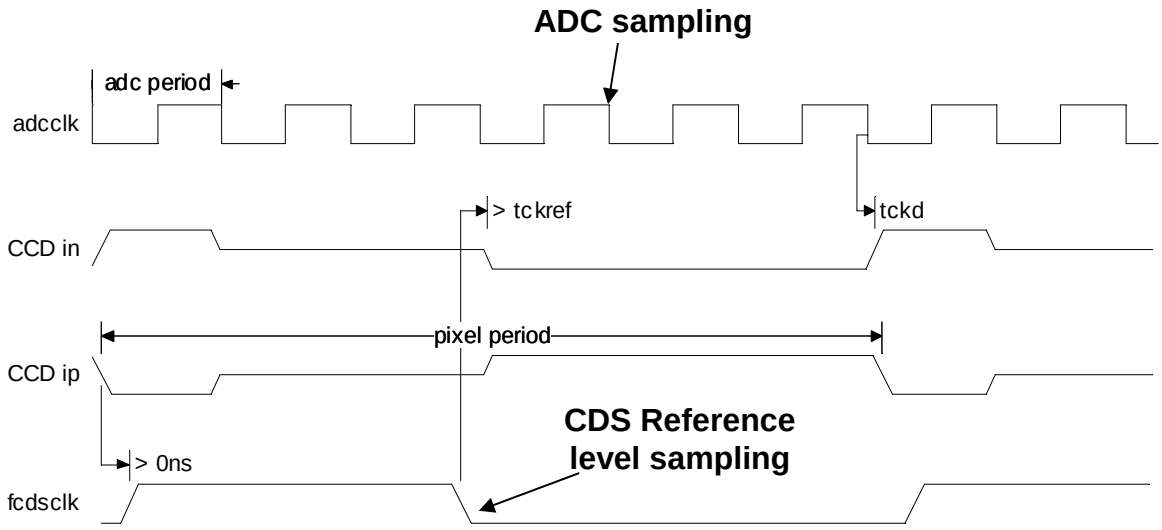


Figure 13 : Sequencing a multi-sampling on CCD signal

On the above figure, an example of sequence is given for a CCD signal multi-sampling application. In this case, the CDS is used to process the CCD signal. The ADC is permanently sampling the CDS output signal and performing the conversion to the output pixel bus. In this case, an external sequencer should distinguish which samples are useful (video signal) and which are not (reset, reference signal, CDS settling, etc.).

Another example should be on a differential CMOS signal using the ADC only. In this case, having an ADC clock n times faster than the pixel rate would simply leads to n samples per pixel.

12.5 OFFSET

There are two possibilities to inject offset in the VASP1. One is linked to the CDS and brings coarse offset with a gain of 1 through the COCP and COCN pins. The other is linked to the ADC and brings fine offset with a gain of ¼ through the FOCP and FOCN pins. The gain of those offsets is the ratio between the differential voltage on the offset inputs and the output code.

Note : The FOC input is internally masked during the ADC calibration so any voltage present is not taken into account.

12.6 Buffer consideration

The reference and offset voltages are internally buffered to bring the necessary high bandwidth and low noise performances. Those internal buffers can add a small offset above the voltages

applied on the pin vrefp_in, vrefn_in, cocp, cocn, focp and focn. These offsets are random error due to mismatch between components during IC manufacture.

Based on simulation results, the following potential offset should be taken into account:

Table 12 : Buffer offset deviation

Signal	Offset standard deviation
vrefp_in, cocp	0.8 mV
vrefn_in, cocn	0.6 mV
focp, focn	0.8 mV

12.7 CLAMP inputs and clock

In case of CCD detector, the DC level may be above the input level range and thus a DC decoupling capacitor is used for DC restore. The clamp allows fixing the DC voltage at the IC input (INP and INN pins) thanks to CLAMPP, CLAMPN inputs and a switch control CLAMPCLK.
When the DC needs to be set on the decoupling capacitor, the CLAMPCLK signal should be set to logical level one and thus the DC values presented on CLAMPP and CLAMPN are tied to INP and INN respectively. During this time, the detector signal cannot be seen by the IC.
If not needed, the CLAMPCLK should be tied to logic level zero. It may also be used as a second video input if the signal on the primary input (INP and INN) is not used (or high impedance).
Since the VASP will not see the detector signal during the fixing of DC voltage, the CLAMPCLK signal should be adjusted with respect to application constraint, typically during an unused slot of the frame.

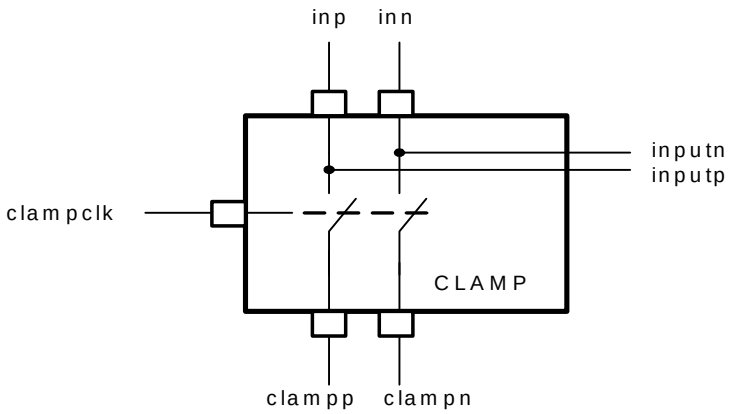


Figure 14 : Clamp input circuit

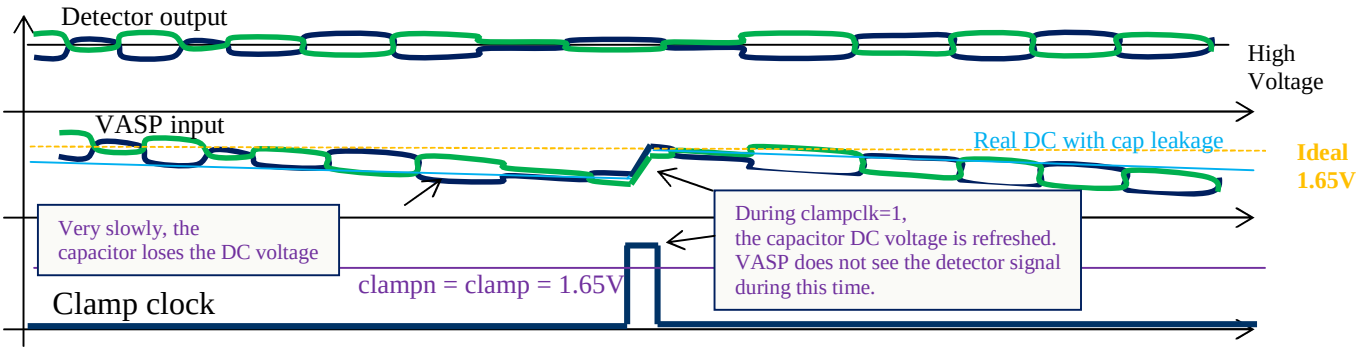


Figure 15: Example of detector / VASP signals across a decoupling cap and CLAMP function

12.8 Reference voltage

The reference voltage section is made to propose either internal or external reference options. If external references are preferred, they can be injected in the reference input pins and the reference generators turn off (pin ena_vref to ground).

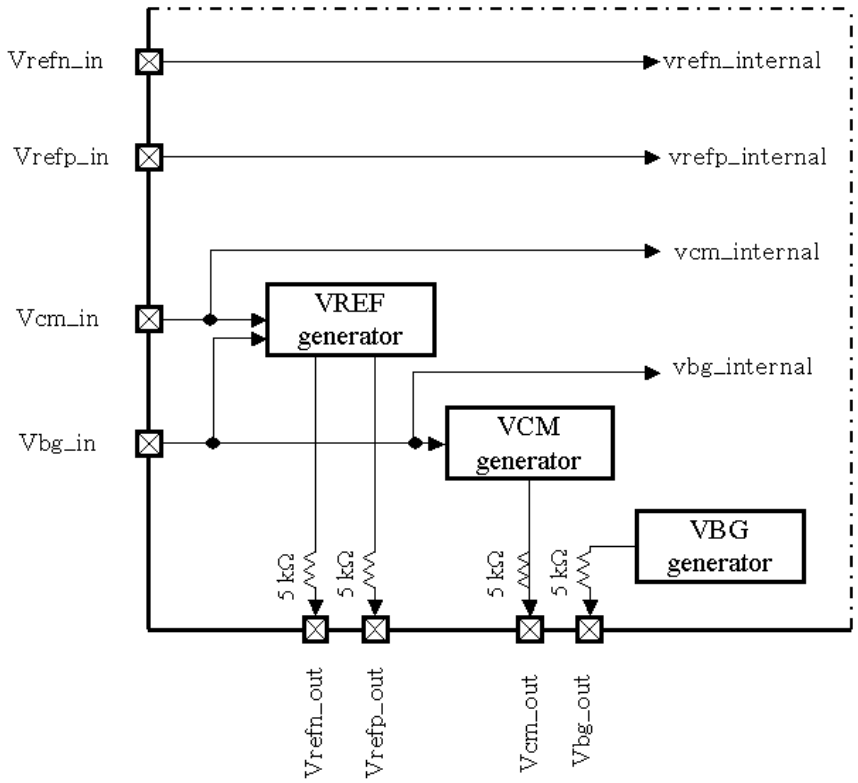


Figure 16 : Reference voltage block diagram

Note that the reference current is internally generated in both options (see “Bias Current Generation” chapter). That is why it is not represented in the above figure.

12.8.1 External references

The voltage references used by the VASP1 FM are the references presented on VBG_IN, VCM_IN, VREFP_IN and VREFN_IN. They can be externally supplied and should nominally correspond to the internal values.
The VBG_IN should be around 1.25 V. As the source of all the biasing current, the stability of this voltage is critical for the performances of the VASP1.
The VCM (for common mode), should be around 1.65V, but the stability is not so critical.
The ΔVREF (VREFP-VREFN) is optimum at 2V (maximum full range of the ADC). It can be chosen to be lower but VREFP and VREFN should be symmetrically placed around VCM. The ADC gain is directly modified by the value of ΔVREF.
The ena_vref pin can be put to logical level zero.

Note : There is no need to trim the internal reference if the external reference method is preferred.

12.8.2 Internal references

The VASP1 circuit can also provide the reference voltages. The ena_vref pin needs then to be connected to the logical level one.
Reference voltages are then available on pin VBG_OUT, VCM_OUT, VREFP_OUT, VREFN_OUT. The user has to route on the PCB those references to VASP input VBG_in, VCM_IN, VREFP_IN and VREFN_IN respectively. A 100 nF decoupling capacitor should be placed on each line to eliminate the internal noise (note that a 5 kOhm resistor is already placed inside the VASP1 circuit).

The internal voltage references can be trimmed based on the I2C registers VREFCM, VREFREF, VREFBG.

The recommended methodology is the following:

- Trim the VBG voltage so as to get the maximally flat voltage versus temperature over the considered temperature range.
- Trim the VCM so as to get as close as possible to 1.65 V
- Trim the ΔVREF so as to get as close as possible VREFP-VREFN = 2 V

12.8.3 Bias Current Generation

The ADC has a built-in bias current generator. However, an external current can also be used. The selection between the internal current and the external current is made through the IREFSEL register.
In normal operation (IREFSEL register to 1), the internal current is used. As represented in the following figure, the *iref* pin can be used for test purposes to monitor the internal bias current or tie to ground if not used at all.

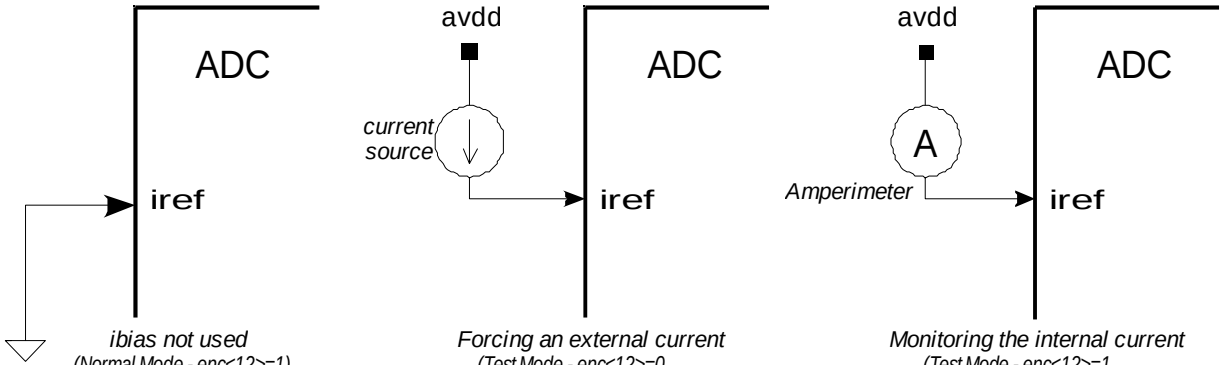


Figure 17 : Bias Current Generation – Existing modes

In the case of using external reference current (IREFSEL register to 0), the nominal current source can be made thanks to a resistor chosen to have an Iref current of 20uA (typical value is 120 kOhms over 3.3 V). However, all the IC biasing depends on the stability of this current (temperature, supply, process, etc.) and a simple resistor might not be sufficient for high performance application.

13. CALIBRATION MODE

The calibration consists in measuring the matching of the internal capacitor and determining an error coefficient for all those capacitors. This lead to a table of 30 coefficients of 13 bits signed.

The calibration should always be done after a time period that ensures the settling of the reference signals. This latency depends on the external filtering, knowing that the internal start-up is shorter than 50 ms.
To calibrate the ADC, the calibration shall be enabled : input ENACALIB at level 1. Then, the STARTCALIB should go to up and then after the calibration time should go to down. The output ENDCALIB may be at level 1 or 0 before the start of the calibration sequence, depending on the previous events ; during the calibration time, the output ENDCALIB is at level 0. The following figure shows the calibration sequence.

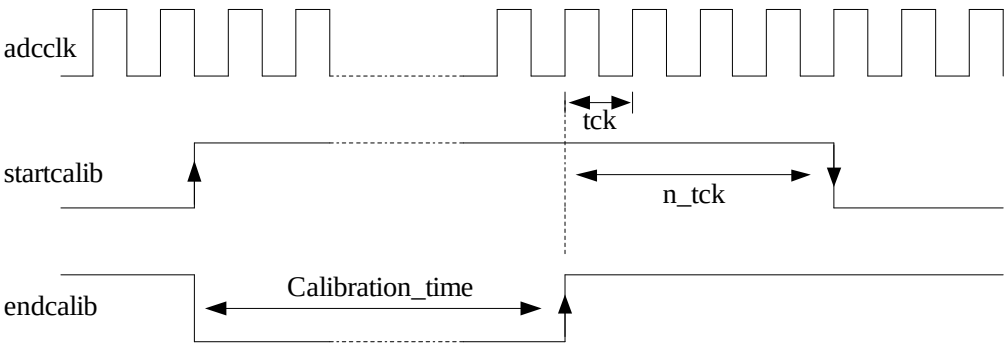


Figure 18 : Calibration sequence

To eliminate noise during the capacitor measurement, each measurement is averaged. The numbers of samples to be averaged are configurable through register NMEAN, by power of 2 values. The following table illustrates the relation between nmean and the number of conversions being averaged :

$$navg = 64 \times 2^{nmean}$$

The numbers of ADC clock cycles necessary to perform a calibration are equal to:

$$Calibration\_time = (navg \cdot 56 + 356)T_{CK}$$

After the calibration time, the *endcalib* goes up indicating the end of the calibration process. However to be able to use the calibrated ADC the startcalib has to go down after *n_tck* clock cycles. The number *n_tck* has to be at least one clock cycle.

If something goes wrong inside the calibration algorithm, an error flag is reported in one of the bit of the register ST1COEFOVERFLOW and ST2COEFOVERFLOW.

Note : the ENACALIB should always be at logic level one to take into account the calibration coefficient and get the calibrated linearity.

14. RESET MODE

Reset input RSTZ is active low, asynchronously asserted but it is internally disabled after 3 ADC clock cycles after detection.

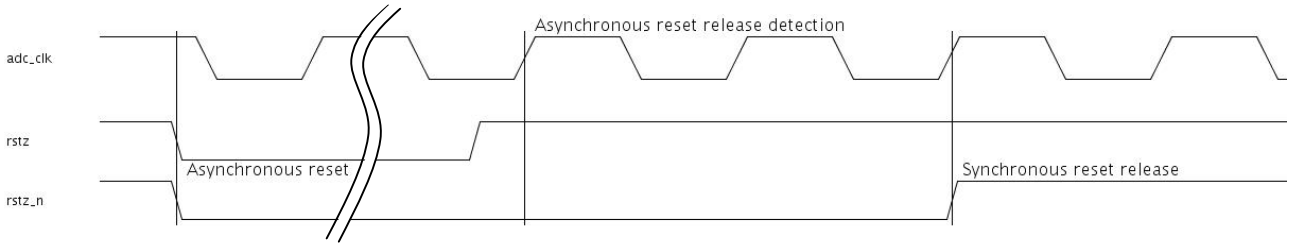


Figure 19 : Reset synchronization

The minimum duration time of the asynchronous low level is two clock periods. It is necessary to have a reset after every power on cycle to correctly set the digital states. A recommended practice is to disable the pixel bus (*ena_pixel* to zero) before a reset sequence has been completely performed to avoid sending wrong pixel code to the other circuits.

Note : the ADC should be running when performing this reset release. It means that the reference current must be working (either the internal current reference working with *VBG_IN* value or externally supplied through the IREF pin ; the selection is made by IREFSEL bit) and the ADC should be enabled (*ena_adc*).

15. I2C INTERFACE

VASP1 implements I^2C slave interface capable of accessing a register bank organized in 8 bit words. The I^2C block functionalities of interest are described in the following paragraphs.
It should be noted that a reset pulse must be applied before any activity on the SDA and SCL lines.
The SDA IO is an open-collector structure to allow bidirectional signal. An external pull-up (typicaly 3.3 kOhms) should be connected to VDD to ensure the regular behavior of this IO.
All transfers are MSB first.
A recommended practice is to read back a configuration after a write command to guarantee that the register has been correctly set. Another good practice is to read back or write the required configuration periodically to check the register content.

15.1 Start/Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition. This is illustrated by Figure 20.

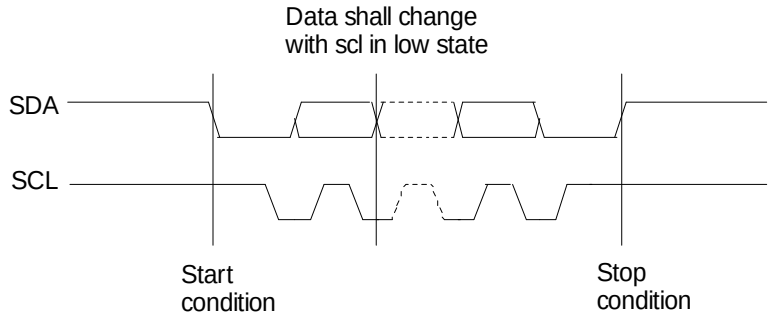


Figure 20 : start and stop conditions

The communication start injects a reset condition to the device's state-machine, so if an I^2C transaction hangs, the next start condition should clean the state machine.
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse.

15.2 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited.

For read operations the master will behave as a receiver and the slave as a transmitter. When this is the case, each data byte is followed by an acknowledge except the last one before the STOP or RE-START conditions. The not acknowledge will allow the slave to release the SDA line in order for the master to be able to issue the STOP or RE-START conditions.

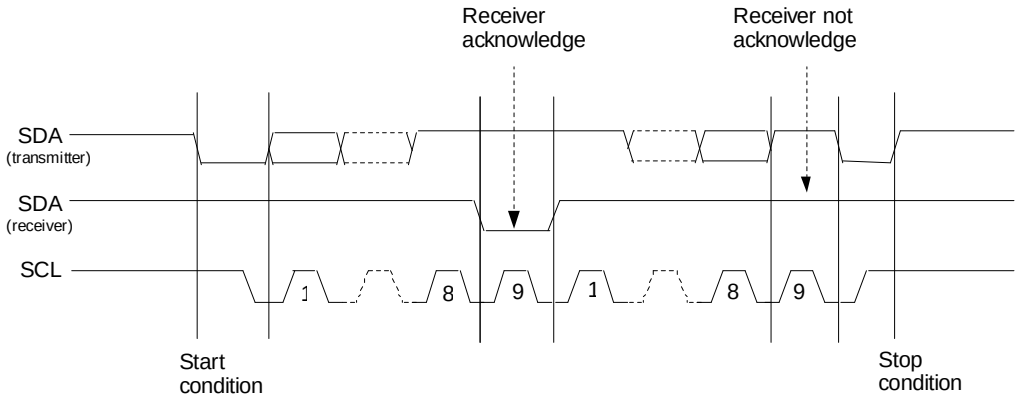


Figure 21 : protocol acknowledge

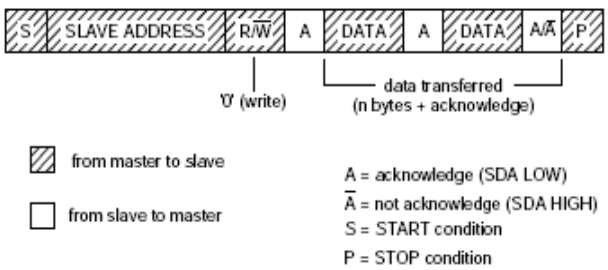
15.3 Stream

As described before, any data transfer must be initiated with a START condition. After that procedure, a slave indexing is performed, meaning that the slave address must be sent. The VASP1 I2C slave address 3 MSB have been hard-coded to “000”. The user can select one among 16 addresses by the I2C<3:0> pins (I2C<0> being the LSB).

Then a read/write bit is also sent. This bit will define the direction of the data bus (0 = write or Master to Slave, 1 = read or Slave to Master), and the direction cannot be changed during a transfer.

An acknowledge is executed from the slave to the master always, either for write or read operations.

Until here the procedure is the same for both operations (read/write), however, from now on there are some differences better illustrated in the next figures :



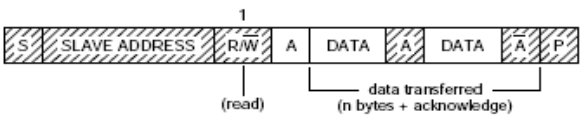


Figure 22 : write / read stream (from I²C bus specification)

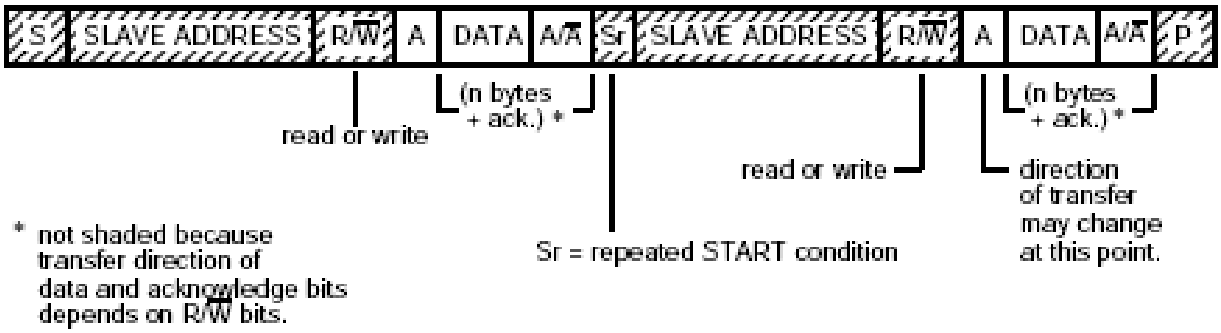


Figure 23 : combined stream (from I²C bus specification)

As shown, if a write is being done, the slave acknowledges the sent data. In the read case it is just the opposite case, the slave sends the data and the master acknowledges it.

Note : When performing a read operation, after the first acknowledge, the data bus direction is already defined from the slave to the master. So, it is **NOT** possible to define the register address to be read in the same operation, what would imply a byte transfer on the opposite direction. There is 3 possibilities to define the read address :

- To perform a write operation to the register address previous to the one to be read followed by a STOP condition. Meaning that if register n is to be read, register n-1 must be pointed by a write operation first and the address pointer (automatically incremented at the end of a transaction) will be pointing to register n.
- To initiate a write to register n containing only the slave address + op bit + register address, followed by a REPEATED START. This way the address will still be register n and the read operation can now be performed.
- To initiate a write to register n containing only the slave address + op bit + register address, followed by a STOP. This way the address will still be register n and the read operation can be STARTED now or later (it may be another operation with other slaves between the write and the read).

15.4 Functionality related to register bank interaction

Figure 22 illustrates the data frame necessary for a write operation. The start condition initiates communication followed by the slave address and the operation bit. The next bit is the slave acknowledge. Following the acknowledge, the master sends the first byte that contains the register bank address to be written. Again, the slave acknowledges the received byte. All remaining bytes sent by the master are the contents to be written to consecutive register bank positions.

Previously was referred that parameters defining the number implemented registers exist and leads to the following special operating conditions:

- If a write is performed to a non-existing register address, no acknowledge from the receiver is returned.
- If a read is performed on a non-existing register address, zero is returned.

After a global reset of VASP1, the internal address pointer will have the address of the first register (00h). To perform a write to other register, use the first data slot to define the new address. If the first write is to be performed on register 0, the first data slot must have register 0 address anyway, it cannot be used for register's data.

The address pointer will NOT return to the first register address whenever a STOP (or START) condition occurs, only on reset it will.

16. I²C REGISTERS

16.1 I²C Register map

The following table shows the content of the register bank, programmed by the I2C. The not used register in grey are either tied to zero or ignored (a value can be read/write but without effect). When indicated the 0 or 1 logical value should always be fulfill. No value others than the default one should be set into the register address not explained below.

Table 13 : I²C register map

Address	B7	B6	B5	B4	B3	B2	B1	B0	Default	Read / Write
00				0	0	nmean		0	0h	W/R
1	I2C_stg1cal0coef[7:0]								0h	W/R
2				I2C_stg1cal0coef[12:8]					0h	W/R
3	I2C_stg1cal1coef[7:0]								0h	W/R
4				I2C_stg1cal1coef[12:8]					0h	W/R
5	I2C_stg1cal2coef[7:0]								0h	W/R
6				I2C_stg1cal2coef[12:8]					0h	W/R
7	I2C_stg1cal3coef[7:0]								0h	W/R
8				I2C_stg1cal3coef[12:8]					0h	W/R
9	I2C_stg1cal4coef[7:0]								0h	W/R
A				I2C_stg1cal4coef[12:8]					0h	W/R
B	I2C_stg1cal5coef[7:0]								0h	W/R
C				I2C_stg1cal5coef[12:8]					0h	W/R
D	I2C_stg1cal6coef[7:0]								0h	W/R
E				I2C_stg1cal6coef[12:8]					0h	W/R
F	I2C_stg1cal7coef[7:0]								0h	W/R
10				I2C_stg1cal7coef[12:8]					0h	W/R
11	I2C_stg1cal8coef[7:0]								0h	W/R
12				I2C_stg1cal8coef[12:8]					0h	W/R
13	I2C_stg1cal9coef[7:0]								0h	W/R
14				I2C_stg1cal9coef[12:8]					0h	W/R
15	I2C_stg1cal10coef[7:0]								0h	W/R
16				I2C_stg1cal10coef[12:8]					0h	W/R
17	I2C_stg1cal11coef[7:0]								0h	W/R
18				I2C_stg1cal11coef[12:8]					0h	W/R
19	I2C_stg1cal12coef[7:0]								0h	W/R
1A				I2C_stg1cal12coef[12:8]					0h	W/R
1B	I2C_stg1cal13coef[7:0]								0h	W/R
1C				I2C_stg1cal13coef[12:8]					0h	W/R
1D	I2C_stg1cal14coef[7:0]								0h	W/R
1E				I2C_stg1cal14coef[12:8]					0h	W/R
1F	I2C_stg2cal0coef[7:0]								0h	W/R
20				I2C_stg2cal0coef[12:8]					0h	W/R
21	I2C_stg2cal1coef[7:0]								0h	W/R
22				I2C_stg2cal1coef[12:8]					0h	W/R
23	I2C_stg2cal2coef[7:0]								0h	W/R
24				I2C_stg2cal2coef[12:8]					0h	W/R
25	I2C_stg2cal3coef[7:0]								0h	W/R
26				I2C_stg2cal3coef[12:8]					0h	W/R
27	I2C_stg2cal4coef[7:0]								0h	W/R
28				I2C_stg2cal4coef[12:8]					0h	W/R
29	I2C_stg2cal5coef[7:0]								0h	W/R
2A				I2C_stg2cal5coef[12:8]					0h	W/R
2B	I2C_stg2cal6coef[7:0]								0h	W/R
2C				I2C_stg2cal6coef[12:8]					0h	W/R
2D	I2C_stg2cal7coef[7:0]								0h	W/R
2E				I2C_stg2cal7coef[12:8]					0h	W/R
2F	I2C_stg2cal8coef[7:0]								0h	W/R
30				I2C_stg2cal8coef[12:8]					0h	W/R
31	I2C_stg2cal9coef[7:0]								0h	W/R
32				I2C_stg2cal9coef[12:8]					0h	W/R

33	51	I2C_stg2cal10coef[7:0]								0h	W/R
34	52				I2C_stg2cal10coef[12:8]					0h	W/R
35	53	I2C_stg2cal11coef[7:0]								0h	W/R
36	54				I2C_stg2cal11coef[12:8]					0h	W/R
37	55	I2C_stg2cal12coef[7:0]								0h	W/R
38	56				I2C_stg2cal12coef[12:8]					0h	W/R
39	57	I2C_stg2cal13coef[7:0]								0h	W/R
3A	58				I2C_stg2cal13coef[12:8]					0h	W/R
3B	59	I2C_stg2cal14coef[7:0]								0h	W/R
3C	60				I2C_stg2cal14coef[12:8]					0h	W/R
3D	61	SIGNAL		CDSGAIN		0	0	0		0h	W/R
3E	62									0h	W/R
3F	63									0h	W/R
40	64			VREFCM[3:0]						0h	W/R
41	65			VREFREF[3:0]						0h	W/R
42	66		0	0	0	COCINV				0h	W/R
43	67		VREFBG[6:0]							0hh	WR
44 to 5D	68 to 93									0h	W/R
5E	94				IREFSEL	0	0	0	0	10h	W/R

A1	161	stg1coefoverflow[7:0]		0h	R
A2	162		st1coefoverflow[14:8]	0h	R
A3	163	stg2coefoverflow[7:0]		0h	R
A4	164		st2coefoverflow[14:8]	0h	R

16.2 Register description

The registers are classified by function below. The following sections described these register content.

Table 14 : VASP1 register description

Name	Adress (H)	Description
ADCconf	00	ADC configuration
I2C_stg1cal0coeff / I2C_stg1cal14coeff	01 to 1E	Read/write ADC Stage 1 Coefficients 1 to 14
I2C_stg2cal0coeff / I2C_stg2cal14coeff	1F to 3C	Read/write ADC Stage 2 Coefficients 1 to 14
CDSconf	3D	CDS configuration
ANAConf	40 to 43 and 5E	Analog Configuration register
stg1coefoverflow	A1 to A2	Stage 1 Detection of overflow during calibration
stg2coefoverflow	A3 to A4	Stage 2 Detection of overflow during calibration

16.2.1 ADCconf register

The register is used for ADC calibration configuration.

Table 15 : ADCconf register specification

Bit	CDSconf Address 00h (00dec)	Default value	Description
7 :3	Not Used	00000	
2:1	nmean	00	Number of averaging during calibration (see chapter 13)
0	Not Used	0	

16.2.2 CDSconf register

The register is used for CDS calibration configuration.

Table 16 : CDSconf register specification

Bit	CDSconf Address 3Dh (61dec)	Default value	Description
7	SIGNAL	0	CDS mode 0 : CCD mode in CDS 1 : CMOS mode in CDS
6	Not Used	0	
5	CDSGAIN	0	CDS gain 0 : gain 2 1 : gain 1
4:0	Not Used	00000	

16.3 ANAconf register

The ANAConf registers are used to control the trim of the references and the inversion of the COC sign for the CDS.

Table 17 : ANAconf register 40h specification

Bit	ANAconf Address 40h (64dec)	Default value	Description
7:6	Not Used	0	
5:2	VREFCM[3:0]	0000	Common mode reference trim The design target is 1.65V. Each LSB is 12 mV variation. The trim slope is negative (the higher the register the lower the voltage).
1:0	Not Used	0	

Table 18 : ANAconf register 41h specification

Bit	ANAconf Address 41h (65dec)	Default value	Description
7:6	Not Used	0	
5:2	VREFREF[3:0]	0000	Vrefp Vrefn trim The design target is Vrefp-Vrefn=2V. Each LSB is 15mV variation. The trim slope is negative (the higher the register the lower the voltage).
1:0	Not Used	0	

Table 19 : ANAconf register 42h specification

Bit	ANAconf Address 42h (66dec)	Default value	Description
7:4	Not Used	0000	
3	COCINV	0	Inversion of COC reference in CDS 0 – Cocn, Cocp are routed for CCD signals 1 – Cocn, Cocp are routed for CMOS signals
2:0	Not Used	000	

Table 20 : ANAconf register 43h specification

Bit	ANAconf Address 43h (67dec)	Default value	Description
7	Not Used	0	
6:0	VREFBG[6:0]	0000000	VBG temperature slope trim. The temperature slope should be adjusted to minimize the temperature variation. The absolute value of the *vbg_out* voltage should be 1.25 V. Each step of temperature slope trim provides roughly 2 mV variation on VBG. The trim slope is negative (the higher the register the lower the voltage).

Table 21 : ANAconf register 5Eh specification

Bit	ANAconf address 5Dh (93dec)	Default value	Description
7:5	Not Used	0	
4	IREFSEL	1	Reference current selection 0 Iref input current provided externally 1 Internal current reference
3:0	Not Used	0000	Reference current in ADC stage 1 MDAC 00 Nominal current 01 Double current 10 1/3rd current 00 Nominal current

17. ASSEMBLY GUIDELINES

17.1 System Level Clock Issues

The Video Chain front-end and ADC sampling instants are the most critical steps in the analog processing of the signal. Noise coupled via the substrate during that short time interval may impact the performance of the system. Internally to the VASP1 FM, extreme care is taken to minimize/eliminate any digital activity that can inject noise into the substrate during this time interval, in order to ensure a quiet sampling instant for the ADC's in the VASP1 FM.

At system level, the same care must be taken. For this, the following guidelines should be followed:

- Increase as much as possible the time between output pad activity and analog sampling instant.
- Delay all digital activity clock edges from the sampling instance in order to ensure quiet sampling instance in the analog domain.

These goals are best achieved if all clock domains in the system have a fixed phase relationship. Phase relations could then be defined such that the sampling time interval is respected.

17.2 ESD

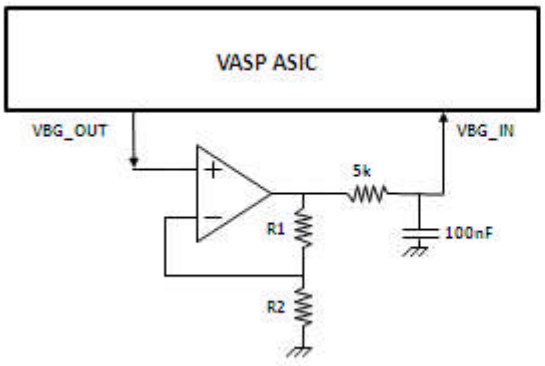
The VASP IC has been designed with specific ESD protection in every pins. The measurement show that VASP can handle 1 kV HBM zap, falling into ESD class 1C classification.

17.3 Reference absolute value and temperature stability

When internal voltage references are used, the VCM, VREFP and VREFN voltages are based on the VBG reference.
The VBG voltage should be trimmed with respect to the temperature stability needs of the equipment. For the most flat response over temperature, the absolute value of the VBG voltage might be low and as a consequence slightly limit the ΔVref (VREFP – VREFN, i.e. the ADC range).

For the most constrained applications that require both optimum temperature stability and 100% of ADC range, the following circuit can be used. After a trim of the VBG voltage to the optimal value (where the temperature does not affect the VBG voltage), the ideal 1.25 V value can be generated thanks to the op amp circuit. Thanks to this, the user can place the VCM, VREFP and VREFN at the best value for a given application and thus reach full ADC range.

Opamp circuit shall be low input current, low band-pass and present good temperature stability (few ppm/°C)



$$VBG_{IN} = VBG\_OUT \times (1 + \frac{R1}{R2})$$

17.4 Decoupling Components

As shown in the figure below :

- Vrefp, Vrefn, Vbg and Vcm must be externally decoupled by 100nF capacitors to agnd.
- All the power supplies should be decoupled by 10uF, 100nF and 1nF capacitors. It is recommended to locate the 1nF capacitors as close as possible to the chip and those capacitors should be good quality capacitors, like RF ceramic ones.

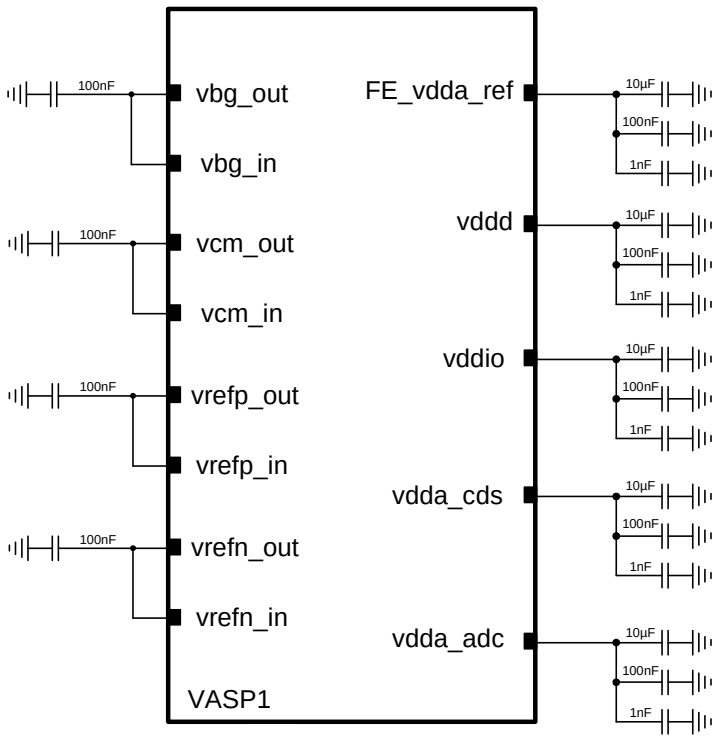


Figure 24 : Decoupling capacitors connections of VASP1 with internal reference use

17.5 Offset generation

FOC*, COC* offset voltages shall be generated from external sources filtered to reduce as much as possible the noise bandwidth. Low noise internal amplifier buffers those signals and the resulting noise shall be negligible.

17.6 SCAN IO

The SCAN IO are used for electrical tests. This special test mode is entered when the pin SCANMODE is at high level.
To disable this test feature, the user should tie all the inputs to digital GND (GNDD) : SCANRSTZ, SCANMODE, SCANIN, SCANCLK and SCANEN. The output SCANOUT can be let unconnected.

END OF DOCUMENT