High-Speed High-Resolution ADC Technology

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ABSTRACT:

This document contains the Summary Report for the project ref. 20263/NL/LvH – High-Speed High-Resolution ADC Technology.

The work described in this report was done under ESA contract. Responsibility for the contents resides in the author or organization that prepared it.

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1 Executive Summary

Introduction

This project consisted in the development and silicon implementation of a new 13-bit 80MS/s ADC technology with buil-in-self calibration (BISC), that improves linearity, energy-efficiency, cost and reliability in new applications in the fields of communications, imaging, physics experiments and space.

A total of five partners were involved in the project: S3 Portugal as the prime contractor, Coreworks from Portugal for digital BISC design and FPGA implementation, Uninova from Portugal for supporting silicon testing, TRAD from France conducted the radiation tests and IMEC from Belgium supported chip manufacturing with foundry TSMC.

This project was funded as part of the ESA "OPPORTUNITY FOR PORTUGAL ON CLOSE-TOMARKET TECHNOLOGY DEVELOPMENTS" ref. AO/1-4686. The difference between the cost of the activity and the price of the contract, which was over 50% of the total, was funded by S3 Portugal through its internal funds.

Key Achievements in Phase 1

In Phase 1, S3 Portugal designed the 13-bit 80MS/s ADC system and the on-chip Analog BISC component including a white gaussian noise generator (WGN) followed by a 16-bit sub-binary programmable gain amplifier (PGA). We also investigated and implemented, for the first time in our company activities, various radiation hardening design techniques including low transistor saturation voltages, enclosed transistors and special guard rings. A test chip was fabricated in a standard, low-cost TSMC 90nm Low-Power 1.2V process without analog options. The ADC core occupies a die area of only 0.88mm^2 or 41% below target and the complete chip uses only 1.28mm^2, or 29% below specification.

The Digital BISC Algorithm was specified by S3 Portugal and was designed and implemented into an FPGA by Coreworks. Coreworks also developed the FPGA board and synthesized the BISC algorithm using a Xilinx Virtex-5 FPGA operating up to 100MHz.

S3 Portugal implemented a high-performance testing board for evaluating the 13-bit 80MS/s ADC and we used two assembly options. Firstly, a 80-pin package was used. It resulted in good performance but was limited to 40MS/s due to the chip small die area and large package cavity resulting in long bounding wires introducing important inductance effect. Secondly, we designed and produced a special-purpose testing board in which the chip dies are assembled directly (chip-on-board assembly). This resulted in greatly improved measurements at 80 MS/s which enabled us to conduct extensive performance tests.

The 13-bit 80MS/s ADC system performance was evaluated successfully and the built-in self-calibration (BISC) algorithm was successfully implemented and verified in an FPGA.

Static DNL and INL specifications were met before and after calibration. Power dissipation at 80MS/s for a single 1.2V supply is only 93mW, 20% below specification. Dynamic performance at 40MS/s was very close to specification with measured 10.8-bit ENOB versus a specified 11.0-bit ENOB. Dynamic results at 80MS/s, including 10.2-bit ENOB before calibration and 10-8-bit ENOB after calibration, were slightly behind the 11-bit target due to three external factors: i) on-chip noise generated by the switching at 80MS/s of the 13 output digital drivers used in the test chip for data interfacing – this problem can be overcome by using an on-chip RAM for acquiring the ADC outputs at full speed and transmitting the data to the test equipment a low speed, ii) noise around the signal frequency originated in the input signal generator and iii) jitter noise from the sampling clock generator.

TRAD implemented a testing platform for biasing the ADC chips during irradiation and for experimental evaluation of the ADC for SEL and for different TID doses. A 64-pin package with open lid was used for assembly. The chip was proved to be robust to SEL up to 70MeV.cm²/mg, as specified. The TID tests were performed up to the specified 100krad dose but were not fully conclusive since package, board design and testing equipment limited the ADC conversion rate to 40MS/s and the effective resolution to only 8-bit ENOB.

Key Achievements in Phase 2

S3 Portugal devised a new testing infrastructure to enable high-performance ADC tests during radiation testing, based on chip-on-board (CoB) assembly and using a system with Mother Boards and multiple Daughter Boards. The Daughter Board is a small board that contains the CoB die and only a few external passive components for decoupling purposes. The ADC analog input signal is connected directly to the Daughter Board to improve performance. The Mother Board contains all active electrical components, switches and main connectors. Each IC sample to be tested has a dedicated CoB assembly and Daughter board. S3 Portugal delivered to TRAD one Mother Board and six Daughter Boards, all fully populated.

With this system, and furthermore by using an input signal filter and sampling clock generator provided by S3 Portugal, TRAD was able to measure ADC static (DNL, INL) and dynamic (FFT measurements) performance at 80 MS/s close to the results obtained at S3 Portugal lab. The ADC was fully functional up to the newly specified 1076krad (a dose ten times higher versus Phase 1) and all 5 samples irradiated achieved over 10.2-bit ENOB dynamic performance (without calibration) at 1076 krad with 80 MS/s sampling rate and 10.7 MHz input signal

Also the Digital BISC algorithm was improved by Coreworks in functionality and the full ADC system including calibration was again tested in detail in Phase 2 using the new testing infrastructure.

Technical Publications & Evaluation of Technology

This work included significant R&D activities in the field of ADC design as well as radiation hardening design techniques, which resulted in one published paper and one invited conference presentation. We have also written an extended paper to be submitted soon to an IEEE Journal.

We have prepared marketing material that we have been presenting and delivering to customers. We have contacted customers for space and non-space related applications resulting in 5 customer leads for space applications and 7 customer leads for non-space applications. These activities resulted in two design wins for non-space applications, both based on modifications performed on the 13-bit 80MS/s ADC implemented as part of this project.

During Phase 1 of the project, we essentially discussed and presented to potential customers based on the performance of the ADC as validated by S3 Portugal, not so much on the radiation test results due to the various test limitations experienced in Phase 1.

In Phase 2 of the project, which was just completed now (November 2009), TID radiation tests results proved very successful due to the improved testing infrastructure. Now that we have achieved outstanding radiation test results, we will start presenting these results to space-related companies.

Conclusions

Overall we believed the project was completed successfully and the results are very positive. The 13-bit 80MS/s ADC systems was designed into a standard, low-cost TSMC 90nm LP 1.2V process, was right first-time and achieved the static and dynamic target specifications, with die area and power dissipation better than specification by 41% and 20%, respectively. The built-in self-calibration (BISC) algorithm was successfully implemented and verified in an FPGA.

The ADC chip was proved to be robust to SEL up to 70MeV.cm²/mg, as specified, and the ADC was fully functional and achieved good static and dynamic results up to a newly specified 1076krad (or 1Mrad, a dose ten times higher than initially specified).

The project took longer than initially planned essentially due to delays during Phase 1. This was mainly due to lengthy design verifications prior to chip implementation and the need to implement a second testing system based on chip-on-board.

Importantly, we managed to secure design wins for non-space applications based on the ADC developments made in this project.

This is the first time S3 Portugal implements radiation hardening design techniques and the outstanding radiation results achieved in the project are particularly encouraging for enabling S3 Portugal to enter into the business of designing high-performance ADCs for space applications.

2 Key Project Goals

High-performance analogue-to-digital converters (ADC) are a critical building block in a growing number of applications for interfacing real-world analogue signals with digital data. Moreover, emerging applications in the fields of communications, imaging, physics experiments and space are setting new requirements in terms of integrated circuit die area, power dissipation, robustness and cost.

This project consisted in developing and implementing in silicon a new high-speed high-resolution ADC technology that improves linearity, energy-efficiency, cost and reliability in these target applications. The ADC will include

The five main technical objectives for this new ADC technology were defined at the beginning of the project as follows:

1. Linearity: Resolution of 13-bits and 11-bit ENOB (effective-number-of-bits) for input frequency of 10MHz

2. Speed: Sampling rate of 80MS/s (conversion speed).

3. Low-Power: Energy-efficiency: better than 0.5 pico-Joules per conversion step in typical conditions and excluding reference circuitry and digital I/O buffers.

4. Low Cost: Standard CMOS manufacturing process with 90nm 1-poly 8-metals from a pure-play foundry to lower cost and nominal operating voltage of only 1.2V.

5. Reliability: Robustness of the custom designed mixed analogue-digital sections against supply voltage variations and space radiation effects.

Table 1: Summary of Key Technical Objectives for the ADC technology.

Parameter	Specification	Comment
Resolution	13-bit	
Sampling Rate	80MS/s	
Fabrication Process	90nm standard CMOS technology	
Supply Voltage	1.2V ±10%	Single supply voltage
Junction Operating Temperature	-40ºC to +125ºC	
Die Area ADC Core	< 1.5mm^2	
Die Area Analog BISC	< 0.3mm^2	
Total Ionizing Dose (TID)	100krad	Use of rad-hard design techniques
Single-Event Latch-up (SEL)	70 MeV.mg^{-1}.cm^2	Use of rad-hard design techniques
Differential Non-Linearity Error	±1.5LSB	Typical
Integral Non-Linearity Error	±1.5LSB	Typical
Signal to Noise Ratio (SNR)	70dB	Typical, with fin= 10MHz
Total Harmonic Distortion (THD)	-72dB	Typical, with fin= 10MHz
Effective Number of Bits (ENOB)	11.0-bit	Typical, with fin= 10MHz
Power Dissipation	116mW	ADC core only; excluding auxiliary and analog BISC circuits.

3 Approaches Undertaken to Reach the Objectives

3.1 Improved Linearity

To improve linearity, in this context non-linearity errors (DNL, INL) and effective number of bits (ENOB), a new BISC (built-in self-calibration) technique for high-speed ADCs based on a white Gaussian noise (WGN) on-chip stimulus was implemented.

This new BISC technique consists in the following steps:

a) applying a WGN analogue input stimulus to the ADC input (Analog BISC Component),

b) digitizing the WGN input using the ADC at the maximum sampling rate,

c) computing the histogram of the resulting output codes (Digital BISC Algorithm),

d) calculating the calibrating codes from the histogram (Digital BISC Algorithm),

e) correcting the ADC codes using the computed calibrating codes in normal operation at maximum sampling rate ("on-the-fly") (Digital BISC Algorithm).

The Analog BISC Component, which includes a WGN circuit, a fine-resolution programmable gain amplifier (PGA) as well as controlling circuitry was designed and implemented on-chip by S3 Portugal.

The Digital BISC Algorithm was specified by S3 Portugal and was designed and implemented into a Xilinx FPGA by Coreworks. Coreworks also developed the FPGA board.

3.2 Improved Energy Efficiency

To improve energy-efficiency, the following approaches were employed:

Use of proprietary equation-based design optimization engine which accelerates analogue design and enables system and circuit optimization for a given set of target specifications and a specific silicon manufacturing process. The output is a fully sized net-list that is validated and fine-tuned with a standard electrical simulator.

As part of this activity, the ADC design was fully mathematically modeled and coded into the design engine and optimized for the target specifications and silicon process. This also permits a cost-effective customization for new applications in the future.

In order to reduce power dissipation and improve die area, an optimized architecture was developed and special amplifier sharing techniques were used.

Also we have implemented a frequency-adaptive current biasing scheme whereby the biasing current of the amplifiers scale automatically with the sampling rate. This results in a more robust ADC and more importantly the power dissipation scales almost linearly with the sampling rate. We have tested this feature by conducting performance measurements at 40MS/s and 80MS/s.

3.3 Improved Reliability

During the ADC design, optimization and sizing of all devices used in the analogue circuitry of the ADC, extensive Monte-Carlo electrical simulations were performed considering worst-case corner deviations (+/-20%) in both threshold-voltages and mobility BSIM3v3.3 device parameters.

In order to reach a good latch-up free performance many guard rings, with many contacts to VDD or to VSS, enclosing groups of transistors and improved substrate biasing techniques were designed during the layout phase in critical parts of the circuit in the Analogue BISC as well as in the ADC core. These techniques minimized the problems of the sub-threshold currents which increase due to induced parasitic structures turned-on by ionization.

We also implemented radiation hardening by design in the Analogue BISC and ADC core to cope with the changes in the threshold voltages and mobility in MOS transistors due to TID (total ionizing dose) effects in space applications.

3.4 Low-Cost Standard Manufacturing Technology

Even though CMOS and BiCMOS technology are naturally hardened against radiation, their tolerance levels are not always compatible with military and Space requirements.

However, modern deep sub-micron technologies tend to be more resistant to TID effects than previous technologies thanks to their thinner oxides. Therefore a standard P-well Bulk 90nm CMOS technology (not the more expensive SOI-CMOS) was preferred rather than a 0.18um one. No analog options, such as MiM caps, were employed.

We decided to chose TSMC since they are the leading foundry and have the best 90nm process as well as the best and most reliable transistor models for simulation. As we have designed analog cells with radiation hardening techniques, and since these methods violate DCR errors, it was necessary to liaise closely with TSMC to obtain permission for manufacturing an IC with such DRC errors.

3.5 High-Performance Testing Infrastructure

The testing infrastructure is a critical component when testing high-performance ADC.

This is particularly true in this project as it turned-out that the testing infrastructure assumed indeed a central role in a) extracting the most of the ADC performance at S3 Portugal labs, and b) obtaining high-performance results during radiation tests at TRAD labs.

Phase 1- Performance Tests Performed by S3 Portugal

In Phase 1 of the project S3 Portugal implemented a high-performance testing board and used a 80-pin package for chip assembly. The tests results indicated very good performance up to 40MS/s sampling rate and degrading performance beyond that point; we identified the problem as related to the small die area and large package cavity resulting in long bounding wires (over 3mm) introducing important inductance effects above 40MS/s that clearly limit performance.

To overcome these limitations, we decided to design and produce a special-purpose testing board where the dies are assembled directly on the test board (so-called chip-on-board (CoB) assembly). The test results improved significantly at 80 MS/s and this allowed us to achieve the targeted ADC specifications.

Phase 1- Tests Performed by TRAD

In Phase 1 of the project TRAD implemented a testing platform for biasing the ADC chips during irradiation and experimental evaluation of the ADC for SEL and for different TID doses. A 64-pin package with open lid was used for assembly. The radiation tests were successful in terms of proving the ADC functionality under radiation effects but the testing platform developed by TRAD proved inadequate for verifying the full-performance of the ADC, since dynamic performance was limited to 8.2-bit ENOB (as opposed to close to 11-bit ENOB as measured in S3 Portugal labs). This was mainly due to the following three factors: i) inductance effects in the package limited tests to 40MS/s, ii) inadequate test board design for high-frequency, high-performance tests and iii) inadequate testing equipment, namely input filter and sampling clock generator.

Phase 2 – Tests Performed by S3 Portugal and by TRAD

In Phase 2 of the project, S3 Portugal devised a new testing infrastructure platform to enable high-performance ADC tests during radiation testing by TRAD. This new testing platform is based on chip-on-board assembly and uses a Mother Board and multiple Daughter Boards.

The Daughter Board is a small board that contains the CoB die and passive components for decoupling purposes. The ADC analog input signal is connected directly to the Daughter Board to improve performance. The Mother Board contains all active electrical components, switches and main connectors. The I/Os between Daughter Board and Mother Board are interfaced via connectors that connect directly after plugging in the Daughter Board.

Each IC sample to be tested has a dedicated CoB assembly and Daughter board. S3 Portugal delivered to TRAD one Mother Board and six Daughter Boards.

With this system, and furthermore by using the same input signal filter and sampling clock generator, TRAD was able to obtain ADC dynamic performance at 80 MS/s of about 10.2-bit ENOB (without calibration enabled), which is over 4 times better than during Phase 1 and close to the results obtained in the S3 Portugal lab.

With this new testing infrastructure in place it was also possible to extend the TID dose from a maximum of 100 krad in Phase 1 to up to 1076 krad in Phase 2 (10 times more). All the 5 IC samples irradiated achieved full ADC performance at 1076 krad with 80 MS/s sampling rate and 10.7 MHz input signal.

4 Work Packages Overview and Key Personnel

The project started in November 2006. Phase 1 of the project was completed in September 2008. Phase 2 of the project was started in March 2009 and was completed in November 2009.

The project took longer than initially planned essentially due to delays during Phase 1. This was mainly due to lengthy design verifications prior to chip implementation and the need implement a second testing system based on chip-on-board.

Table 2: Overview of project work packages.

Ref.	Ref.	Work Package Title	Responsible Company
Phase 1	WP1	Project Management & Reporting	S3 Portugal
	WP2	Design & Implementation in Silicon	S3 Portugal
	WP3	Digital BISC - Design & Implementation in FPGA	Coreworks
	WP4	Fabrication of IC	IMEC
	WP5	Implementation of Prototype #1	S3 Portugal
	WP6	Validation ADC in Silicon & BISC in FPGA (Phase 1)	S3 Portugal
	WP12	Radiation Testing (Phase 1)	TRAD
Phase 2	WP3	Digital BISC - Design & Implementation in FPGA, Improvements on Phase 1	Coreworks
	WP10	Implementation New Testing Infrastructure for Prototype #1	S3 Portugal
	WP11	Validation ADC & BISC in FPGA	S3 Portugal
	WP13	Radiation Testing Under Extended TID Dose and New Test Infrastructure	TRAD, S3 Portugal
	WP14	Evaluation of Technology	S3 Portugal

Table 3: Key personnel who participated in the project.

Name	Company	Work Packages
Dr. Bernardo Henriques	S3 Portugal	Contributed to all work packages.
Dr. Bruno Vaz	S3 Portugal	WP1, WP2, WP5, WP6, WP14
Dr. Joao Goes	S3 Portugal, Uninova	WP1, WP2, WP5, WP6
Dr. Nuno Paulino	S3 Portugal, Uninova	WP1, WP2, WP5, WP6
Mr. Marco Rodrigues	S3 Portugal	WP1, WP2, WP5, WP6, WP10, WP11
Mr. Pedro Faria	S3 Portugal	WP2
Mr. Nuno Penetra	S3 Portugal	WP2
Mr. Rui Piloto	S3 Portugal	WP2
Mr. João Neto	S3 Portugal	WP2
Mr. Miguel Santos	S3 Portugal	WP2
Mr. Tiago Domingues	S3 Portugal	WP2
Mr. Rui Monteiro	S3 Portugal	WP1, WP2, WP5, WP6, WP10, WP11
Mr. Erik Snelling	S3 Portugal	WP5, WP6, WP10, WP11
Dr. Jose de Sousa	Coreworks	WP3
Mr. Nuno Lourenço	Coreworks	WP3
Mr. Steven Redant	IMEC	WP4
Mr. Luc Laeveren	IMEC	WP4
Mr. Paul Ribeiro	TRAD	WP12
Mr. Alexandre Rousset	TRAD	WP13
Mr. Lemuel Coquelet	TRAD	WP12, WP13
Mr. Enoal Le Goulven	TRAD	WP12

5 Overview of the ADC System and Design Considerations

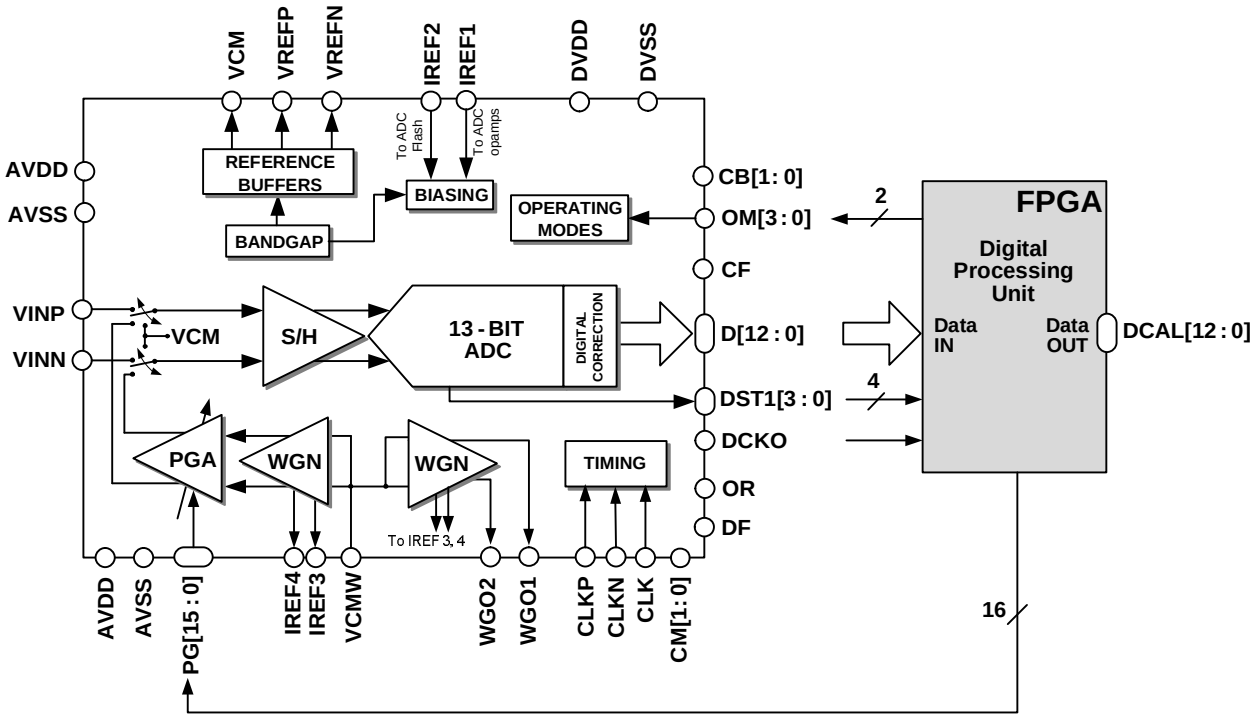

Figure 1. Block diagram of the proposed integrated ADC solution with BISC functionality.

5.1 ADC Core

The 13-bit A/D conversion system consists of an input fully-differential sample-and-hold (S/H) followed by pipeline core. This pipeline core consisting of one 3.5-bit stage followed by height stages with 1.5-bit per stage and by the last stage which uses a 2-bit flash quantizer. This distribution of the resolution per stage was carefully tailored by using S3's internal design methodology, in order to meet the best trade-off between power dissipation, calibration requirements and die area.

The ADC sample-and-hold circuit is based on a gain-one flipped-around architecture. This circuit has unitary gain and maximum feedback factor (around 1) requiring the lowest current consumption from the amplifier to achieve the needed Gain-Bandwidth product. On the other hand, this topology is gain insensitive since there is no capacitive ratio in the gain definition.

The ADC MDAC circuits use a flip-around configuration. Special attention was paid to the coding of digital control signals x, y, and z, in order to guarantee that the INL has a symmetrical shape. This is very important for an effective calibration of the ADC.

The amplifiers used in each ADC stage employed a two-stage architecture consisting of a folded-cascode input stage followed by a differential pair second-stage. Enhanced cascode-compensation was used to improve the bandwidth over the conventional Miller compensation. Since the second stage is a differential pair, two common-mode feedback circuits were needed, one circuit to adjust the common-mode of the first stage and another to adjust the common-mode of the second stage. Although the amplifier requires two CMFB circuits, its implementation is easier than a single CMFB due to the high gain of the amplifier.

The flash quantizers used in each ADC stage, except for the first stage, consist of a bank of comparators followed by a bubble suppressor and by a thermometer-to-binary digital encoder. Each comparator comprises an input SC divider network to define the threshold level, followed by a single-stage preamplifier and by a dynamic positive-feedback latch. In the first stage, a pre-amplification stage was added to the comparator to improve the off-set performance.

The ADC auxiliary circuits comprise reference generation, buffering circuitry and biasing circuitry.

5.2 BISC Algorithm Development and Modelling Tool

The BISC algorithm consists in 3 main steps:

1) Adjust the standard deviation of the on-chip WGN generator to the desired value, by successive approximations and using a 12-bit sub-binary programmable-gain-amplifier (PGA) for this purpose;
2) Calibrate the gain-error of the ADC;
3) Calibrate the non-linearity errors of the ADC.

During this project some important improvements in the BISC algorithm have been achieved, mainly to relax the comparators offset specifications without compromising the accuracy of the calibration codes calculations. The goal of these improvements was to establish a 64-code bin-width, keeping in mind that the bins must catch the segment transition codes. Since the maximum comparators offset specification is 15mV, which corresponds to a maximum deviation of 118 codes, it is necessary to cover that code length for each side of the ideal transition code between segments.

Instead of using a single bin with a 256-codes bin-width, 7 bins of 64 codes bin-width are used now instead (named “heptabin technique”). For each one of the seven bins the calculations of the Deviations Dev[k] are computed. The bin with a higher absolute value of deviation contains the transition and is selected to enter in the calibration codes calculation. By using bins with only 64 codes instead of 256 codes the precision of the algorithm is improved and the required number of samples is smaller, thereby making the calibration cycle faster.

In order to validate the implementation of the BISC algorithm, a modelling tool was developed in software as part of this project. This tool allows the modelling of any type of pipeline topology and also the modeling of various ADC building-blocks in order to estimate their respective error contributions (static, dynamic and noise). This software was developed in C++ language since encoded in MATLAB language the tool became too slow for demonstrating an histogram-based BISC technique (in which many samples are required)..

This C++ tool was intensively used to double-check, in software whether the proposed calibration technique worked properly in all worst-case conditions or not (an exhaustive Monte-Carlo analysis was carried out). It helped also defining all the required specifications for the different building-blocks (amplifiers, comparators, etc) used in the ADC as well as the analogue circuitry required to assist calibration.

5.3 Analog BISC Implementation

The on-chip Analog BISC includes a WGN generator followed by a 16-bit sub-binary PGA. The new on-chip WNG circuit consists of a 3-stage nested-Miller compensated OTA, where the first two stages rely on NMOS differential-pairs loaded by PMOS cascoded current sources, followed by two enhanced voltage-followers (EVF) that drive the PGA. The thermal noise of the large input resistors (R_n) is amplified by a high closed-loop gain. To remove accumulated offset and $1/f$ noise, the 3-stages are AC coupled. Dedicated active continuous-time common-mode feedback (CMFB) circuits are used in each amplifying stage.

Since the noise standard-deviation ($\sigma \cong 42$ mV) is PVT dependent, an SC 16-bit sub-binary PGA adjusts the σ to half the differential reference voltage ($\cong 250$ mV) with 10-bit accuracy. The average programming step was set to 1.7 (sub-binary), which ensures convergence of a successive-approximation algorithm (SAA) when adjusting the noise amplitude.

5.4 Digital BISC Algorithm Implementation

The Digital BISC Algorithm digital signal processing part consists of Control Unit, Histogram Generator and Calibration Logic blocks. A high-level block diagram of the controller is shown below.

In calibration mode a histogram is built using the samples produced by the ADC when fed with a White Gaussian Noise analogue signal. The histogram is read by the Control Unit, which executes the BISC algorithm and computes the calibration codes, which are written back to the Calibration Logic block. The Control Unit has a Debug Interface that will be used for debug and validation purposes in the FPGA prototype.

For flexibility testing purposes, the digital calibration circuitry has been completely implemented using a Virtex-5 FPGA. Notice that the FPGA was required to operate, at least, at 80 MHz to enable real time (on the fly) silicon verification in conjunction with the ADC chip. Since the digital circuitry is relatively small, one of the smallest FPGAs of this family (e.g. a Virtex 5) could have been used. The hardware synthesis has also been performed for a Xilinx Spartan 3 FPGA, but it was not able to meet the 80 MHz speed-of-operation requirement.

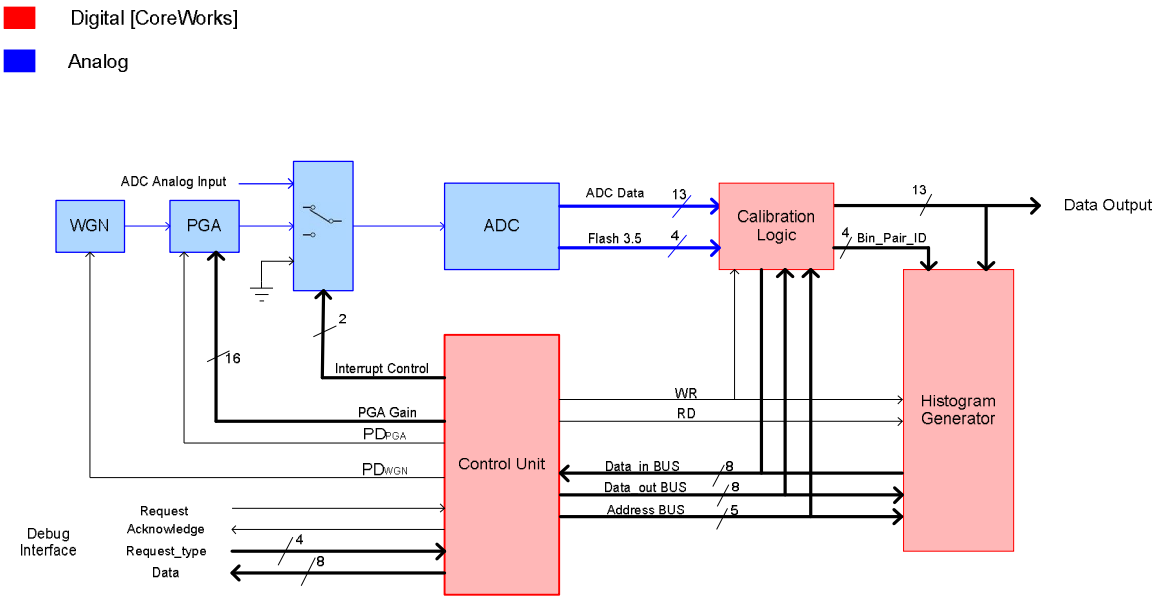

Figure 2. System overview showing details on the Digital BISC Algorithm.

5.5 Radiation Hardening by Design Techniques Employed

In the table below we summarize the radiation effects considered in this project, their effects in the circuits and the hardening methods we have employed in the design. It should be noted that this was the first time that S3 Portugal investigated, devised and implemented radiation hardening by design techniques in IC design.

Table 4: Summary of radiation hardening by design techniques.

	Specification	Effect in the circuit	Hardening by Design Techniques Employed
TID	100krad Max. (Phase 1) 1000krad Max. (Phase 2)	V_T change	• Effect diminished has process geometries are reduced. Should not be very critical in 90nm technology. • Use high-Vt NMOS and standard-Vt PMOS devices. • Design transistors with a lower V_{Dsat} voltage to improve robustness to Vt variations. • Calibrate the ADC offset.
TID	100krad Max. (Phase 1) 1000krad Max. (Phase 2)	Parasitic leakage current	• Use P+ guard rings to separate different circuit in the layout. • Use enclosed layout transistors specially designed for this project by S3 Portugal.
SEL	70MeV.mg-^{1}.cm^{2}	Circuit latch-up	• Use large P+ guard rings to separate NMOS and PMOS transistors. • Use large N+ guard rings inside NWELLS.

We have designed enclosed transistors in TSMC CLN90LP by developing a PCELL (parameterized cell) that can be sized individually.

The layout of this PCELL, for the case of the smallest transistor size (W=0.425 um and L=0.1um, with two fingers) is shown next. The dimensions depicted in this figure are the result of discussions held with IMEC and TSMC. The layout follows DFM rules, the size of the cell depends on the transistor size (channel width and channel length), except for the other dimensions shown in the figure, which are constant.

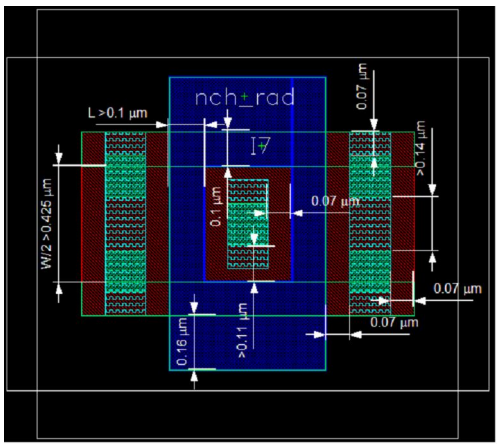

Figure 3. Enclosed-layout transistor PCELL designed by S3.

This layout structure produces a DRC violation because it is not possible to have bent transistor gates (rule PO.R1). The transistor gate is defined by the poly and thin oxide layers (OD).

This new transistor structure was presented to TSMC in order to verify if the DRC violation was an impediment of using this type of layout and TSMC stated that the DRC violation could be waived and recommended that DFM rules should be used in the transistor.

We also needed to develop a new set of rules for the LVS deck and extraction deck files, so that the LVS tool could identify this layout as a transistor and match it to the corresponding transistor in the schematic.

Furthermore, this type of transistor has an extra gate capacitance that must be added to the normal gate capacitance and we implemented an electrical model to take this effect into account.

Enclosed layout transistors were implemented in certain key locations ADC where leakage current through the transistors can affect negatively circuit performance, namely:

- reset switches inside each MDAC circuit,
- Reset switches inside each comparator circuit,
- the power down switches,
- the NMOS transistor in the logic circuits.

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Obviously, the layout using enclosed transistors results in significantly larger circuits. For example, one radiation hard D type flip-flop used many times in the ADC circuit occupies as much as 2.6 times the die area occupied by a standard structure, as shown in the figure below. Consequently, the power dissipation also increases.

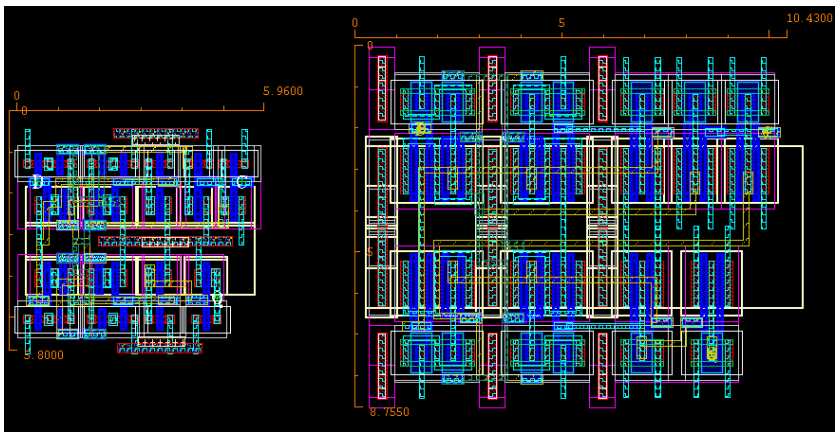

Figure 4. Regular D type flip-flop (on the left) and radiation hard D type flip-flop (on the right) designed in this project.

5.6 Key ADC Design Results (prior to chip implementation)

The ADC amplifiers were optimized using S3's proprietary optimization tool. A key input to the system is a file containing all relevant process technology parameters which are specific to the chosen fabrication technology (TSMC 90nm LP).

The amplifier optimization was performed considering 17 different design corners simultaneously by taking into account the following key opamp features: low frequency gain, product gain-bandwidth, output swing, slew-rate and settling time, excess noise factor and gate area.

The following table summarizes the final optimization results for the 13-bit 80MS/s ADC. Both the typical and worst power/noise conditions are presented.

Table 5: Summary of radiation hardening by design techniques.

	Worst Power & Noise	Typical conditions	Units
ADC Thermal noise	106	84	μVrms
ADC Power dissipation	145	116	mW
ADC 3σ DNL	1.0	0.7	LSB
ADC total capacitance	82 / 99	90	pF
SNR	68.7	70.1	dB
SINAD	68.4	69.9	dB
ENOB	11.1	11.3	bit

The following table summarizes the impact of the BISC calibration system in the main specifications of the ADC.

Table 6: Summary of radiation hardening by design techniques.

	Typical Conditions without Calibration	Typical Conditions with Calibration	Units
SNR	70.1	70.1	dB
THD	−68	−82	dB
ADC 3σ DNL	1.5	0.7	LSB
SINAD	65.9	69.9	dB
ENOB	10.7	11.3	bit

6 Chip Implementation

6.1 Full-chip Overview

A total of 10 I/O cells for analog VDD and 10 I/O cells for analog VSS are used to minimize the RI drop due to the maximum 110mA analog current. A total of 21 I/O cells are used exclusively to interconnect the ADC and analog BISC with the digital BISC external block. The I/O ring was fully verified by simulation as well as included into full-chip DRC and LVS checks.
An extra WGN was included for stand-alone test purposes.

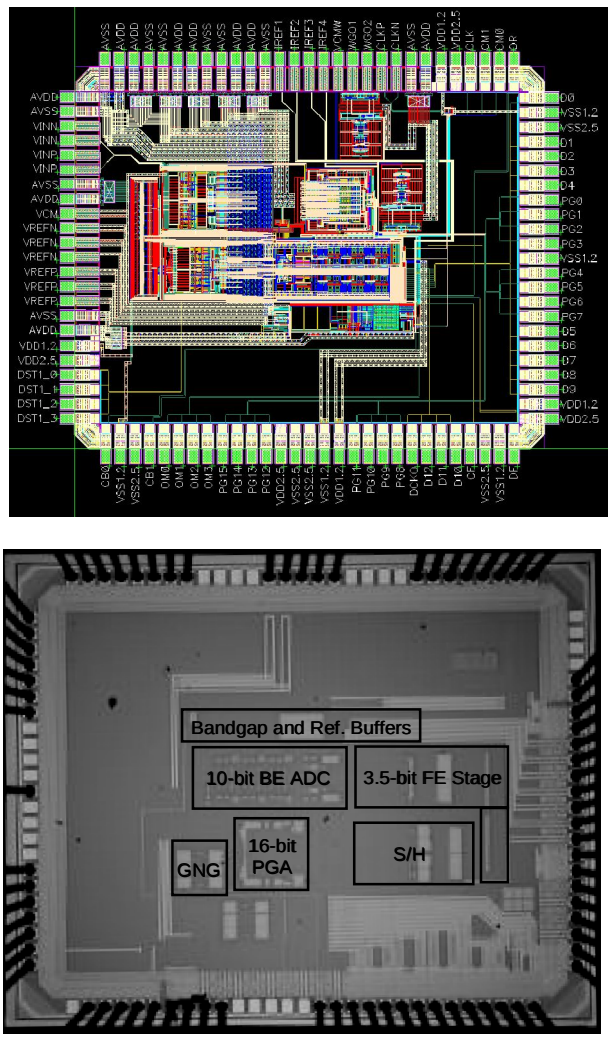

Figure 5. Plot of the test chip with full PAD ring and die photo of the test chip (all analog blocks are implemented on-chip as well as the digital synchronization and correction logic).

6.2 Chip Core Overview

The figure below depicts the ADC, WGN and PGA layout. The ADC core die area is 0.88mm^2, or 41% below specification of 1.5mm^2. This includes auxiliary circuits. The analogue BISC die area is 0.28mm^2, or 7% below specification of 0.3mm^2. The complete die area is 1.28mm^2 or 29% below specification.

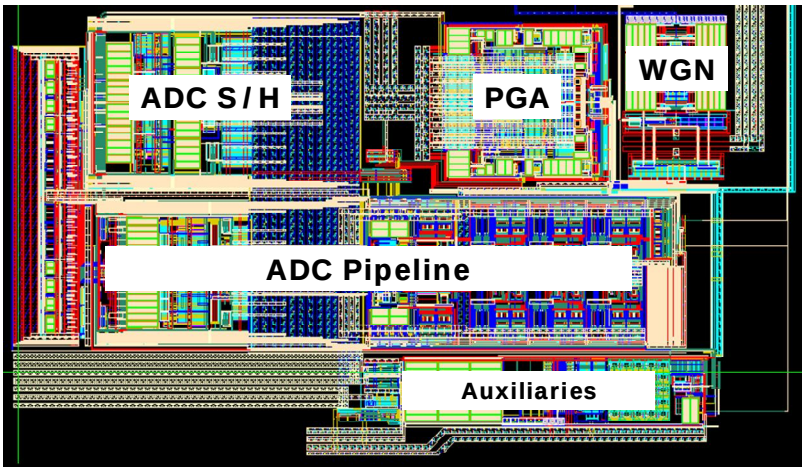

Figure 6. Chip core layout overview.

6.3 Chip Fabrication Details

The chips were fabricated by TSMC and taped-out to TSMC by IMEC who is a TSMC certified Design Center in Europe.

Shuttle Tape-Out Month: October 2007, taped-out via IMEC.

Technology: TSMC 90nm MS/RF Low Power 1P9M 1.2V-2.5V Cu Low-k CMN90LP-1.2-2.5-CU-LK

Analog Options: No

Test Chip TM number: TMT530_C18

TSMC Lot ID: P61486.00#2

7 Prototype Implementation

7.1 Prototype Implementation Phase 1

In Phase 1, three different chip assembly types have been employed:

1) 64L CQFP package with open lead for radiation tests by TRAD (stand-alone ADC).
2) 80L TQFP package with Exposed Pad for ground connection for full performance evaluation at S3 Portugal labs (complete ADC with BISC analog circuits). During performance tests with this testing platform we realized that the bounding wire inductances were affecting the ADC performance above 40MS/s. It was then decided to implement a second testing platform based on chip-on-board (CoB) assembly. The test results improved significantly at 80MS/s.
3) CoB assembly for full performance evaluation at S3 Portugal labs.

Coreworks implemented an FPGA board and synthesized the BISC algorithm using a Xilinx Virtex-5 FPGA operating up to 100MHz.

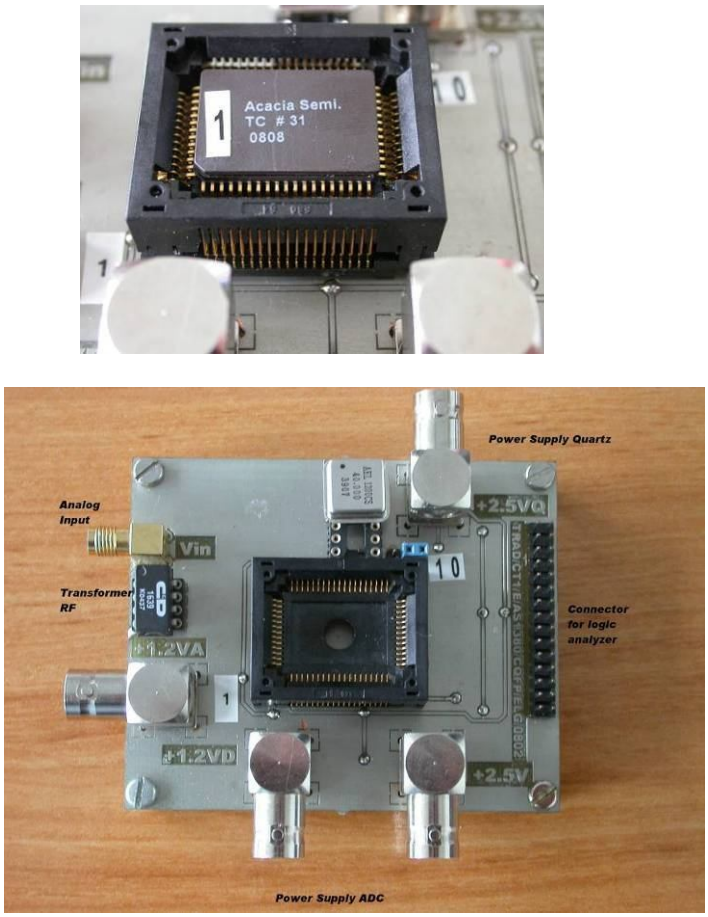

Figure 7. 64L CQFP Package & PCB board for radiation tests by TRAD (PCB designed by TRAD).

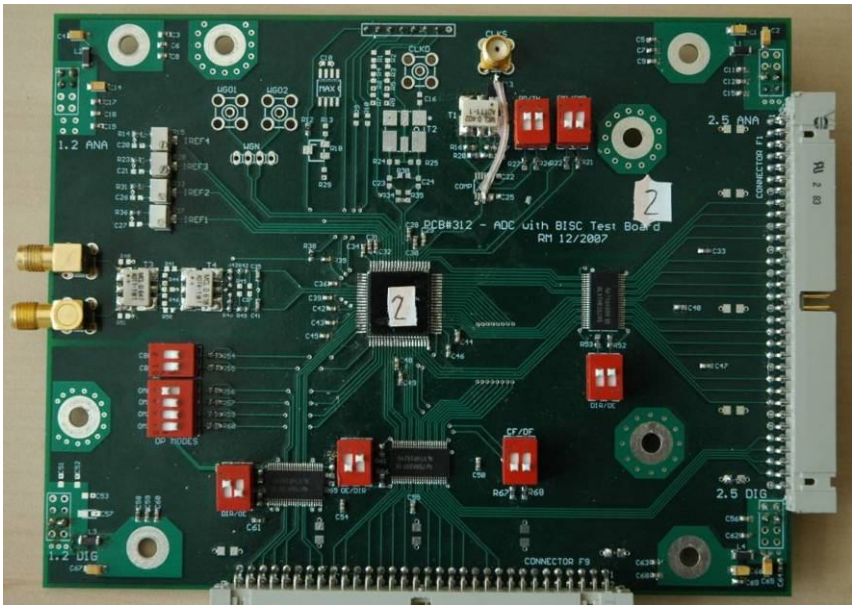

Figure 8. PCB for 80L TQFP Package for full performance evaluation at S3 Portugal labs.

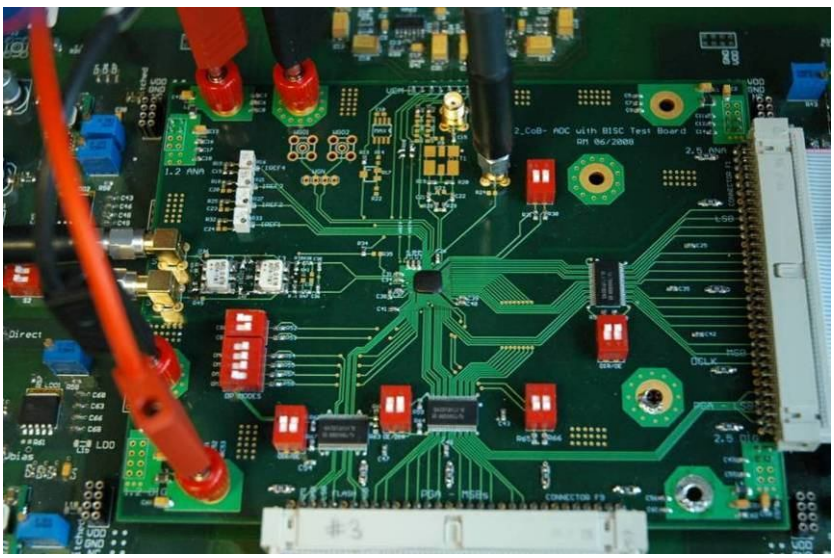

Figure 9. CoB assembly & PCB board for full performance evaluation at S3 Portugal labs.

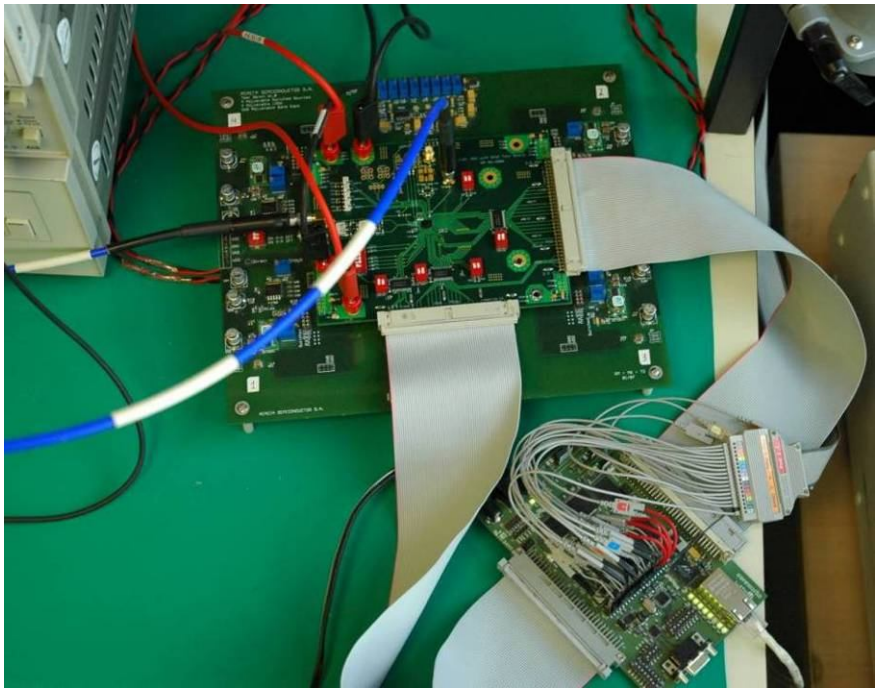

Figure 10. PCB with CoB assembly and FPGA board.

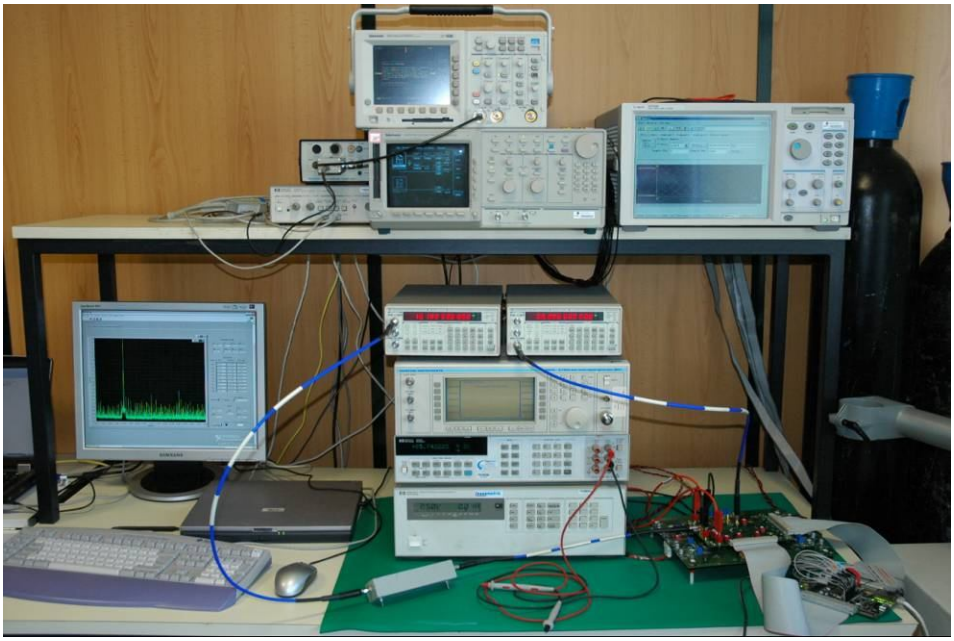

Figure 11. S3 Portugal test bench.

7.2 Prototype Implementation Phase 2

In Phase 2 of the project, S3 Portugal devised a new testing infrastructure platform to enable high-performance ADC tests during radiation testing by TRAD. This new testing platform is based on chip-on-board assembly and uses a Mother Board and multiple Daughter Boards.

Figure 12. CoB assembly & PCB board for Daughter Board.

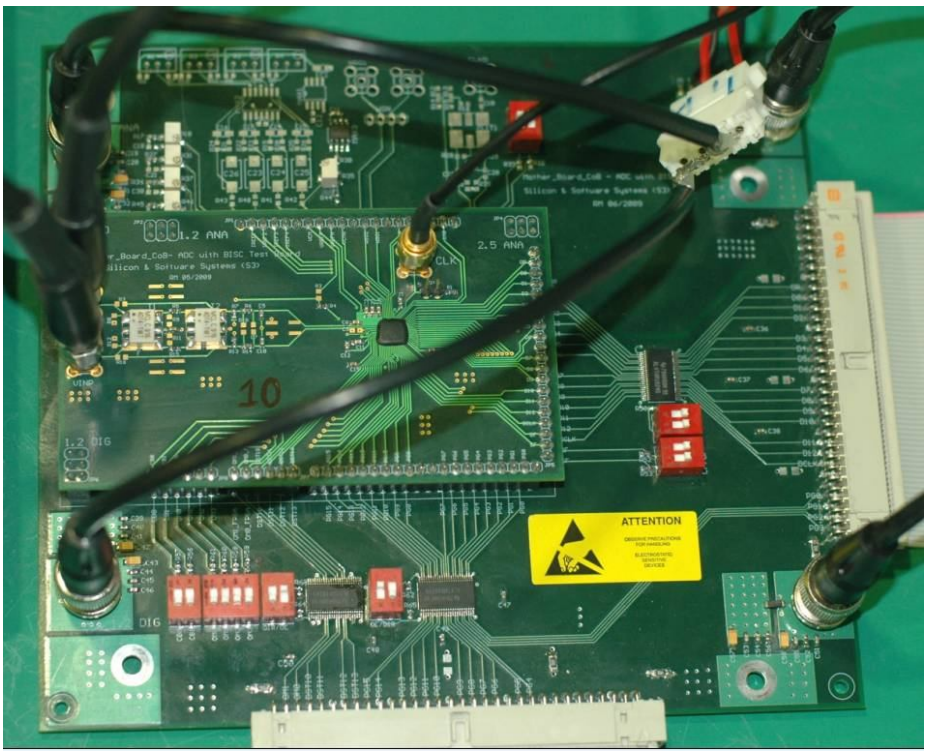

Figure 13. Daughter and Mother Board plug-in system.

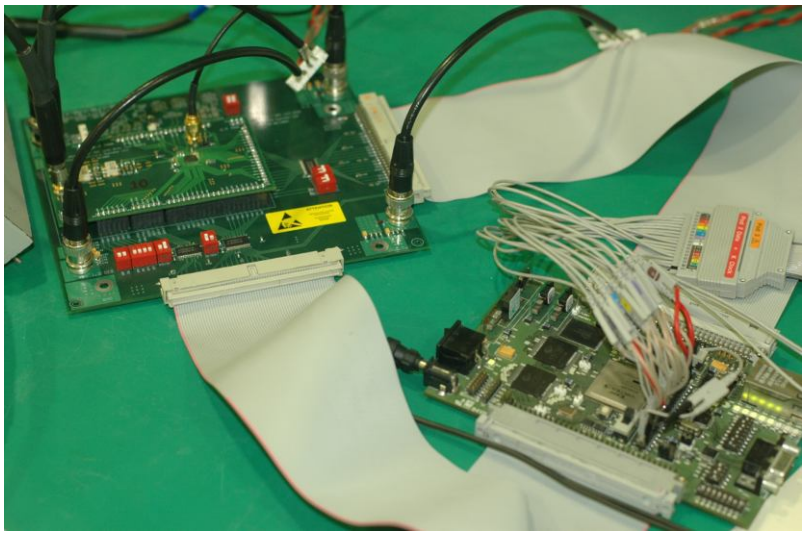

Figure 14. Mother Board, Daughter Board and FPGA board.

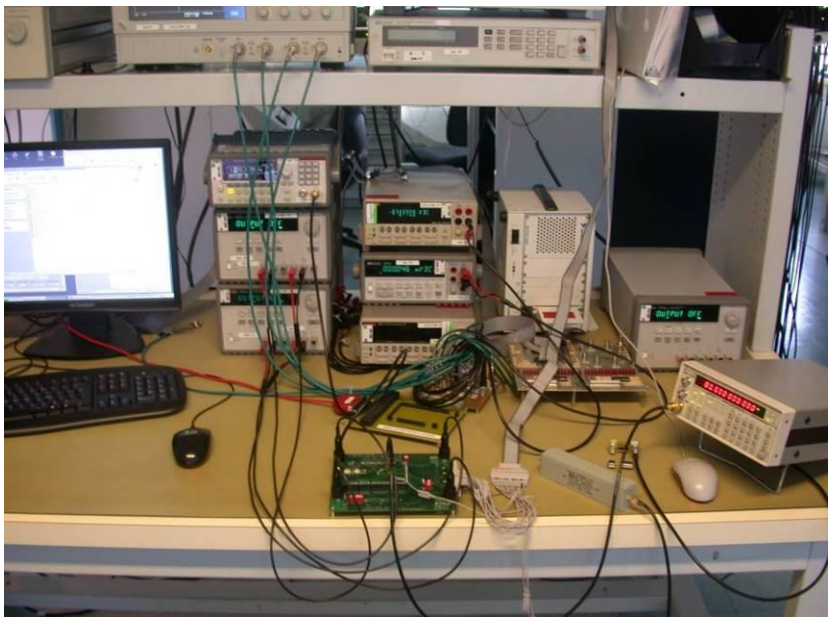

Figure 15. TRAD test bench.

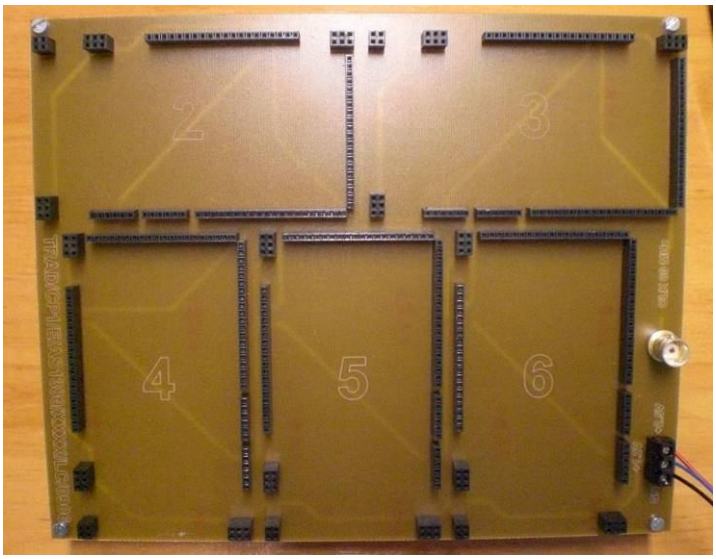

Figure 16. TRAD board designed to contain 5 Daughter Boards for biasing and irradiation.

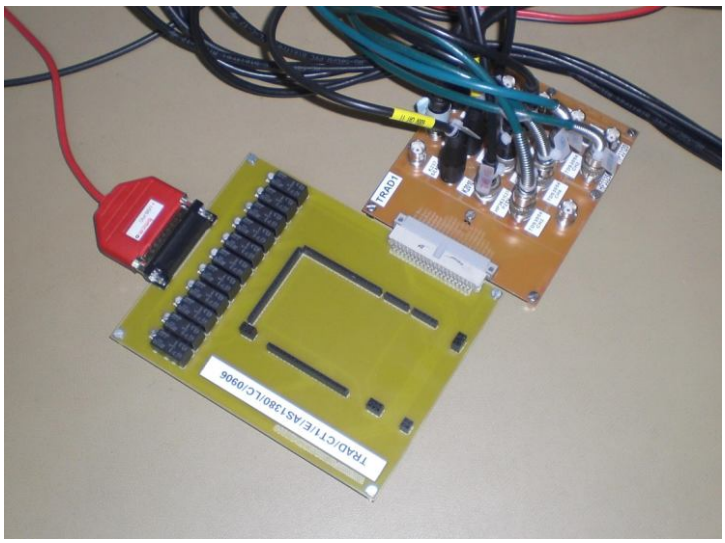

Figure 17. TRAD static testing board system (Mother Board Type 2).

8 Prototype Validation

8.1 ADC System Performance Evaluation by S3 Portugal (Phase 1 and Phase 2)

In both validation phases we performed extensive measurements considering multiple packaged and chip-on-board samples, supply voltage variations, temperature variations, results before calibration, results after calibration, among others. This resulted for both phases in detailed test reports with over 70 pages each.

In this Summary Report we only give illustrative and concise examples.

This section illustrates key measurements performed by S3 Portugal using the chip-on-board testing platform (as used in Phase 1 and Phase 2).

8.1.1 Tests of the WGN Block

The 13-bit ADC was used to digitalize the WGN noise at an 80 MS/s sampling rate and at the nominal power supply voltage. The PGA gain was set to the minimum (approximately 4) and 20.8 million samples were collected at the outputs of the ADC. After computing the histogram, as depicted right after, and performing statistical analysis, the relevant measured noise performance parameters are summarized below. Notice that both, the asymmetry and kurtosis coefficients are very close to the expected ideal values (zero). Any spikes/holes that appear in the histogram are mainly due to the gain-error and non-linearity errors of the 3.5-bit front-end stage and, their information contents, suffices for extracting all calibrating-codes.

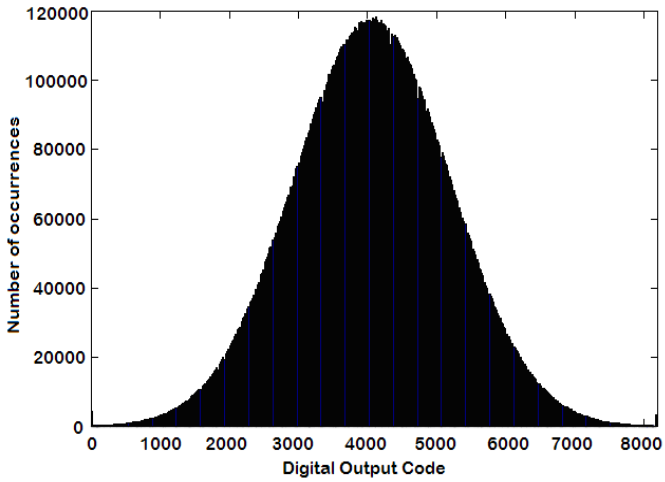

Figure 18. Measured digitized histogram of the output of the WGN.

Table 7 : MEASURED PERFORMANCE SUMARY OF THE WGN BLOCK.

Parameter	Measured Results	
	Fs = 80 MS/s	Unit
Mean	4148.0	LSB
Offset	52.0	LSB
Standard-deviation, σ	1052.0	LSB
Asymmetry coefficient	0.0000516	-
Kurtosis coefficient	-0.0018050	-

8.1.2 Tests of the ADC with and without Calibration

The next figure displays one example of the measured DNL/INL plots before and after calibration and for F_S = 80 MS/s. As it can be observed, calibration improves both characteristics and, after calibration, INL is always bounded to ±1.5 LSB. This limit is mainly imposed by the second stage in the pipelined chain (that corresponds to the first stage of the 10-bit back-end ADC) which has a 1.5-bit resolution and it is not calibrated.

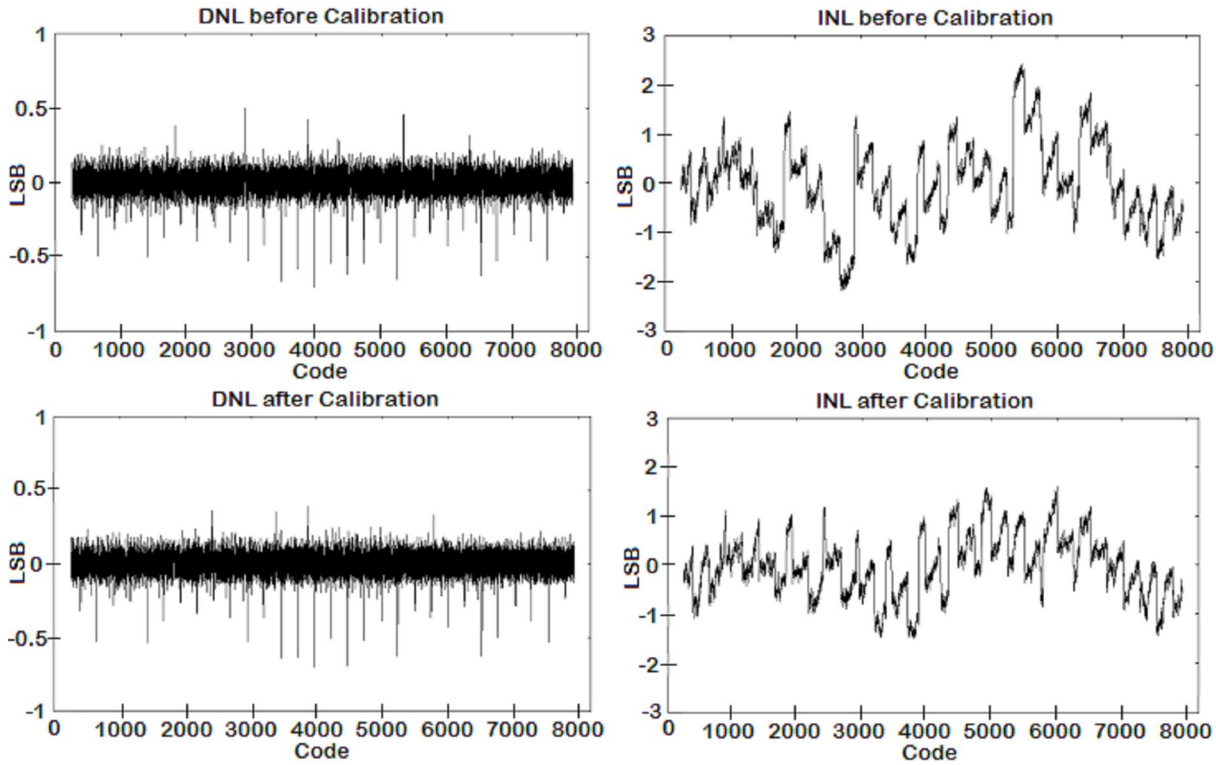

Figure 19. Measured DNL and INL errors before and after calibration.

The figure below displays a measured FFT for a 10 MHz input signal frequency (f_{in}) and 80 MS/s sampling frequency (F_S) before and after calibration. SFDR (mainly dominated by HD3) is improved by 10 dB to 74.6 dB and THD is improved by 8.4 dB to -72.7 dB.

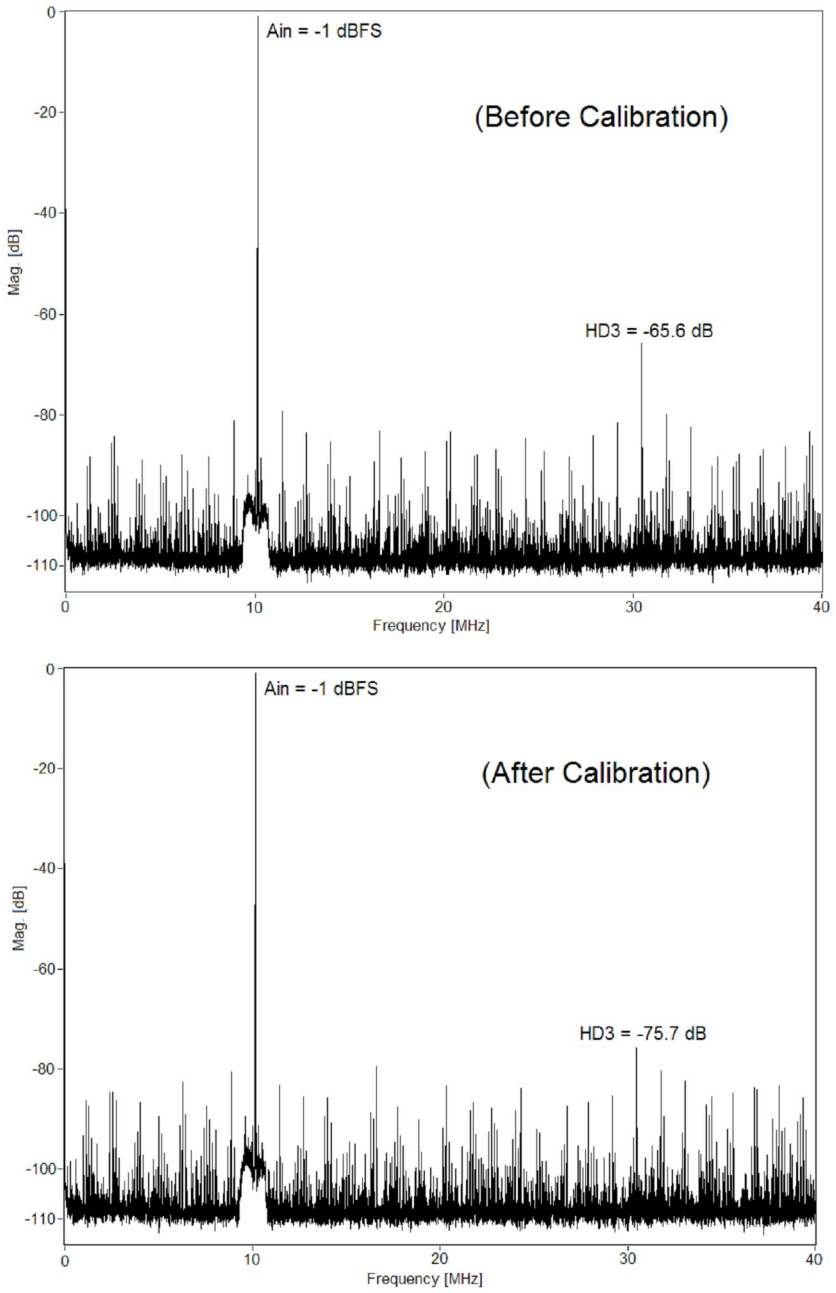

Figure 20. Measured FFT results for f_{in} = 10 MHz (@-1dBFS) and F_S = 80 MS/s before and after calibration.

The figure below shows how measured SFDR, SNDR and THD are significantly improved after calibration for different values of f_{in} and F_S. The largest improvements, corresponding to over 14.8 dB in SFDR (to 81 dB) and 13.8 dB in THD (to -79.7 dB), are obtained at 40 MS/s. The SFDR and THD degradation measured for f_{in} signals below 10 MHz is mainly due to the even harmonics from the single-ended-to-differential conversion on the testing PCB which relied on a cascaded of two RF transformers, with poor low-frequency performance together with the input passive matching network optimized for f_{in} >10 MHz.

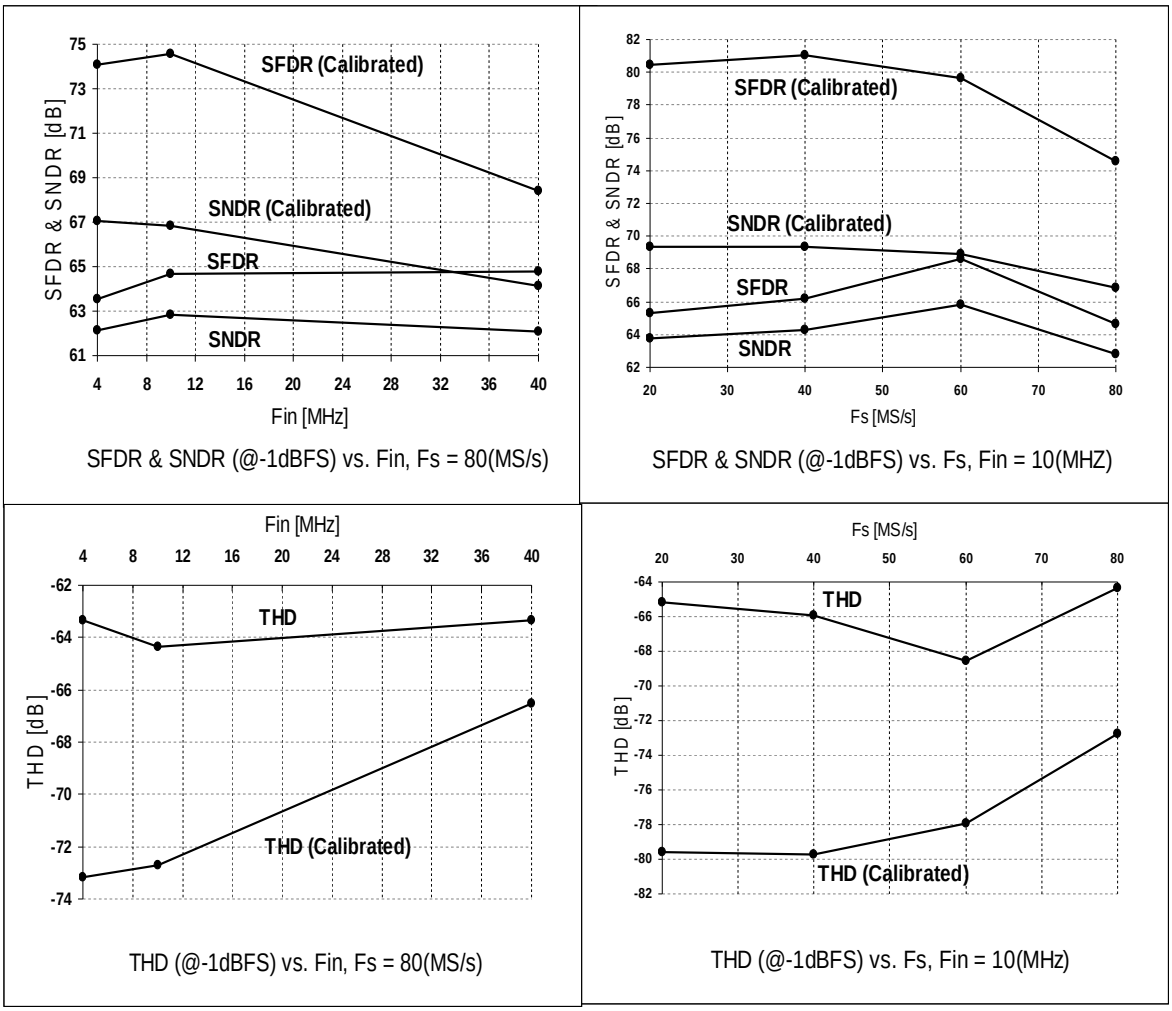

Figure 21. Measured SFDR, SNDR and THD for different input signal frequencies (f_{in}) and different sampling frequencies (F_S) before and after calibration.

8.2 Radiation Tests by TRAD

8.2.1 Phase 1 Results

During Phase 1, TRAD conducted two radiations tests: SEL and TID.

For the SEL tests, 3 delidded samples were irradiated. No SEL was observed during this test under a Xenon irradiation (LET = 69.99 MeV.cm²/mg) with a total fluence equal to 1E+7 #/cm².

For the TID tests, 5 samples were irradiated with a ^{60}Co source in the following steps up to 100krad: 12, 19, 41, 53,66 and 100krad. Annealing was considered with 24h at 25ºC and 168h at 100ºC. One sample was used as a reference (not irradiated). The resulted showed similar performance for all dose levels. However, both package and test set-ups limited the ADC conversion rate to 40MS/s and the effective resolution to only 8.0-bit ENOB, as depicted below.

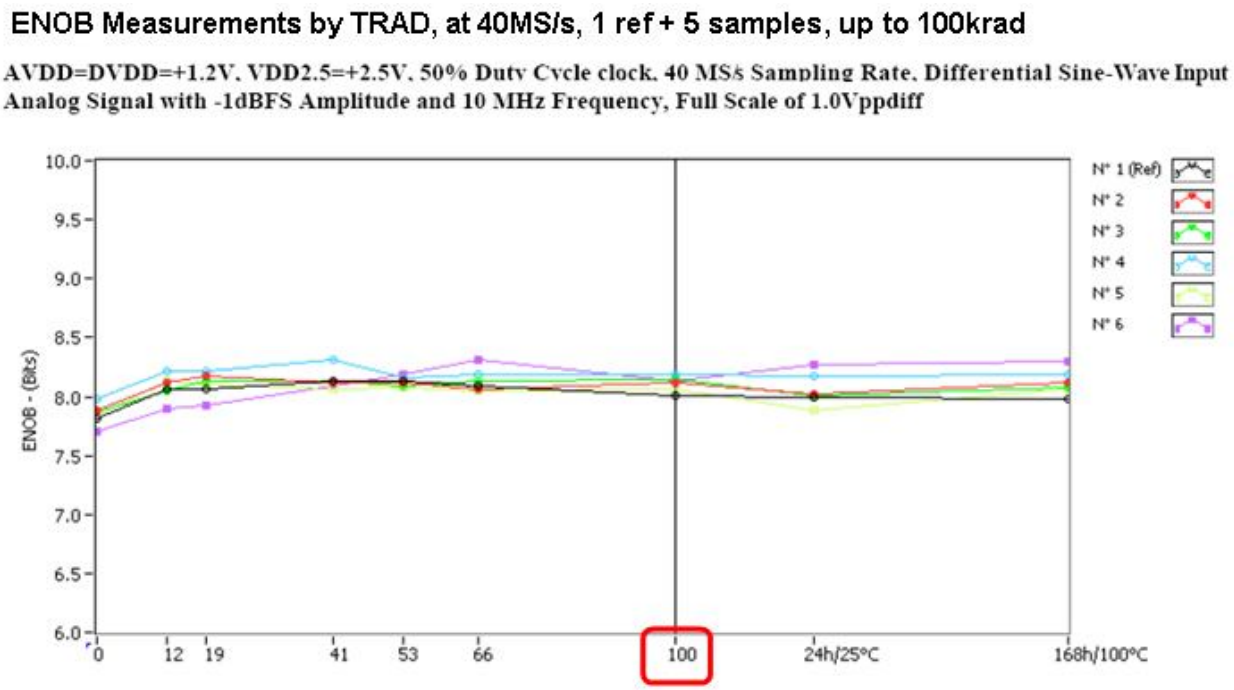

Figure 22. One example of TRAD performance testing – ENOB in Phase 1, limited to 40MS/s and to 8-bit ENOB, up to 100krad.

8.2.2 Phase 2 Results

During Phase 2, TRAD conducted TID radiation tests only.

For the TID tests, 5 Daughter Boards with chip-on-board assembly were irradiated with a ^{60}Co source in the following steps up to 1076krad: 66, 106, 276, 342, 500, 745 and 1076krad. Annealing was considered with 24h at 25ºC and 168h at 100ºC. One sample was used as a reference (not irradiated). The resulted showed a greatly improved performance versus the results from Phase 1, thereby proving that the new testing platform was indeed a very good strategy to adopt.

ADC static performance (DNL, INL) and ADC dynamic performance of between 10.0 and 10.25-bit ENOB were maintained over the entire extended TID dose up to 1076krad, as shown in the next figure for the particular case of ENOB performance. These results also show how good and robust against TID effects both the TSMC 90nm process and the design techniques developed by S3 Portugal are.

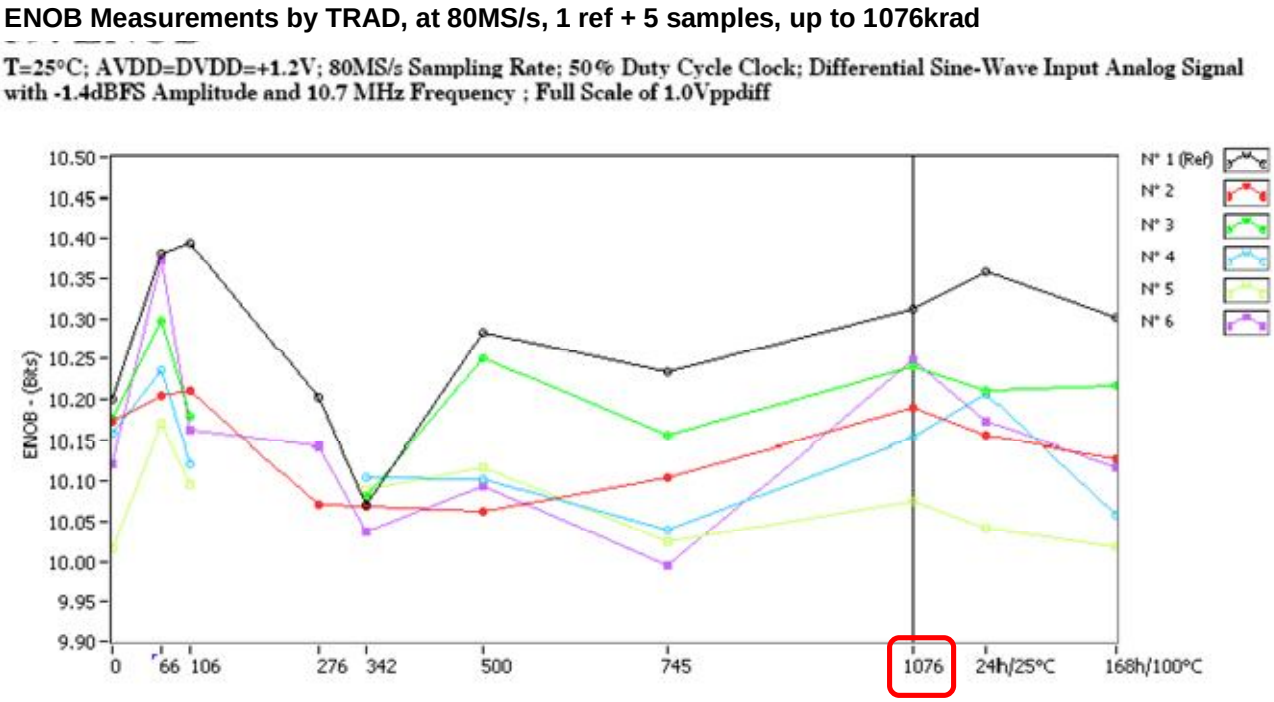

Figure 23. One Example of TRAD performance testing – ENOB in Phase 2, at 40MS/s, up to 1076krad and showing above to 10-bit ENOB.

8.3 Measured Performance versus Target Specifications

Table 8: Summary of Key Technical Objectives for the ADC technology.

Parameter	Target Specification	Measured Specification	Comments
General Specifications			
Resolution	13-bit	13-bit	Achieved.
Sampling Rate	80MS/s	80MS/s	Achieved. Also operates efficiently at 40MS/s.
Supply Voltage	1.2V ±10%	1.2V ±10%	Achieved.
Junction Operating Temperature	-40ºC to +125ºC	-40ºC to +125ºC	Achieved.
Die Area ADC Core	< 1.5mm^2	0.88mm^2	Over-achieved. Actual die area 41% below target.
Die Area Analog BISC	< 0.3mm^2	0.28mm^2	Achieved.
Radiation Specifications			
Total Ionizing Dose (TID)	100krad	1076krad	Better than 10x versus spec.
Single-Event Latch-up (SEL)	70 MeV.mg^{-1}.cm^2	70 MeV.mg^{-1}.cm^2	Achieved.
Static Performance			
Differential Non-Linearity Error	±1.5LSB	<±1LSB	Achieved < ±1 LSB even without calibration at 40MS/s and 80MS/s.
Integral Non-Linearity Error Before Calibration	-	<±3LSB	
Integral Non-Linearity Error After Calibration	±1.5LSB	±1.5LSB	Achieved after calibration.
Dynamic Performance			
Signal to Noise Ratio (SNR) At 40MS/s	70dB	68dB	See Note 1 below for more details
Signal to Noise Ratio (SNR) At 80MS/s	70dB	66dB	3 to 4dB less, depending on the sample chosen. See Comment 1 below for more details.
Total Harmonic Distortion (THD) – Before to Calibration	-	-68dB	
Total Harmonic Distortion (THD) – After Calibration	-72dB	-75dB	
Effective Number of Bits (ENOB) Before Calibration at 40MS/s	11.0	10.8	Less then 0.2-bit difference. Determined by lower SNR, see Comment 1.
Effective Number of Bits (ENOB) Before Calibration at 80MS/s	11.0	10.2	Determined by lower SNR, see Note 1 and by THD before calibration.
Effective Number of Bits (ENOB) After Calibration at 80MS/s	11.0	10.8	Determined by lower SNR, see Note 1. THD is corrected by calibration.
Power Dissipation at 40MS/s	-	50mW	Typical.
Power Dissipation at 80MS/s	116mW	93mW	Typical, -20% below spec. See Comment 2
Calibration Time at 80MS/s	TBD	27s	

Comment 1:

The measured SNR differs from the specified value by -2dB at 40MS/s and -4dB at 80MS/s. Notice that this degradation, which has a direct impact of about half bit in the measured ENOB, is explained by 3 factors:

1. Large test-board and chip substrate noise generated by the switching in the 13 output digital drivers buffers (supplied with 2.5V) in the output digital PADs, which becomes more significant at 80MS/s compared with 40MS/s.
2. The amount of noise from the input signal source that passes through the ±5 % bandwidth around 10.7MHz in the 7th.-order passive band pass filter (BPF) used between the analog signal generator and the ADC test board.
3. The jitter noise from the external clock-driver that was estimated (by measurements) to be around 3ps-rms when the maximum specified value was 2ps-rms.

To overcome effect 1), which is the most critical as we can see from the noise increase from 40MS/s to 80MS/s operation, the best strategy is to include a on-chip RAM in the test chip that will read and store the several million ADC samples at full-speed (80MS/s) and then transmit the digital codes to the acquisition equipment at a much lower speed (e.g. below 1MS/s). In this manner there is virtually no noise associated with the output digital drivers and ADC SNR performance will be optimized.

To overcome effect 2) and 3), a very highe-performance signal source and very high-performance clock generator should be used, respectively, but these are extremely expensive (above €30,000 in cost for each).

Comment 2:

Corresponds to an energy efficiency below 0.6pJ per conversion step excluding references. Would be equivalent to 0.5pJ if SNR was 70dB and was not limited by the aspects discussed above.

9 Technical Publications that Resulted from the Project

This work included significant R&D activities in the field of ADC design as well as radiation hardening design techniques.

We have published one paper and gave one invited talk, as follows:

> "Design and Testing of a Radiation Hardened 13-bit 80 MS/s Pipeline ADC Implemented in a 90nm Standard CMOS Process"; paper presented by N. Paulino at AMICSA'08;
>
> "Digitally Enhancing Dynamic Linearity in High-Resolution A/D Converters", invited talk presented at NMI Event, Dublin, 22nd. October 2009.

We have also written an extended paper to be submitted soon to an IEEE Journal:

> "Self-Calibration of a 13-bit 80 MS/s CMOS Pipeline ADC using On-Chip Thermal Noise"; ready for submission to an IEEE Journal (but not submitted yet);

10 Evaluation of Technology

We have prepared marketing material that we have been presenting and delivering to customers.

This includes:

- Product brief.
- Full datasheet.
- Silicon Characterization Report.
- Silicon Quality Reports.
- Evaluation Kit User Guide.
- Evaluation Kit.

We have contacted customers for space and non-space related applications resulting in 5 customer leads for space applications and 7 customer leads for non-space applications. These activities resulted in two design wins for non-space applications, both based on modifications performed on the 13-bit 80MS/s ADC implemented as part of this project.

During Phase 1 of the project, we essentially discussed and presented to potential customers based on the performance of the ADC as validated by S3 Portugal, not so much on the radiation test results due to the various test limitations experienced in Phase 1.

In Phase 2 of the project which was just completed now in November 2009, TID radiation tests proved very successful due to the improved testing infrastructure. The ADC was fully functional up to the newly specified 1076krad (a dose ten times higher versus Phase 1) and the dynamic performance exceeded 10-bit ENOB at 80MS/s over all TID dose steps. Now that we have achieved outstanding radiation test results, we will start presenting these results to space-related companies.