High Resolution 1kHz ΣΔ DAC for Space Applications

Brief datasheet

V1.0

DAC24BISDA

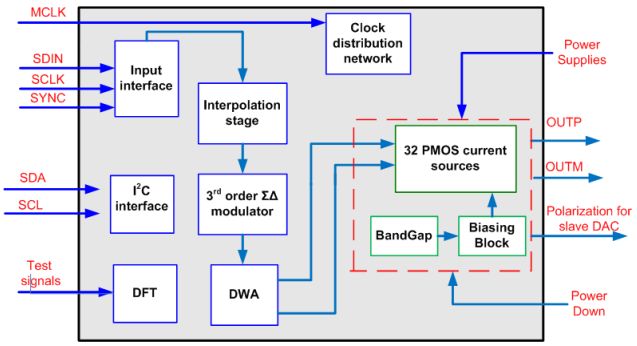
FEATURES

- **24-bit DAC including two DAC cells (main and redundant)**
- **Differential current output**
- **Internal or external reference current setting**
- **Synchronous serial input data format**
- **SYNC input**
- **Configuration via I²C interface**
- **1.2V digital power supply**
- **3.3V analog power supply**
- **<70mW power consumption**
- **Sampling frequency 6 or 12kHz**
- **Bandwidth 0.1mHz to 1kHz**
- **Oversampling ratio X256 or X128**
- **Multi-bit Sigma-Delta modulator**
- **Radiation hardened design**
- **Requires external analog post filter**

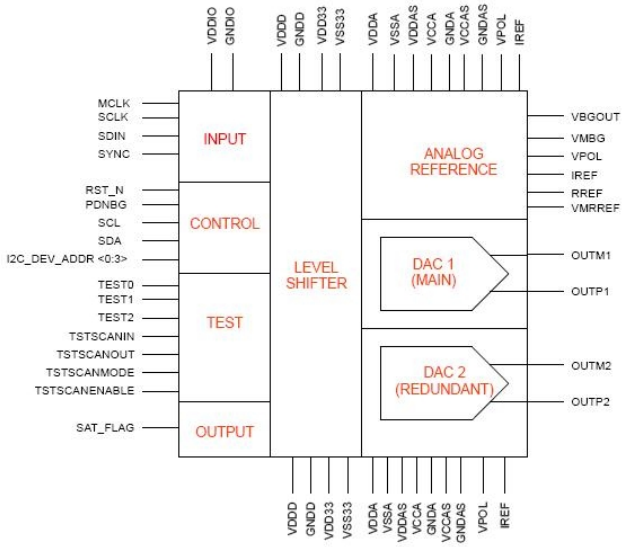
TARGET APPLICATION

- **High-accuracy instrumentation and actuator drive for systems operating in space**

FUNCTIONAL BLOCK DIAGRAM



FLOORPLAN OVERVIEW



DESCRIPTION

This Digital-to-Analog converter is a low-noise, low frequency, radiation hardened device operating at a sampling frequency of 6 or 12kHz, while it is optimized to operate in a bandwidth of 0.1mHz to 1kHz. The DAC receives a 24-bit input data in a synchronous serial format and converts it into a differential current analog output signal.

The converter uses a third-order multi-bit Sigma-Delta (ΣΔ) modulator that provides superior noise and linearity performance. The interpolator follows a multiple-stage architecture and consists of an FIR equiripple LPF followed by two cascaded stages of Half-band equiripple filters, while the last stage is a programmable SINC filter which provides variable interpolation ratios. The oversampling ratio is selectable between 256 and 128.

The synchronization input (SYNC) can be used to synchronize the conversions of multiple DAC devices and the conversion process is accomplished in respect to an externally provided master clock signal (MCLK). The DAC includes various registers for configuration and operating mode selection which are accessed through a standard I²C interface.

The analog part includes two identical DAC cells which are driven by the same input data, but can be powered down independently and a reference block. Each DAC cell consists of a matrix of 32 current sources , which are synchronously controlled by a 32 bit signal arriving from the digital part. The elementary current sources are selected in a cycled fashion by the preceding Data Weighted Algorithm (DWA) block, which exists in the digital part. The aim of the DWA block is to shape the noise created by the mismatch between the elementary current source cells and this is accomplished by the data rotation algorithm.

The reference block consists of bandgap cell and a low noise operational amplifier which generates and regulates the DC reference current value. An additional RC filtering stage before the low noise amplifier is used to enhance the noise performance of the voltage reference block. The reference current can be fixed internally, or by connecting an external resistor to the dedicated RREF pad. A DAC operating as a master can be used to polarize other devices connected as slaves.

The device employs a variety of radiation hardening strategies such as triple-mode redundancy in the critical digital blocks, usage of radiation tolerant standard cells and techniques at layout level.

NOTE

This document is a brief datasheet of the DAC24BISDA Digital-to-Analog Converter. The information provided hereafter reflects the specifications and characteristics of the device at the time of tape-out.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDD33/VDDA/VDDAS/ VCCAS/VCCA	Analog Power Supply	4 (Max)	V
VDDD/VDDIO	Digital Power Supply	2 (Max)	V
VID	Digital Input Voltage	VDDD+0.5	V

ELECTRICAL SPECIFICATIONS

All specifications at T_A = 27ºC, VDDD = VDDIO = 1.2V, VDD33 = VDDA = VCCA = VDDAS = VCCAS = 3.3V, GNDD = GNDIO = VSS33 = VSSA = GNDA = GNDAS = 0V, MCLK = 1MHz, R_L = 10Ω, RREF = 219Ω, typical process parameters, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
VDDD/VDDIO	Digital power supply	1.08	1.2	1.32	V
GNDD/GNDIO	Digital power supply		0		V
I_D	Digital Supply Current		2		mA
VDD33/VDDA/VDDAS/ VCCAS/VCCA	Analog Power Supply	3.0	3.3	3.6	V
VSS33/VSSA/ GNDA/GNDAS	Analog Power Supply		0		V
I_A	Analog Supply[1] current (per DAC)		8.75		mA
I_o	Single-ended analog current output (per DAC)	12nA		5.83mA	
I_{com}	Common mode output current		2.915		mA
I_{cs}	LSB step current		182.2		uA
VBGOUT	Internal bandgap voltage		1.198		V
VPOL	Polarizing voltage		2.11		V
C_{in}	Input capacitance (input buffers)		0.7		pF
V_{IL}	Digital I/O low level input voltage			0.35*VDDD	V
V_{IH}	Digital I/O high level input voltage	0.65*VDDD			V
f_{MCLK}	Master clock frequency		1.536		MHz
f_s	Sampling frequency[2]		6 or 12		kHz
T_o	Functional Temperature	-55		125	°C
T_f	Temperature range for full performance	0		50	°C

NOTES

1) Digital input nodes must never float; they must always be driven by a low impedance source.

2) f_{MCLK} is equal to 256*f_s or 128*f_s (see note 2).

3) C_{in} corresponds only to the capacitance of the digital input buffer.

DIGITAL FILTER CHARACTERISTICS

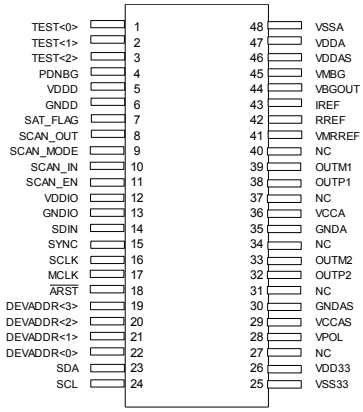
Filter type	Upsampling factor	Fs	Pass-band frequency	Stop-band frequency	Pass-band ripple	Stop-band attenuation	Filter order
FIR equiripple	2	12 kHz	1.01 kHz	3 kHz	0.0001 dB	-130 dB	44
Half Band Filter	2	24 kHz	3 kHz	9 kHz	0.00001 dB	-130 dB	30
Half Band Filter	2	48 kHz	3 kHz	21 kHz	0.00001 dB	-130 dB	18

1 Specification with internal current reference or external current reference fixed by Rext = 220Ω. The analog current consumption can be reduced using a higher external resistor

2 The sampling frequency is 6 kHz when OSR = 256 and 12kHz when OSR = 128.

PIN ASSIGNMENTS

DAC24BISDA
48-Lead ceramic flat package (1)
(top view)



(1) This is a preliminary pin assignment. The final pin assignment will be defined upon the final package assembly and it may differ accordingly.

PIN DESCRIPTION

The 3.3V value following the entries in the 'VOLTAGE' column marked with an asterisk (*), is used to indicate that the particular pad belongs to the analog power domain. It does not represent the actual voltage value of that pad under normal operating conditions. The NC indication means no internal connection. However It is recommended to connect these pins to the analog ground (GNDA).

PIN #	NAME	TYPE	FUNCTION	VOLTAGE (V)	DESCRIPTION
1	TEST<0>	D	Input	1.2	Fixed current source mode select
2	TEST<1>	D	Input	1.2	Fixed current source mode select
3	TEST<2>	D	Input	1.2	Fixed current source mode select
4	PDNBG	D	Input	1.2	Analog bandgap power down
5	VDDD	Power	Digital supply	1.2	Digital core
6	GNDD	Ground	Digital supply	0	Digital core (also digital substrate connection)
7	SAT_FLAG	D	Output	1.2	DAC saturation flag
8	SCAN_OUT	D	Output	1.2	Scan chain output
9	SCAN_MODE	D	Input	1.2	Scan test mode select
10	SCAN_IN	D	Input	1.2	Scan chain input
11	SCAN_EN	D	Input	1.2	Scan test enable
12	VDDIO	Power	Digital supply	1.2	Digital I/O
13	GNDIO	Ground	Digital supply	0	Digital I/O
14	SDIN	D	Input	1.2	Serial Data Input for the data stream
15	SYNC	D	Input	1.2	Synchronization signal
16	SCLK	D	Input	1.2	Serial clock input derived from the MCLK
17	MCLK	D	Input	1.2	Master clock at 256*Fs
18	$\overline{\text{ARST}}$	D	Input	1.2	Asynchronous reset
19	DEVADDR<3>	D	Input	1.2	I2C device address setting bit
20	DEVADDR<2>	D	Input	1.2	I2C device address setting bit
21	DEVADDR<1>	D	Input	1.2	I2C device address setting bit
22	DEVADDR<0>	D	Input	1.2	I2C device address setting bit
23	SDA	D	I/O	3.3 (5V tolerant)	Serial data for I2C
24	SCL	D	Input	3.3 (5V tolerant)	Serial Clock for I2C
25	VSS33	Ground	Analog supply	0	Level shifter block (translator and clock cells)
26	VDD33	Power	Analog supply	3.3	Level shifter block (translator and clock cells)
27	NC				No internal connection.
28	VPOL	A	Output	3.3(*)	Voltage biasing for slave DAC
29	VCCAS	Power	Analog supply	3.3	Analog NISO polarization
30	GNDAS	Ground	Analog supply	0	Analog substrate connection
31	NC				No internal connection.
32	OUTP2	A	Output	3.3(*)	Redundant DAC differential analog output positive
33	OUTM2	A	Output	3.3(*)	Redundant DAC differential analog output negative
34	NC				No internal connection.
35	GNDA	Ground	Analog supply	0	Analog part (both DAC)
36	VCCA	Power	Analog supply	3.3	Analog part (both DAC)
37	NC				No internal connection.
38	OUTP1	A	Output	3.3(*)	Main DAC differential analog output positive
39	OUTM1	A	Output	3.3(*)	Main DAC differential analog output negative
40	NC				No internal connection.
41	VMRREF	Ground	Input	0	Ground internal resistor reference
42	RREF	A	Input	3.3(*)	Input current reference. Must be shorted with IREF pin to select the internal current reference.
43	IREF	A	Output	3.3(*)	Output of internal current reference. Can be used for slave DAC
44	VBGOUT	A	Output	3.3(*)	Output bandgap voltage
45	VMBG	Ground	Input	0	Ground bandgap voltage
46	VDDAS	Power	Analog supply	3.3	CS switch control block NISO polarization
47	VDDA	Power	Analog supply	3.3	CS switch control block (Flip-Flops)
48	VSSA	Ground	Analog supply	0	CS switch control block (Flip-Flops)

TYPICAL PERFORMANCE CURVES

The following results were obtained after modeling and simulation.

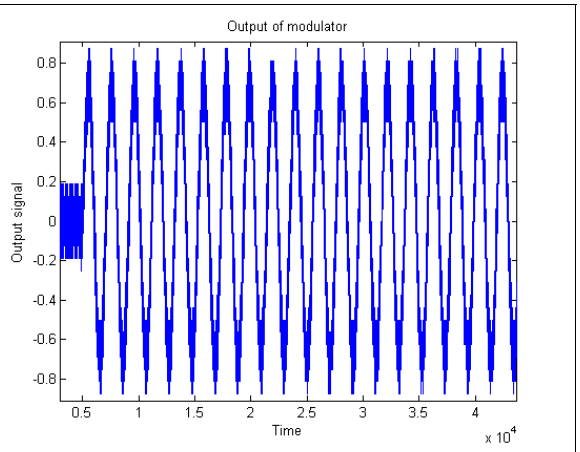


Figure 1: Output of the modulator in the time domain

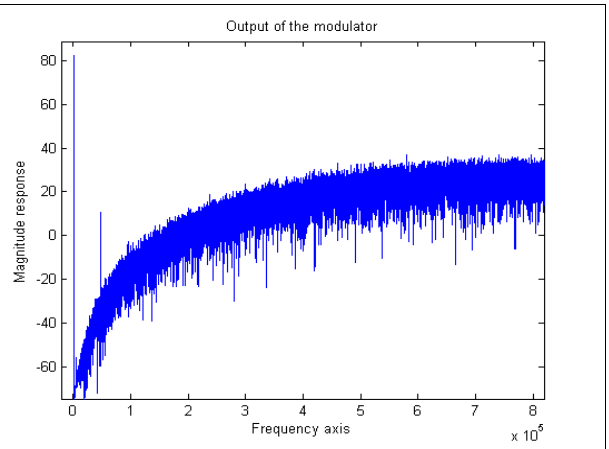


Figure 2: Magnitude response of the modulator for OSR x 256

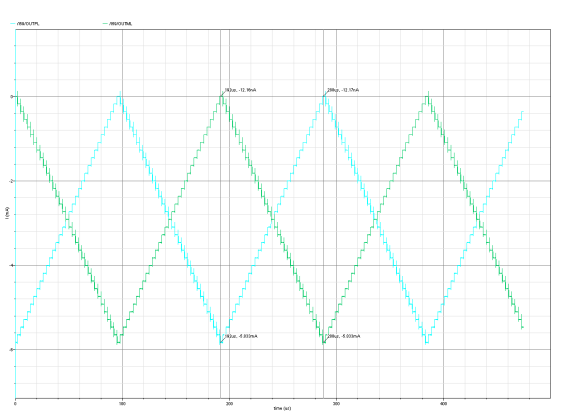


Figure 3: Differential current output I_o(single DAC)

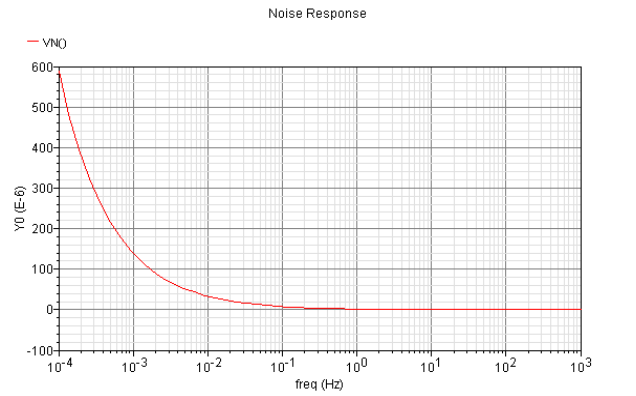


Figure 4: Noise power spectral density (V^2/Hz)

BASIC CONFIGURATION

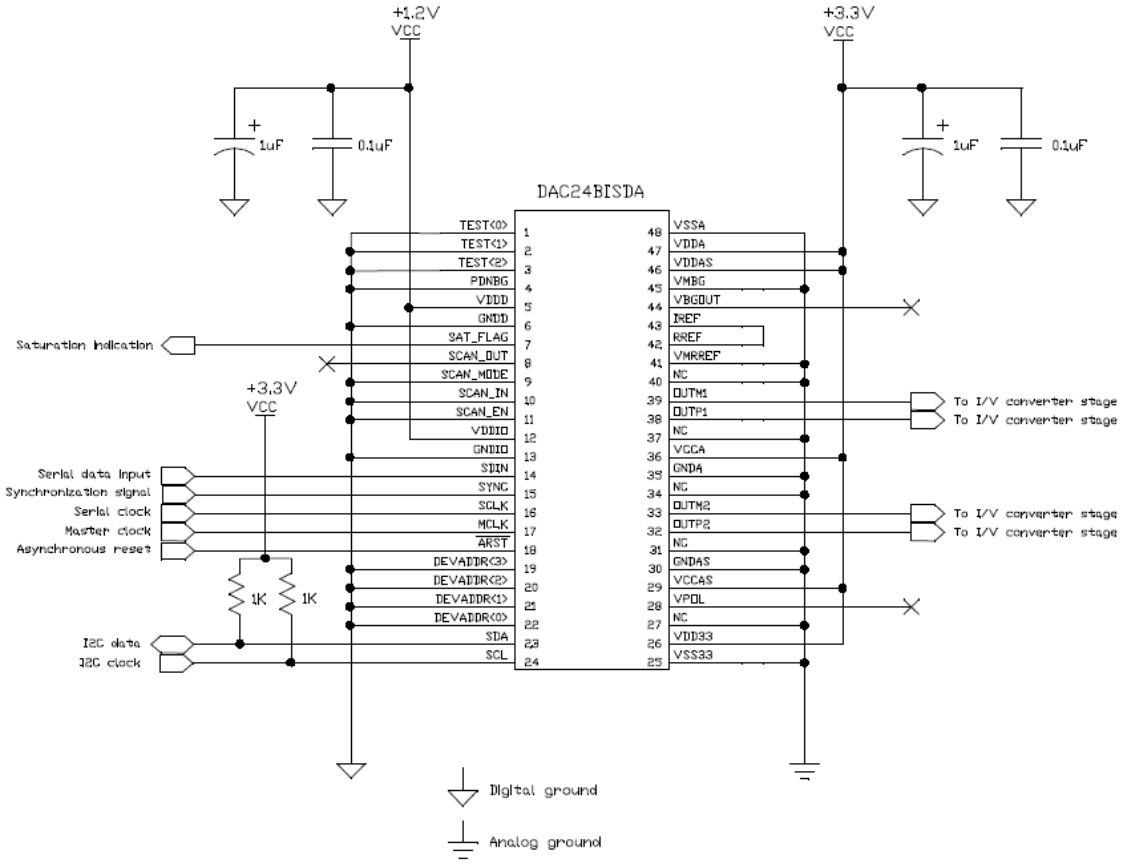


Figure 5: Basic configuration

PACKAGE INFORMATION

48 LEADS CERAMIC FLAT PACKAGE

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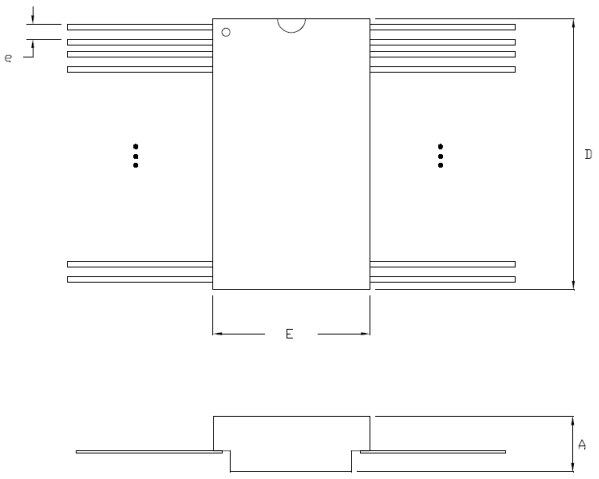

Legend	Nominal dimensions (mm)
A	2.45
E	9.65
e	0.635
D	15.75

- Drawing NOT in scale -