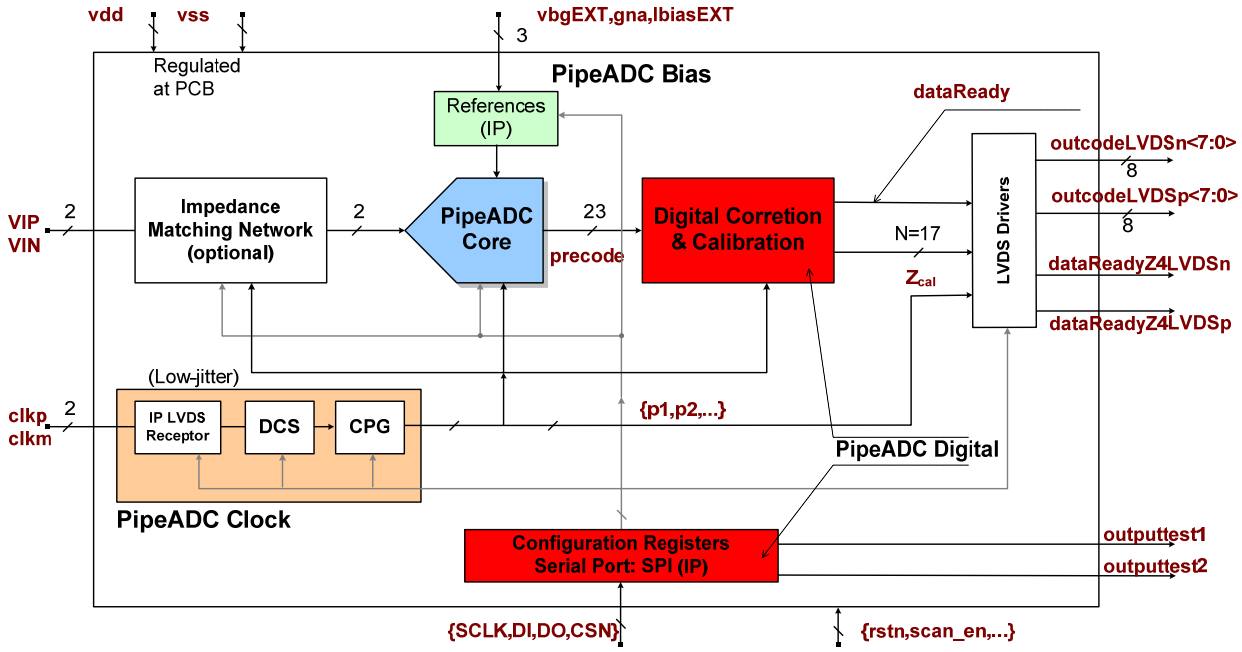
16bADC ASIC: A 1.8V/3.3V 16bit 1-to-100Msps Oversampled Pipeline ADC with Digital Self-Calibration



16bADC Block Diagram

General Description:

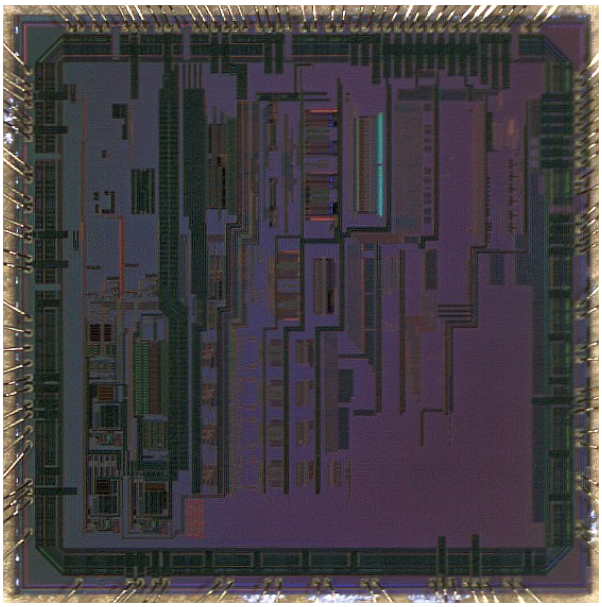
The 16bADC ASIC is a radiation hardening analog-to-digital converter (ADC) developed under the ESA (European Space Agency) framework in a 1.8V/3.3V 0.18µm CMOS process. The base performance specification of this device is 12-ENOB for a 2Vpp differential input signal range within the input bandwidth from 1MHz to 10MHz. If needed, the analog input bandwidth is extended up to 100MHz to allow intermediate-frequency (IF) sub-sampling in communication applications.

The ADC has a SHA-less Pipeline architecture comprising seven stages with digital foreground self-calibration. Bias references are generated on-chip. A differential clock input controls all internal conversion cycles. The analogue and mixed signal section of the ASIC have been implemented exclusively with thin-oxide transistors, robustly protected again latch-ups with dedicated guard rings, using a single power supply voltage of 1.8V. The digital logic section uses the 1.8V standard cells for the core and the 3.3V ones for I/O pads from the rad-hard digital library DARE (= Design Against Radiation Effects). Redundant flip-flops are used in all critical configurations and programming registers, which could be setup using a 4-wire serial interface. The ADC output bits are provided in parallel in LVDS (low-voltage differential signaling) format. To facilitate the receiving operation a data ready clock defines the proper sampling instant.

Applications:

Sampled Video signals, Band-Pass communication signals.

Key Features:



Microphotograph of the 16bADC ASIC (Dec 2016)

Package: Ceramic QFN52 ([1])
Resolution: 16 bits
Control Interface: 4-wire serial port
Analog Input:
Range: 2.0Vpp fully differential
Bandwidth: 1MHz ≤ f_{in} ≤ 100MHz
Digital Output Code:
Encoding: Binary and Two's Complement
Signaling: LVDS standard
Bandwidth: 10 MHz (LP / BP)
ENOB: ~12.0 bits for f_{in} ≤ 10MHz @ 27°C
~ 10.0 bits for 10MHz ≤ f_{in} ≤ 100MHz @ 27°C
SNR: ~ 73 dB (f_{in} ≤ 10MHz @ 27°C)
SFDR: ~ 83 dBc (f_{in} ≤ 10 MHz @ 27°C)
Power supply: 1.8V for Analog and Digital Cores
3.3V for CMOS Digital I/O
Power consumption: ~ 500mW (whole ASIC)
Temperature range: -55° to +100°C. Functional ([2]): -55° to +125°C

Notes: ([1]) Other package solutions are also feasible, please contact us for further details. ([2]) Expected data, real values to be provided.

Radiation Performance:

TID: > 100 krad([3])
SEL and SEFI: immune > 70 MeV·cm^2/mg ([3])
SEE: < 1 Bit/day ([3])

([3]) Minimum expected data, real values to be provided upon completion of radiation tests.

Development Status:

The ASIC has been electrically characterized after fabrication. The core area is approximately 3.460 µm x 3.600 µm (12.43 sqmm). From this area, 10.21 sqmm corresponds to analog part and 2.2 sqmm corresponds to digital part. Radiation performance results are expected soon.

Acknowledgements

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Electrical Features:

Parameter	Unit	Temp. = -55 °C	Temp. = 25 °C Typical Value	Temp. = 100 °C	Conditions
Resolution Encoding: Offset Binary: [0, 65535]	bits	16	16	16	
Power Consumption fsampling: 20 Msps / 80 Msps finput = 10 MHz	mW	470 / 587	456 / 585	507 / 612	Power average
Analog Input Voltage Span	Vp-p	1.99	1.97	1.94	Overload condition

DC Accuracy

Test signal: Filtered sine wave at the available lowest frequency (2.0 MHz)
Test Input Voltage = -0.5 dBFS (~1.9 Vp-p)
Test sampling frequency = 20 Msps
Procedure: Non-overloaded Coherent Sine-Wave Histogram
Sample Number: 3.3 M (65536 x 50)
More insight can be extracted from graphical results in next figures

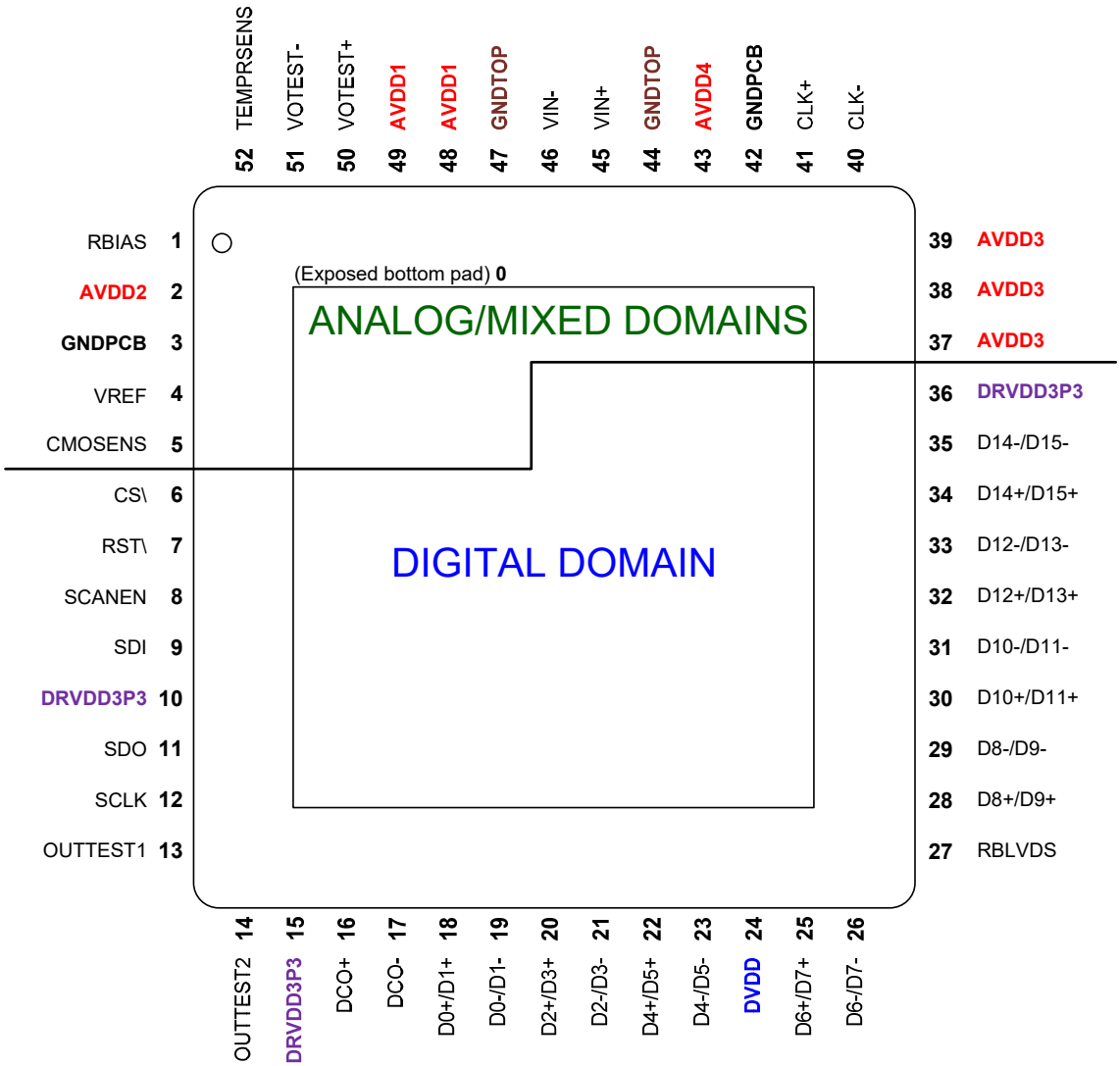
No Missing Codes	-	Guaranteed	Guaranteed	Guaranteed	Code@16 bits
Gain	LSB/V	0.88	0.94	0.89	Code@14 bits
DNL	LSB	[-0.32, 0.34]	[-0.34, 0.39]	[-0.32, 0.58]	Code@14 bits
INL	LSB	±1.1	±1.2	±2.0	Code@14 bits
ENOB	bits	13.2	13.2	12.6	Code@14 bits

AC Accuracy

Test signal: Filtered sine wave at five frequencies from 2.0 MHz to 25 MHz
Test Input Voltage = -1.0 dBFS (~1.8 Vp-p)
Test sampling frequency: Two cases, 20 Msps and 80 Msps
Procedure: Coherent Sine-Wave Averaged Non-windowing FFT Spectrum
Sample Number: 16384 x 4 x 10
More insight can be extracted from graphical results in next figures

ENOB	bits	20Msps / 80Msps	20Msps / 80Msps	20Msps / 80Msps	
		12.35 / 11.82	12.44 / 11.30	11.99 / 11.38	finput = 2.0 MHz
		12.38 / 11.70	12.20 / 11.19	12.05 / 10.90	finput = 5.0 MHz
		11.74 / 11.46	11.68 / 11.05	11.90 / 10.95	finput = 10 MHz
		10.64 / 11.17	10.64 / 10.68	10.60 / 10.10	finput = 25 MHz
SNR	dB				
		77.2 / 75.2	76.7 / 74.3	75.8 / 73.4	finput = 2.0 MHz
		75.5 / 75.5	75.0 / 74.0	75.4 / 72.5	finput = 5.0 MHz
		71.8 / 74.5	71.0 / 73.4	74.1 / 71.8	finput = 10 MHz
		65.1 / 71.9	65.1 / 70.9	64.9 / 68.9	finput = 25 MHz
THD Harmonics with amplitude greater than -100 dBFS. Assuming the first 65 harmonics in 20 Msps case, and the first 151 harmonics in 80 Msps case.	dB				
		79.0 / 74.6	81.6 / 70.1	75.9 / 71.3	finput = 2.0 MHz
		85.3 / 73.1	80.9 / 69.3	77.0 / 67.6	finput = 5.0 MHz
		80.6 / 71.5	79.4 / 68.4	76.9 / 68.2	finput = 10 MHz
		74.5 / 70.1	75.4 / 66.3	74.0 / 62.4	finput = 25 MHz
SFDR	dBFS				
		80.2 / 80.1	82.7 / 71.8	77.7 / 74.4	finput = 2.0 MHz
		90.1/ 75.9	85.1 / 72.8	80.6 / 74.0	finput = 5.0 MHz
		82.5/ 72.4	80.5 / 70.9	80.2 / 77.4	finput = 10 MHz
		75.7 / 77.9	77.1 / 73.9	76.7 / 68.4	finput = 25 MHz

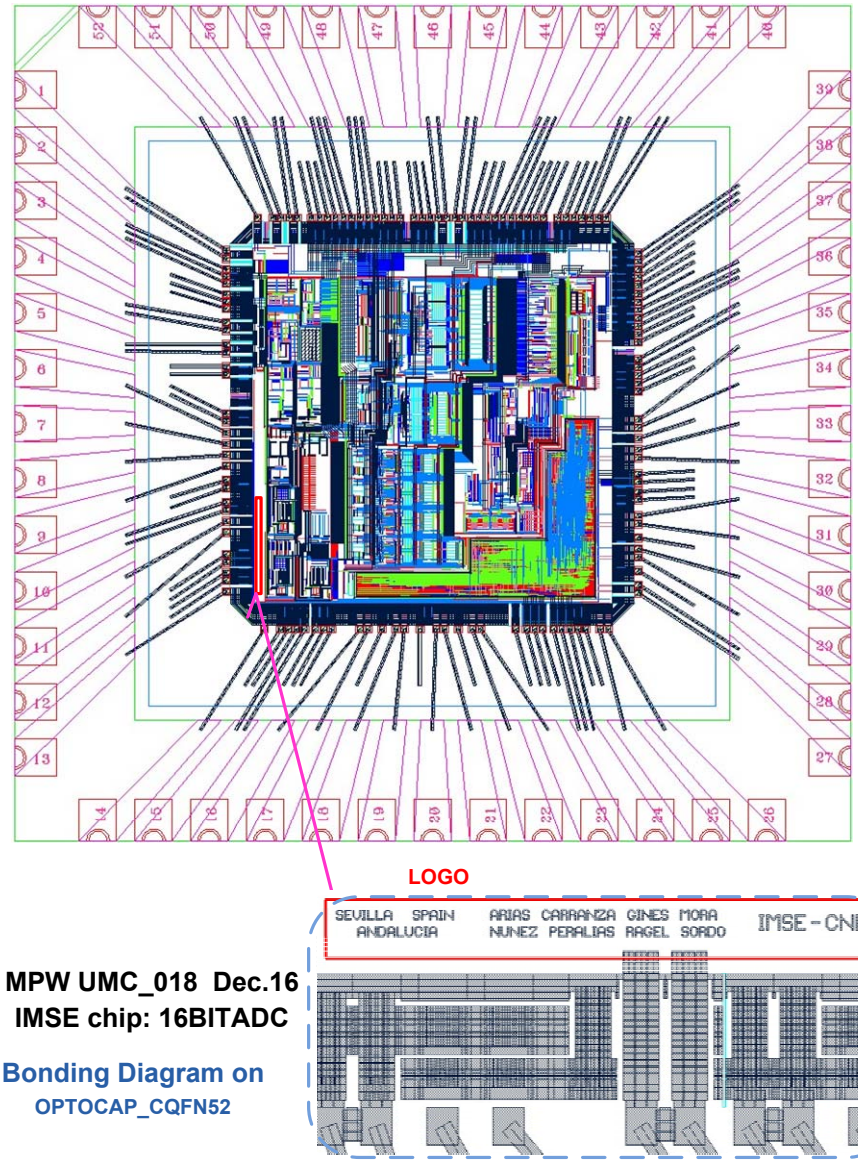
IO Pins:



Top view of the ASIC pin configuration.
Package type: Ceramic QFN52 from OPTOCAP.

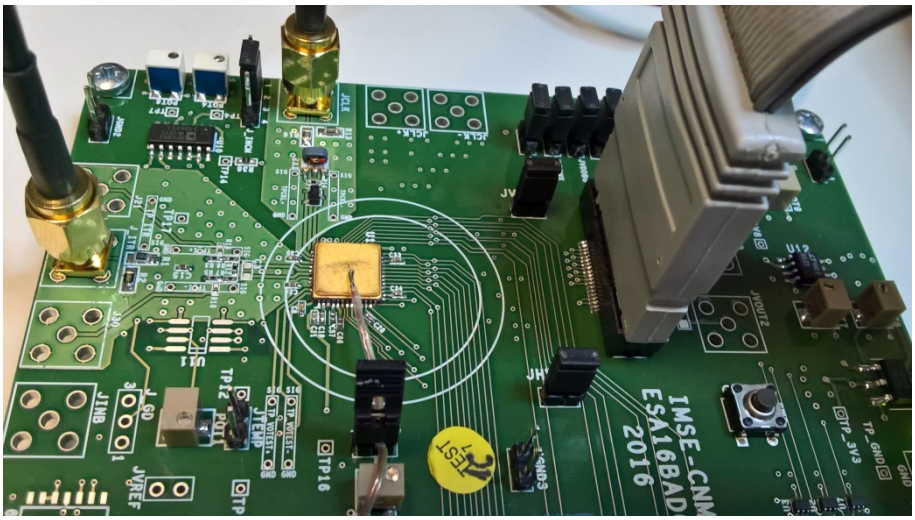
PIN Number	PIN Name	Description	Type
0	GND	Exposed thermal pad. Must be connected to ground.	Ground
1	RBIAS	External reference bias resistor. Outputs a current of ~100 µA.	Input/Output
2	AVDD2	Analog Power Supply (1.827 V Nominal). Bias subsystem.	Supply
3	GNDPCB	External common ground.	Ground
4	VREF	External voltage reference (optional by configuration). Inputs a voltage of ~1.225 V.	Input
5	CMOSENS	Internal Common Mode monitor. When it is enable, it outputs a voltage of ~1.0V	Output
6	CS\	SPI chip select (Active Low)	Input
7	RST\	Chip reset (Active Low)	Input
8	SCANEN	Scantest enable	Input
9	SDI	SPI serial data input	Input

10	DRVDD3P3	Digital Output Driver Supply (3.3 V Nominal).	Supply
11	SDO	SPI serial data output	Output
12	SCLK	SPI serial clock	Input
13	OUTTEST1	Digital test output. Depending on configuration output will be the Data Overrange flag or other error flags.	Output
14	OUTTEST2	Digital test output. Depending on configuration output will be the End Calibration flag, or the Reset state or the Process Sensor output among others.	Output
15	DRVDD3P3	Digital Output Driver Supply (3.3 V Nominal).	Supply
16	DCO+	Data Clock LVDS output. (True)	Output
17	DCO-	Data Clock LVDS output. (Complement)	Output
18	D0+/D1+	LVDS Output Data (True). D0 is the code LSB.	Output
19	D0-/D1-	LVDS Output Data (Complement). D0 is the code LSB.	Output
20	D2+/D3+	LVDS Output Data (True).	Output
21	D2-/D3-	LVDS Output Data (Complement).	Output
22	D4+/D5+	LVDS Output Data (True).	Output
23	D4-/D5-	LVDS Output Data (Complement).	Output
24	DVDD	Digital Core Supply (1.8 V Nominal).	Supply
25	D6+/D7+	LVDS Output Data (True).	Output
26	D6-/D7-	LVDS Output Data (Complement).	Output
27	RBLVDS	External LVDS Bias resistor (6.8kΩ Nominal)	Input/Output
28	D8+/D9+	LVDS Output Data (True).	Output
29	D8-/D9-	LVDS Output Data (Complement).	Output
30	D10+/D11+	LVDS Output Data (True).	Output
31	D10-/D11-	LVDS Output Data (Complement).	Output
32	D12+/D13+	LVDS Output Data (True).	Output
33	D12-/D13-	LVDS Output Data (Complement).	Output
34	D14+/D15+	LVDS Output Data (True). D15 is the code MSB.	Output
35	D14-/D15-	LVDS Output Data (Complement). D15 is the code MSB.	Output
36	DRVDD3P3	Digital Output Driver Supply (3.3 V Nominal).	Supply
37	AVDD3	Analog Power Supply (1.827 V Nominal). Clock subsystem.	Supply
38	AVDD3	Analog Power Supply (1.827 V Nominal). Clock subsystem.	Supply
39	AVDD3	Analog Power Supply (1.827 V Nominal). Clock subsystem.	Supply
40	CLK-	ADC clock differential input (Complement)	Input
41	CLK+	ADC clock differential input (True)	Input
42	GNDPCB	External common ground.	Ground
43	AVDD4	Analog Power Supply (1.827 V Nominal). Mixed subsystem.	Supply
44	GNDTOP	External common ground in Top Plane.	Ground
45	VIN+	Analog differential input (True)	Input
46	VIN-	Analog differential input (Complement)	Input
47	GNDTOP	External common ground in Top Plane.	Ground
48	AVDD1	Analog Power Supply (1.827 V Nominal). Analog subsystem.	Supply
49	AVDD1	Analog Power Supply (1.827 V Nominal). Analog subsystem.	Supply
50	VOTEST+	Analog test differential output (True)	Output
51	VOTEST-	Analog test differential output (Complement)	Output
52	TEMPRSENS	Temperature sensor output. Must be connected to an external reference resistor. Outputs a current of ~50 μA.	Input/Output



MPW UMC_018 Dec.16
IMSE chip: 16BITADC

Bonding Diagram on
OPTOCAP_CQFN52



16bADC ASIC Test Board