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10108 - Configurable mixed-signal MF ASIC

Summary Report

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1 Introduction

1.1 Executive summary

This project has its origins in the low availability of high performance components that could cope with the stringent radiation requirements of ESA's Juice Mission. In order to face that need, ESA initiated two TRP activities (one of them addressed in this project) to create radiation tolerant high-performance mixed-signal components for the Juice instrumentation teams.

The design team that took part on the activity was led by ARQUIMEA Ingeniería, a company devoted to space electronics, microelectronics and actuators. It also counted on the valuable participation for the design of IMB a microelectronics research institute, the AHA design group of UPC and UC3M.

Throughout the project execution phase, the project objectives where tailored and adapted to target the most valuable goals within the timeframe and budget available and always keeping in mind both the best achievable performances and the potential use of the activity outcomes. So departing from the original specification that aimed the design of 8 identical analogue processing blocks that could be configured individually as ADC, DAC, Filter, LNA, PA, CCD signal processor and Radiation detector, instead, it was decided to pursue and validate the basic building blocks separately (IPs). The design, verification and validation effort put in place to demonstrate the challenging requirements of each of the mixed signal blocks required much more time that the one originally conceived for the project and showed the great complexity of the development of high performance mixed signal space chips.

Given the challenging specifications included in the statement of work and the fact that most of the design objectives were reached with a single tape-out, the activity can be considered a technical success. Additionally it served to improve and consolidate the mixed signal flow to be used when implementing space grade ASICs in DARE/UMC180 technology and it also stablished a clean methodology of collaboration between research institutes and companies to achieve ESA project goals.

The outcomes of the project are a set of high performance IPs, in particular an ADC, LNA, PA, Bandgap, Regulator and SPI digital interface, that will be made available to the European Community through ESA for its reuse in other activities with minimum risk. It is important also to highlight that a great number of lessons have been learnt by the project team that will definitely contribute to raise the quality standards of not only the groups involved in this activity but also those that have access to the project summary and outcomes.

1.2 Scope

This document provides a summary of the work done during the project including its context, a description of the programme of work, a report on the activities performed and the main results achieved.

1.3 Documents

1.3.1 Applicable documents

Ref.	Number	Title
AD-01	4000101556/10/NL/AF	ESTEC contract 4000101556/10/NL/AF with ARQUIMEA INGENIERIA S.L "Front-end readout ASIC technology study and development test vehicles for front-end readout ASICs"
AD-02	CCN1	Contract Change Notice Number 1
AD-03	CCN2	Contract Change Notice Number 2
AD-04	CCN3	Contract Change Notice Number 3

Table 1-1: List of applicable documents

1.3.2 Reference documents

Ref.	Number	Title
RD-01	4000101621/10/NL/AF	ESTEC contract 4000101621/10/NL/AF with ARQUIMEA INGENIERIA S.L "Radiation Tolerant analogue/mixed signal technology survey and test vehicle design"
RD-02	N/A	Stepan Sutula (2015, November). Low Power High Resolution CMOS Switched Capacitor Delta Sigma Analog to Digital Converters for Sensor Applications. PhD Thesis
RD-03	ARQ_10108_DSH_001	ARQ-CVB001 Datasheet
RD-04	ARQ_10108_DSH_002	ARQ-CVC001 Datasheet
RD-05	ARQ_10108_RPT_001	Performance compliance matrix report

Table 1-2: List of reference documents

1.4 Acronyms and abbreviations

AD Applicable Document(s)

ADC	Analogue to Digital Converter
ADR	Architectural Design Review
ASIC	Application Specific IC
BF	Bessel Filter
CCD	Charged Coupled Device
CCN	Contract Change Notice
CDR	Critical Design Review
CSIC	Consejo Superior de Investigaciones Científicas
DAC	Digital to Analogue Converter
DARE	Design Against Radiation Effects
EDA	Electronic Design Automation
ENOB	Effective Number of Bits
ESA	European Space Agency
ESTEC	European Space TEchnology centre
IP	Intellectual Property
LNA	Low Noise Amplifier
LVDS	Low Voltage Differential Signalling
MPW	Multi Project Wafer
NA	Not Applicable
PA	Power amplifier
RD	Reference Document(s)
SFDR	Spurious Free Dynamic Range
SNR	Signal-to-Noise ratio
SSDP	Scalable Sensor Data Processor
TASE	Thales Alenia Space España
UC3M	Universidad Carlos III de Madrid
UPC	Universidad Politécnica de Cataluña

2 Context

This project was conceived in the frame of ESA's Cosmic Vision programme related to the interplanetary mission to Jupiter named Juice. In the radiation environment envisaged for that mission, the electronic equipment would be required to withstand up to 300krad of Total Ionization Dose. The availability of high performance components that could cope with that requirement was low or non-existent and hence ESA decided to initiate two TRP activities to create radiation tolerant high-performance mixed-signal components for instrumentation.

ARQUIMEA, a young company at the time of the tender, decided to present a proposal for both activities based on the space electronics background of its key people, the strong microelectronics expertise of the manager that coordinated the technical proposal and the valuable experience gained in the development of a space chip set for CASA (REDSAT) which was eventually qualified and used in the mission where it was developed. In addition to ARQUIMEA, the proposal team was completed with well settled and reputed experts from three Spanish institutions: CSIC (in particular the Microelectronics Institute of Barcelona), UPC (in particular the AHA group) and UC3M. All of these institutions had a demonstrated background on the fields where their contributions would take place. The consortium prepared a complete and detailed proposal for both tenders which were finally selected by ESA to take care of the activity.

This document addresses exclusively the contract specified in AD-01 however it has run in parallel with the contract detailed in RD-01. Given the fact that the two contracts have some similarities (aiming high performance mixed-signal components as described before) and that both have been developed by the same design team, a few references are made in this text to the RD-01activity for clarification purposes.

3 Programme of work

The activity was originally conceived to last 24 months from kick off to final review. The evolution of the project was such that if finally took 72 months. Three CCNs were signed to cope with this extension (AD-02, AD-03 and AD-04), to reflect the project updated objectives and to grant extra funds (125k€). As can be understood, a great number of additional engineering and administrative hours were spent both from the project consortium and ESA to come to a successful project conclusion.

The following paragraphs will give a detail on the main activities performed in each project phase in chronological order.

3.1 Architecture definition phase: From KO to MS1 (ADR)

In this phase, the architecture of the building blocks of the project was tailored. In the original proposal the target ASIC required 8 identical analogue processing blocks that could be configured individually as ADC, DAC, Filter, LNA, PA, CCD signal processor and Radiation detector. After a preliminary analysis on the ASIC overall architecture it was agreed that targeting 8 analogue processing blocks would be a nice objective for the future but it was first required to validate a single analogue processing entity. After that, the main focus was to address the architecture of the principal building blocks of the remaining analogue processing entity: ADC, DAC, LNA, PA and Filter.

3.2 Block Design Phase: From ADR to MS2 (PDR) and MS3 (Delta-PDR)

The detailed design work started in parallel for each of the building blocks. Every project participant started with the schematic design of its IP, iterating to reach the agreed block specifications. However this iterative process took much longer than expected especially for the ADC and DAC blocks. With regards to the former, it was agreed to divide the job into four different sigma delta modulators, to cover all the frequency/resolution range. As for the DAC also two different sub-modules were targeted to address the required specification nevertheless only the low speed one was finally included. The LNA and PA schematic designs were the first ones completed.

Regarding layout, as soon as it was completed for each of the blocks, post layout simulations started. When the implementation of each of the blocks was mature enough for a Critical Review, a meeting was held with ESA for block approval. It has to be noted that the layout of the digital side (mainly used for configuration) was not performed by a project participant but as an external service (IMEC) since the DARE library was used. Netlists were provided to IMEC along with physical constraints and restricted views of the layout were returned back by them to integrate them on the overall ASIC floor plan as will be detailed later.

The successive iterations needed for most of the blocks, at schematic level and also at layout level extended quite a lot the design phase of the IPs which shows the big complexity of these tasks. Once all IPs layout and post layout simulations were completed, MS3 (Delta-PDR) was achieved. This meeting took place on 16/05/2014.

3.3 CVB-001 and CVC-001 integration and fabrication: From Delta-PDR to MS4 (Pre-CDR)

Once all IPs design was completed, the integration process started along with the overall chips planning and floorplan. Due to the experience gained in the activity detailed in RD-01 and the updates performed in the library, the interaction with IMEC for the integration of pads and digital backed was seamless.

Due to the long time it took to complete the design phase, an assessment was made with regards to the tape-out dates of the chips. It was finally decided to tape out the CVB-001 chip in the 08/09/2014 MPW window and the CVC-001 in the 01/12/2014 one.

Despite the extra time included, it was not possible to close a fully functional DAC IP.

3.4 CVB-001 and CVC-001 validation: From delta-PDR to Project closure

Once the designs were taped out, IMEC took care of the fabrication and packaging services. The chosen packages were standard ones with the least inductance possible to improve performances: QFN64 for CVB-001and LQFP120 for CVC-001. Packaged CVB-001chips were received from IMEC on February 2015 and packaged CVC-001 chips on June 2015.

When the chips were ready, the validation phase started. The overall activity was divided in two main stages: functional testing and temperature & performance testing. The main objective of the first stage was to build a simple functional test board to check the basic functionality of the fabricated ASICs and to confirm that they were operative. The second stage addressed the behaviour of the chips in temperature and their performance (as much as it could finally be measured)

The functional testing proved that the ASICs were operative. Additionally, the IPs behaviour was verified to be functionally correct for the ADC, LNA and PA however the BF and the DAC showed big degradations.

After the functional tests were performed, the setup for the performance and temperature measurements was completed. At the same time, it was agreed with ESA to include an additional chip (referred as LOPO in the rest of the document) on the validation campaign. This chip contained only one of the ADC modulators designed in the frame of the project, in particular the LSSB one (as opposed to the four modulators included in CVB-001) and was taped-out by CSIC-IMB with their own funds in the frame of a doctoral thesis presentation (RD-02). A few dies were sent to ARQ so that they could be assembled in the frame of the Cosmic Vision activity. A QFP60 package was selected for such purpose.

The main challenge of the performance validation activity was to reach the IP performance requirements as much as possible but given the low noise margins, the cleanness of the input signals and the high precision of the modulators it was quite complicated to reach many of them. At the end, in many cases the limiting factor was proved to be either the equipment or the boards or the setup. Nevertheless for some particular cases quite high performance measurements were finally accomplished.

4 Main results

In the following paragraphs detailed project results will be discussed by means of an interpretation of the verified and validated performances measured for the different blocks. It shall be noted that the Statement of Work specs were derived into block level specifications which were then verified at block level and finally verified at top level and validated. Through the whole section, the terms IP or block level verification will make reference to the simulations done considering the IP or block without its context (no pads and no package influences) whereas top level verification will make reference to IP or block level verification considering pads and package. For a complete description of the ASIC functionality and performances please refer to RD-03, RD-04 and RD-05.

The legend of the summary tables available for each IP is the following:

Column field	Purpose
SoW spec	Statement of Work Specification
IP spec	IP specification derived from the SoW and agreed to be targeted
IP ver	IP verification results
CVB/CVC ver	CVB/CVC verification results
CVB/CVC spec	Specification derived from the SoW and IPs used as reference for the CVB/CVC chip development that includes all IPs.
CVB/CVC/LOPO val	CVB/CVC/LOPO validation results

Table 4-1: IP performance summary legend

4.1 ADC

In order to comply with the wide range of frequencies and effective resolutions specified for the ADC development it was agreed to divide the converter into four modules:

- Low-speed single-bit (LSSB): a ΣΔ modulator designed for the [50; 150] kHz signal frequency range and with the highest resolution
- High-speed single-bit (HSSB: a) ΣΔ modulator designed for the [150; 500] kHz signal frequency range.
- Low-speed multi-bit (LSMB): a ΣΔ modulator, designed for the [0.5; 2] MHz signal frequency range.
- High-speed multi-bit (HSMB): a ΣΔ modulator, designed for the [2; 5] MHz frequency range and the lowest resolution.

As described before, the four modulators were implemented on the CVB-001 chips with their inputs interconnected. Additionally, the LLSB modulator was also integrated in the LOPO ASIC.

The ENOB of each of the modulators has been set as the main figure of merit for performance evaluation. From the IP point of view the design was correctly verified at block level reaching the expected performances on the LLSB modulator (18 ENOB at 100 Ksps) both at schematic and post layout (including process, temperature and mismatch variation). For the intermediate frequencies of the LSBM modulator, also the block level simulations showed good results (15 ENOB at 1Msps). For higher frequencies (HSMB modulator) it was not possible to reach the expected performances even at IP level (7 ENOB at 10Msps). Nevertheless, the promising results of the LLSB modulator made clear that the focus should be put on a complete verification and validation of this module.

The top level verification of the blocks showed that including the four modulators on the same die had major drawbacks in terms of performance. Additionally, the fact that the ADC input was the same for all modulators reduced the performance even more. However, this degradation was quite complicated to assess because of the demanding characteristics (in terms of CPU and memory) of the top level simulations with all the blocks active at the same time. Apart from a few checks with all the blocks connected, most of the top level simulations were run on one modulator considering the rest as black boxes. At this level it was verified that with the configuration of modulators on the CVB-001 chip, the HSMB and the LSMB modulators could be discarded from the performance point of view (approximately 50% reduction).

With the information obtained from the verification phase, the validation was mainly targeted to assess the performance of the LSSB modulator both on CVB-001 and LOPO. The HSSB was preliminary tested as well but in spite of being functional, the noise measured inside the band of interest was above expectations so the overall performance validation of this block was finally discarded.

With regards to the LSSB modulator, the measured performance on the CVB-001 is approximately 10 ENOB, being the limiting factor of the quality of the digitized signal the system noise (mainly due to board setup). With regards to the version included in LOPO, the measured performance was limited in this case by the purity of the input signal, reaching up to approximately 15 ENOB. It is also important to highlight that the behaviour of the modulator in temperature is quite stable for all the operational range.

The future use of the LSSB IP seems promising considering the electrical results obtained. It would be very interesting to also assess in the future its performances under radiation.

A summary of the IP performance can be found in the following table.

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVB spec	CVB ver	CVB val	LOPO val	Comments
1	ADC_SPLR	Minimum Nyquist sampling rate (at most)	MS/s	0,1	0,1	0,1	0,1	0,1	0,1	0,1	

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVB spec	CVB ver	CVB val	LOPO val	Comments
2	ADC_ENOB_MAX	Maximum Effective number of bits @ADC_SPLR_ MIN (at least)	bits	19	18	18	17	-	9,47	14,57	Top level simulations of the LSSB module were not conclusive since the simulations could not complete the required number of cycles for a proper FFT. Performances of the LOPO ASIC were limited by the input source noise.
3	ADC_SFDR_MAX	Spurious Free Dynamic Range @ADC_SPLR_ MIN (at least)	dBc	130	110	-	104	-	81,7	95,3	
4	ADC_IDD_MIN	Overall current consumption @ADC_SPLR_ MIN (at most)	mA	1	2	9,07	2	-	10	7	
5	Operational temperature range	Temperature range where performance is maintained	ºC	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85	-10 to 85	

Table 4-2: ADC performance summary

4.2 DAC

The ENOB of the DAC has been set as the main figure of merit for its performance evaluation. From the IP point of view the design was verified at block level reaching 15.4 ENOB (out of the 18 specified). However at top level it was observed that the full DAC was not operative, only the flash DAC stage could be functionally verified.

At validation level the results were in line with the top level verification and hence the MASH stage of the DAC had to be bypassed. Unfortunately it was also observed that on the flash DAC stage the behaviour was not as expected since its output signals were rectified above 0.8V. Considering these results, it was finally agreed not to proceed with any further validation of the block

The status of the IP at the end of the project is that it is not mature enough to be reused in future projects as it is.

4.3 LNA

This block had a great number of configuration options and switches, all of which have been verified at block level and some of which were verified at top level and later validated. From the IP point of view the design was correctly verified at block level reaching the agreed performances. As a remarkable example, the noise density reached is between 5.9 and 9.2 nv/√Hz. The top level simulations run also showed very good results; in line with the block level ones (verified for a 30dB gain).

The validation of this block did not cover all parameters due to the high number of configuration options; however the tested modes show good results and in all cases the measurements were limited mainly by the input source. Additionally, the performance is maintained over the whole operational range.

The future use of the IP is still open. Although very good results have been obtained in this activity it still has to be analysed how the block can be re-used since no feedback from potential users has been received so far. It would be very nice to know the behaviour of the block under radiation but similar (and hence good) results to the ones presented in the activity detailed in RD-01 are expected.

A summary of the IP performance can be found in the following table.

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVC spec	CVC-001 ver	CVC-001 val
1	LNA_VV_GF	Voltage mode: gain flatness between LNA_FMIN and LNA_FMAX for G=21dB (at most)	dBc	0,2	0,4	0,4	0,4	-	1,284
2	LNA_VV_N_TYP	Voltage mode: typical noise density	nV/√Hz	-	6.6@1	6.6@1	-	7.13@3	289,4@100
3	LNA_VV_THD_DIF_TYP	Voltage mode: Typical Total Harmonic Distortion for differential input (2Vpp tone, 0dB gain, 1kΩ//1pF load, 1,5V common mode in, 900mV common mode out)	dB@MHz	-	-110@0,1 -103@0,3 -94@1 -89@2 -76@5	-110@0,1 -103@0,3 -94@1 -89@2 -76@5	-	-	-80,14@0,1 -72,81@0,3 -71,03@1 -70,54@2
4	LNA_VV_IDD_MAX	Voltage mode: Current consumption @LNA_VV_GMAX	mA	4	24	24	20	-	20,15
5	Operational temperature range	Temperature range where performance is maintained	ºC	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85

Table 4-3: LNA performance summary

4.4 PA

This block had also a great number of configuration options and switches, all of which have been verified at block level and some of which were verified at top level and later validated. From the IP point of view the design was correctly verified at block level reaching the agreed performances. As remarkable examples, the output current reached in voltage mode was 160 mA and the THD was 84dB (at 0.3MHz) and 74dB (1MHz) in voltage output mode. The top level simulations run showed comparable THD results (68 dB at 1MHz).

The validation of this block did not cover all parameters due to the high number of configuration options. As an example, The THD measured in voltage output mode at 0.3MHz was 73.4 dB which is in line with the expected results taking into account that the performance was limited mainly by the input source. An interesting result observed was that the final power consumption measured was 60% lower than expected, measuring 100mA in voltage output mode. Additionally and in line with the results obtained on the LNA, the performance is maintained over the whole operational range.

The future use of the IP is still open. Although very good results have been obtained in this activity it still has to be analysed how the block can be re-used since no feedback from potential users has been received so far. It would be very nice to know the

behaviour of the block under radiation but similar (and hence good) results to the ones presented in the activity detailed in RD-01 are expected.

A summary of the IP performance can be found in the following table.

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVC-001 spec	CVC-001 ver	CVC-001 val
1	PA_VX_F_MAX	Voltage output mode: maximum input frequency (at least)	MHz	10	17@-0,4dB 27@-3dB	17@-0,4dB 27@-3dB	17@-0,4dB 28@-3dB	19,65@-3dB	>2
2	PA_VX_THD_TYP	Voltage output mode: Typical Total Harmonic Distortion (at most)	dB	-	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-87@0,1MHz -84@0,3MHz -74@1MHz -79@2MHz -48@5MHz	-67,72@1MHz	-75,5@01MHz -73,4@0,3MHz -66,6@1MHz 64,2@2MHz
3	PA_VX_IDD_MAX	Voltage output mode: maximum current consumption for single-ended 50Ω load (at most)	mA	-	160	160	160	-	100
4	PA_TID	Maximum TID	krad(Si)	300				> 505	
5	Operational temperature range	Temperature range where performance is maintained	ºC	-10 to 85	-10 to 85	-10 to 85	-10 to 85	-	-10 to 85

Table 4-4: PA performance summary

4.5 BF

The Bandwidth of the Bessel filter has been set as the main figure of merit for performance evaluation. The functionality of the Bessel filter was split in two designs to cover different frequency ranges: one design with 1 MHz cut-off frequency and another with 5 MHz. In the design phase, different interpretation on the bandwidth calculation of this block led to deviations from the requirements: the bandwidth was calculated as the frequency of the dominant pole instead of the bandwidth that accomplishes the gain flatness specification. For the lower cut-off frequency design, the top level post–layout simulations gave a 0.5MHz -3dB bandwidth instead of the expected 1MHz. Furthermore, both designs are limited by distortion, presenting a worst case THD at block level of around -30dB for the lower bandwidth design and -22dB for the higher bandwidth one, which are far from the performances of the rest of the blocks verified at block level.

In the validation phase, this block was discarded in an early stage since none of the bias voltages were close to the expected value obtained in the verification phase for the two auto-calibration options.

The future use of the IP is still open. The different interpretation of the bandwidth and the obtained distortion results cause that the use of the Bessel filter in conjunction with the other blocks developed in this project is not possible. Additionally, filters are very application dependent so the possibilities of its re-use in the future are lower than for the rest of the IPs.

A summary of the IP performance can be found in the following table.

	Parameter	Description	Unit	SoW spec	IP spec	IP ver	CVC spec	CVC0-01 ver	CVC001 val	Comments
1	BF_BW_MAX	Maximum configurable bandwidth (at least)	MHz	10	5	5,33	-	-	-	No trans-impedance amplifier was used in the validation of CVC-001. Without it no valid signal could be obtained at the output of this amplifier for any of the biasing options.
2	BF_SFDR_INTER4	Spurious Free Dynamic Range @BF_BW_INTER4	dBc	96	62	72,42@1kHz 56,06@10kHz 34,45@0,2MHz	62	~38,3 @0,1MHz	-	

Table 4-5: BF performance summary

4.6 Common blocks

Several common blocks were included both in the CVB-001 and CVC-001chips but they were also tested and measured in the parallel activity detailed in RD-01. For more information, please refer to RD-05.