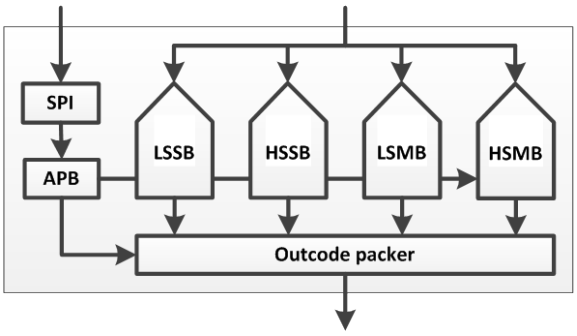
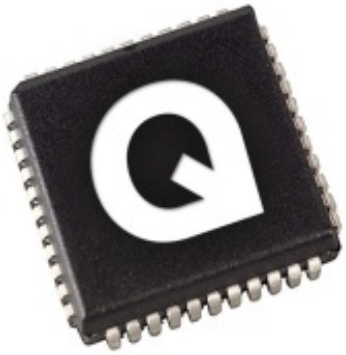
ARQ-CVB001
Rad-hard programmable ΣΔ modulator

Functionalities

- Low speed single-bit (LSSB) ΣΔ modulator
- High speed single-bit (HSSB) ΣΔ modulator
- Low speed multi-bit (LSMB) ΣΔ modulator
- High speed multi-bit (HSMB) ΣΔ modulator

Block diagram





Common features

- UMC L180 / DARE180 technology
- IO supply voltage: 3.3V
- Operation temperature range: [-10 ; 85] ^{o}C
- Functional temperature range: [-55 ; 125] ^{o}C
- Rad-hard: 300 krad TID / 60 MeV·cm^{2}·mg^{-1} / 1E-10 errors/bit/day
- Switch-off capability per modulator

LSSB ΣΔ modulator features

- Multiple sampling rates
- Up to 18 ENOB
- Up to 0.145 MHz signal bandwidth
- Maximum analogue current consumption: 8,5 mA
- Maximum digital current consumption: 2 mA

HSSB ΣΔ modulator features

- Multiple sampling rates
- Up to 16.3 ENOB
- From 0.175 to 0.465 MHz signal bandwidth
- Maximum analogue current consumption: 80 mA
- Maximum digital current consumption: 30 mA

LSMB ΣΔ modulator features

- Multiple sampling rates
- Up to 14.5 ENOB
- From 0.64 to 1.755 MHz signal bandwidth
- Maximum analogue current consumption: 110 mA
- Maximum digital current consumption: 40 mA

HSMB ΣΔ modulator features

- Multiple sampling rates
- Up to 13.9 ENOB
- From 2.14 to 5.00 MHz signal bandwidth
- Maximum analogue current consumption: 290 mA
- Maximum digital current consumption: 60 mA

Applications

- High resolution acquisition systems
- Moderate frequency acquisition systems

Available options

Product	Quality Level	Variant (*)	Temperature ranges (^{o}C)		Ordering number	Description
			Operational	Functional		
ARQ-CVB001	S (Space)	00	[-10 ; 85]	[-55 ; 125]	ARQ-CVB001S-00	Naked die
ARQ-CVB001	M (Militar)	01	[-10 ; 85]	[-55 ; 125]	ARQ-CVB001M-01	LQFP120 package

(*) other packaging options, including raw die format, are also available under request.

Index

Glossary

ADC	Analogue Digital Converter
Addr	Address
APB	Advanced Peripheral Bus
ASIC	Application-Specific IC
CLK	Clock
ChipID	Chip Identification
CPHA	SPI Clock Phase
CPOL	SPI Clock Polarity
CS	Chip selection
DEM	Dynamic Element Matching
ENOB	Effective Number Of Bits
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
HSMB	High-Speed Multi-bit
HSSB	High-Speed Single-bit
LSMB	Low-Speed Multi-bit
LSSB	Low-Speed Single-bit
LSB	Least Significant Bit
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
PCB	Printed Circuit Board
SCLK	SPI Clock
SDNR	Signal Difference Noise Ratio
SEE	Single-Event Effect
SEL	Single-Event Latch-up
SFDR	Spurious Free Dynamic Range
SPI	Serial Port Interface
THD	Total Harmonic Distortion
TID	Total Ionising Dose
VDDA	Analogue power supply
VDDD	Digital power supply
WC	Worst Case

System overview

ARQUIMEA's ARQ-CVB001 is a radiation hardened programmable ΣΔ modulator. It is composed by four modulators, each one designed for a non-overlapped signal band. Only one modulator is active at a time depending on the bandwidth of the input signal.

The four modulators can be classified as function of resolution (from highest to lowest) and signal bandwidth (from lowest to highest):

1) LSSB modulator
2) HSSB modulator
3) LSMB modulator
4) HSMB modulator

LSSB and HSSB modulators have single-bit output while LSMB and HSMB have it multi-bit (5-bits). In order to reduce the frequency of output code D, several conversions have been packed in a 20-bits word: 20 conversions for the single-bit modulators (LSSB and HSSB) and 4 conversions for the multi-bit ones (LSMB and HSMB). The oldest conversion occupies the D's MSB(s) while the newest the LSB(s). In any case, the output code needs to be post processed (digital filtering and down-sampling) to obtain the conversion with the effective resolution.

ARQ-CVB001 is configured through a Serial Port Interface and dedicated pins (for analogue circuitry biasing).

Interfaces

Communication with ARQ-CVB001 is possible through: 1) direct chip ports and 2) SPI (to program internal configuration registers).

Ports description

ARQ-CVB001 ports are collected in Table 2. Column # collects the port number in the package. Column “pin type” gives the nature of each signal, as one of the options collected in Table 1.

Acronym	Meaning
AI	Analogue Input
AO	Analogue Output
AIO	Analogue Input / Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input / Output
GND	Ground reference
PWR	Power supply

Table 1: Pin type legend

#	Name	Type	Functionality	Additional Information
1	VSSA	GND	Analogue ground (0V) paired with pin 64 (VDDA).	See pin 6.
2	REF_BOOT	AI	Internal DAC and bootstrap reference	1.4V DC voltage (low noise) (also TID test bias) Differential signal: REF_BOOT (plus) / REF_DAC (minus) DC/rms current compliance: [0.38 ; 4] / [1.4; 24.2] mA
3	REF_DAC	AI	Internal DAC and bootstrap reference	0.4V DC voltage (low noise) (also TID test bias) Differential signal: REF_BOOT (plus) / REF_DAC (minus) DC/rms current compliance: [0.37 ; 4] / [1.4; 19.3] mA
4	REF_IN	AI	Common mode reference	0.9V DC voltage (low noise) (also TID test bias) DC/rms current compliance: [0.014 ; 0.11] / [0.37; 6.1] mA
5	VDDA	PWR	Analogue supply (3.3V) paired with pin 6 (VSSA)	All VDDA pins are connected. Overall VDDA current consumption: [10 ; 300] mA TID-test bias: 3.3V
6	VSSA	GND	Analogue ground (0V) paired with pin 5 (VDDA)	All VSSA pins are connected. Overall VSSA current consumption: [10 ; 300] mA TID-test bias: 0V
7	INp	AI	ADC differential voltage input (plus terminal)	Amplitude (differential): 2Vpp Common mode (also TID test bias): 0.9V / [0; 1.8] V Signal bandwidth: [0.1; 5] MHz Equivalent input impedance (differential): 350Ω (WC)
8	INm	AI	ADC differential voltage input (minus terminal)	See pin 7 (INp).
9	VSSA	GND	Analogue ground (0V) paired with pin 10 (VDDA)	See pin 6.
10	VDDA	PWR	Analogue supply (3.3V) paired with pin 9 (VSSA)	See pin 5.
11	TEST_A	AO	Analogue test bus output	Voltage range: [0 ; 1.8] V Signal bandwidth: DC Output impedance (single-ended): Low Idle state: Open circuit. TID test bias: NC
12	BTST_50uA	AI	Bias input of the output buffer of the analogue test bus	50µA sink DC current (also TID test bias) Input impedance: Low Expected DC voltage : ~712mV Idle state (ordered by preference): Connected to ground / Open circuit

#	Name	Type	Functionality	Additional Information
13	VDDC	PWR	Core supply (1.8V) paired with pin 14 (VSSC)	Direct access to the core power supply net for test purpose. Idle state: Open circuit. TID test bias: NC
14	VSSC	GND	Core ground (0V) paired with pin 13 (VDDC)	Direct access to the core ground net for test purpose. Idle state: Open circuit. TID test bias: NC
15	ID2	DI	Chip ID port (bit 2)	DC 3.3V CMOS TID-test bias: 0V (proposed value, it could also be 3.3V)
16	VSSA	GND	Analogue ground (0V) paired with pin 17 (VDDA)	See pin 6.
17	VDDA	PWR	Analogue supply (3.3V) paired with pin 16 (VSSA)	See pin 5.
18	ID1	DI	Chip ID port (bit 1)	DC 3.3V CMOS TID-test bias: 0V (proposed value, it could also be 3.3V)
19	ID0	DI	Chip ID port (bit 0)	DC 3.3V CMOS TID-test bias: 0V (proposed value, it could also be 3.3V)
20	RST	DI	Asynchronous reset	3.3V CMOS @10MHz (maximum) TID test bias: 3.3V
21	CS	DI	SPI chip select	3.3V CMOS @10MHz (maximum) TID test bias: 3.3V
22	SCLK	DI	SPI clock	3.3V CMOS @10MHz (maximum) Duty cycle: 50% TID test bias: 0V
23	MOSI	DI	SPI Master Output Slave Input	3.3V CMOS @10MHz (maximum) TID test bias: 0V
24	MISO	DO	SPI Master Input Slave Output	3.3V CMOS @10MHz (maximum) TID test bias: NC
25	VDDD	PWR	Digital supply (3.3V) paired with pin 26 (VSSD)	All VDDD pins are connected. Overall VDDD current consumption: [6 ; 60] mA TID test bias: 3.3V
26	VSSD	GND	Digital ground (0V) paired with pin 25 (VDDD).	All VSSD pins are connected. Overall VSSD current consumption: [6 ; 60] mA TID test bias: 0V
27	D19	DO	ADC outcode (bit19)	3.3V CMOS @40MHz (maximum) TID test bias: NC

#	Name	Type	Functionality	Additional Information
28	D18	DO	ADC outcode (bit18)	3.3V CMOS @40MHz (maximum) TID test bias: NC
29	D17	DO	ADC outcode (bit17)	3.3V CMOS @40MHz (maximum) TID test bias: NC
30	D16	DO	ADC outcode (bit16)	3.3V CMOS @40MHz (maximum) TID test bias: NC
31	D15	DO	ADC outcode (bit15)	3.3V CMOS @40MHz (maximum) TID test bias: NC
32	VDDD	PWR	Digital supply (3.3V) paired with pin 33 (VSSD)	See pin 25.
33	VSSD	GND	Digital ground (0V) paired with pin 32 (VDDD)	See pin 26.
34	D14	DO	ADC outcode (bit14)	3.3V CMOS @40MHz (maximum) TID test bias: NC
35	D13	DO	ADC outcode (bit13)	3.3V CMOS @40MHz (maximum) TID test bias: NC
36	D12	DO	ADC outcode (bit12)	3.3V CMOS @40MHz (maximum) TID test bias: NC
37	VSSD	GND	Digital ground (0V) paired with pin 38 (VDDD)	See pin 26.
38	VDDD	PWR	Digital supply (3.3V) paired with pin 37 (VSSD)	See pin 25.
39	D11	DO	ADC outcode (bit11)	3.3V CMOS @40MHz (maximum) TID test bias: NC
40	D10	DO	ADC outcode (bit10)	3.3V CMOS @40MHz (maximum) TID test bias: NC
41	D9	DO	ADC outcode (bit9)	3.3V CMOS @40MHz (maximum) TID test bias: NC
42	D8	DO	ADC outcode (bit8)	3.3V CMOS @40MHz (maximum) TID test bias: NC
43	VDDD	PWR	Digital supply (3.3V) paired with pin 44 (VSSD)	See pin 25.
44	VSSD	GND	Digital ground (0V) paired with pin 43 (VDDD)	See pin 26.
45	D7	DO	ADC outcode (bit7)	3.3V CMOS @40MHz (maximum) TID test bias: NC
46	D6	DO	ADC outcode (bit6)	3.3V CMOS @40MHz (maximum) TID test bias: NC

#	Name	Type	Functionality	Additional Information
47	D5	DO	ADC outcode (bit5)	3.3V CMOS @40MHz (maximum) TID test bias: NC
48	VDDD	PWR	Digital supply (3.3V) paired with pin 49 (VSSD)	See pin 25.
49	VSSD	GND	Digital ground (0V) paired with pin 48 (VDDD)	See pin 26.
50	D4	DO	ADC outcode (bit4)	3.3V CMOS @40MHz (maximum) TID test bias: NC
51	D3	DO	ADC outcode (bit3)	3.3V CMOS @40MHz (maximum) TID test bias: NC
52	D2	DO	ADC outcode (bit2)	3.3V CMOS @40MHz (maximum) TID test bias: NC
53	D1	DO	ADC outcode (bit1)	3.3V CMOS @40MHz (maximum) TID test bias: NC
54	D0	DO	ADC outcode (bit0)	3.3V CMOS @40MHz (maximum) TID test bias: NC
55	VDDD	PWR	Digital supply (3.3V) paired with pin 56 (VSSD)	See pin 25.
56	VSSD	GND	Digital ground (0V) paired with pin 55 (VDDD).	See pin 26.
57	D_READY	DO	ADC outcode data ready	3.3V CMOS @40MHz (maximum) TID test bias: NC
58	VSSD	GND	Digital ground (0V) unpaired	See pin 26.
59	CLK	DI	ADC sampling clock	3.3V CMOS @160MHz (maximum) Jitter: <30ps Duty cycle: 50% Possible values: 13.6, 21.76, 29.92, 34.5 39.44, 46, 57.5, 69, 80.5, 92, 103.5, 115, 126.5, 138, 149.5, 161 MHz TID test bias: 0V
60	VSSD	GND	Digital ground (0V) paired with pin 61 (VDDD)	See pin 26.
61	VDDD	PWR	Digital supply (3.3V) paired with pin 60 (VSSD)	See pin 25.
62	BIAS_50uA	AI	Bias for the ADC analogue core	50µA sink DC current (also TID test bias) Input impedance: Low Expected DC voltage: ~780mV

#	Name	Type	Functionality	Additional Information
63	REF_SW	AI	Common mode reference	0.9V DC voltage (also TID test bias) DC/rms current compliance: [0.06 ; 2.1] / [3.5; 30.6] mA Input impedance: low
64	VDDA	PWR	Analogue supply (3.3V) paired with pin 1 (VSSA)	See pin 5.

Table 2: Pinout Description

SPI interface

ARQ-CVB001 is programmed through a standard SPI interface. The SPI block can send parameters and obtain information from the different analog blocks in the ASIC. Analogue blocks are arranged in a bus configuration. APB bus is used, where SPI block is the bus master and each analogue block is a bus slave (see Figure 1).

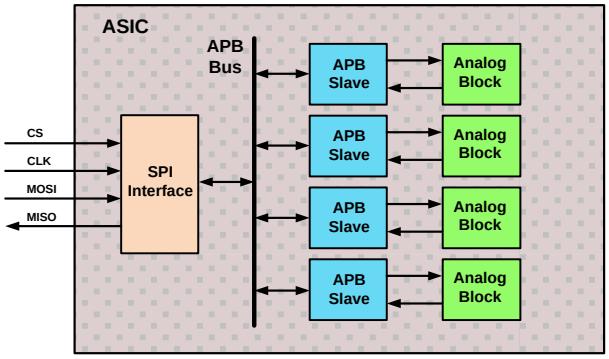


Figure 1: SPI interface

SPI protocol

The protocol complies with the SPI standard with the modes and variants defined below, and it has the following characteristics.

- The communications protocol is a master-slave oriented protocol where the ASIC assumes the slave role. Transmission is full-duplex. When the master is transmitting a data packet the ASIC sends back a return packet simultaneously.
- All data transmissions are arranged in transfers, involving a command from the master and a response from the ASIC. Only the master can start a transfer.
- The packets being transmitted are fixed in length.
- The packets include a parity bit. Any packet arriving with an improper parity bit is discarded.

SPI physical layer

The communications interface physically offers the following four-wire interface, as seen in Figure 1. This interface complies with SPI bus mode 3 (CPOL = 1, CPHA = 1).

- SCLK: the communications interface is synchronous, using a clock signal to synchronize data bits and event execution. The maximum clock frequency is 10MHz. Please note the inverted clock polarity (CPOL = 1) and that the trailing (even) edges of the CLK signal (CPHA = 1) define the bit sampling points.
- MOSI (Master Output Slave Input): through this data line, the ASIC receives the information sent by the master.
- MISO (Master Input Slave Output): through this data line, the ASIC sends information to the master.
- CS: This data line will be set low by the master to initiate a transfer.

SPI chronogram

The sequence for a 5-bit packet SPI transmission is shown in the chronogram of Figure 2.

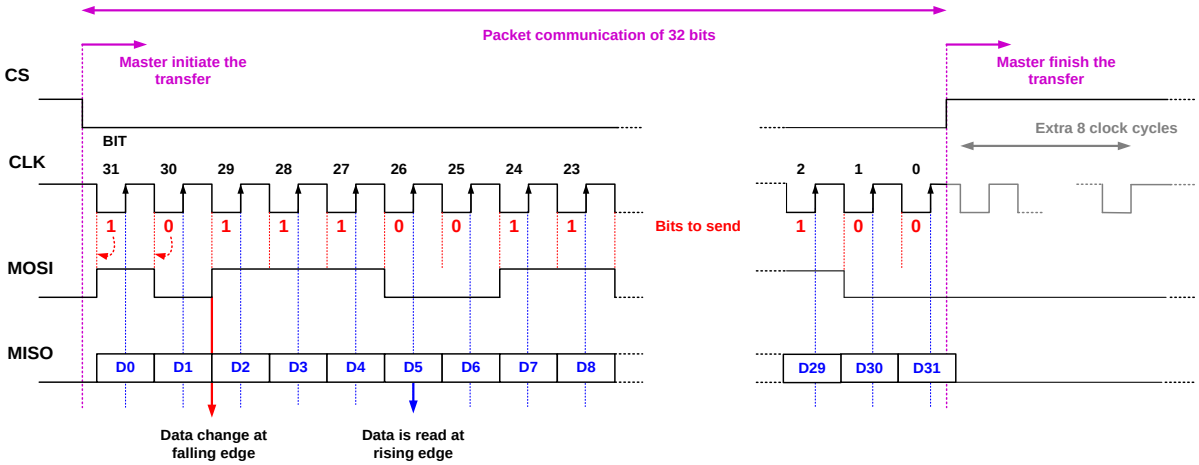


Figure 2: Chronogram for SPI packet transfer

Once a packet has been correctly transmitted and checked, the SPI block will send the required information to the corresponding analog block. It is required to send some Clock pulses after every SPI transmission so that the slave circuits can process the incoming packet information. Although in the general case (writing configuration information) only 3 clock pulses are required, it is highly recommended to use 8 clock cycles to cover all possible cases.

SPI frame composition

The packet format is represented in Figure 3: SPI frame distribution. The packet consist of 32 bits and the transmission is full-duplex. The first line is transmitted from SPI master to SPI slave (ASIC), and the second line is the simultaneous transmission from slave to master.

The packet is transmitted starting with MSB and ending with LSB. In Figure 3: SPI frame distribution, bit 31 is transmitted first, and it is considered the most significant bit of the Chip ID field.

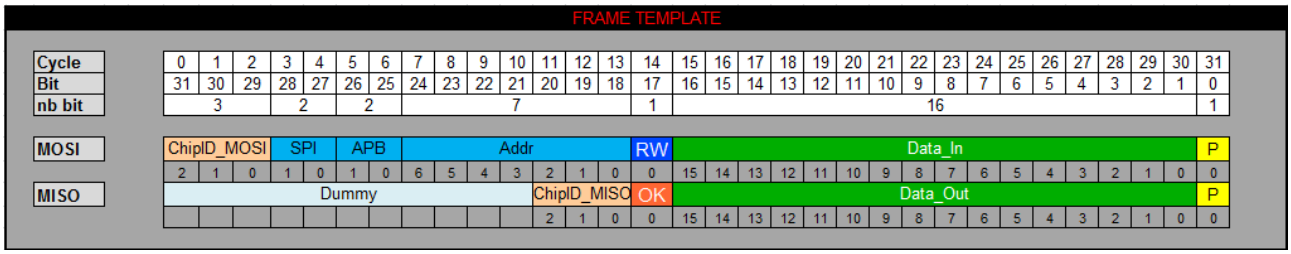


Figure 3: SPI frame distribution

ChipID_MOSI (MOSI 31...29, 3 bits):

Every ASIC has three input pins forming a three bit identification code. The code in the ASIC pins must match the code sent in the packet for the ASIC to attend the packet information. If they do not match, the packet is ignored.
The Chip identification (ChipID port) is handled and hardware programmed through ID{0;1;2} Input Pins.

SPI Address (MOSI 28...18, 11 bits):

The address identification is composed by the 3 following fields:

- SPI (2 bits): Identifies one of the four different SPI blocks that an ASIC may have and allows the selection of the Test Vehicle.
- APB (2 bits): Identifies one of the four APB block inside an SPI block and allows the selection of the sub block
- Addr (7 bits): Identifies one of the 128 internal registers inside an APB block and allows the selection of a specific data byte/register

RW Read-Write (MOSI 17, 1 bit):

It indicates whether a write operation (RW=1) is performed or not (RW=0). A read operation is always performed.

Data_In (MOSI 16...1, 16 bits):

If a write operation is indicated by RW, Data field is written into the register pointed by the Address field.

P Even Parity bit (MOSI & MISO 0, 1 bit):

The packet uses even parity, so that the parity bit is set to 1 if the number of ones in the packet (not including the parity bit) is odd, making the number of ones in the entire packet (including the parity bit) even.

Dummy (MISO 31...21, 11 bits):

Data to discard

ChipID_MISO (MISO 20…18, 3 bits):

The ChipID of the chip responding to the packet

OK Flag (MISO 17, 1 bit):

It is set if the previous packet parity bit was correct, and thus the previous packet was processed. Note that it is not related to the packet currently being transmitted, as it has not completely arrived.

Data_Out (MISO 16...1, 16 bits):

Content of the register pointed by the Address field of the current master to slave packet, which has already arrived

Memory map

ARQ-CVB001 is configurable through different dedicated registers as depicted in the table below:

- SPI, #APB and Addr form the Address.
- Access is the access capability of the corresponding register (RW is read-write, R is read-only, W is write-only).
- #Bits is the field length, in bits.
- High / Low are the higher and lower bits of the field in the 16 bit word.
- Reset is the initial value of the field.

Module Controlled block	Address			Access	Data					
	SPI (2bXX)	APB (2bXX)	Addr (2hXX)	Read / Write	# bits	High	Low	Reset	Register name	Description
DIG GEN Test bus / ADC / REGs	00	00	00	RW	4	3	0	0x0/0xF	rega_off	Power-off the regulators dedicated to the analogue core.
				RW	3	6	4	0x0/0x7	regd_off	Power-off the regulators dedicated to the digital core.
				RW	9	15	7	0x000/0x1FF	Not used	Spare bits
			01	RW	5	4	0	0x00/0x1F	ADCconfig	ADC mode configuration
				RW	1	5	5	0/1	ADCstandby	ADC standby
				RW	10	15	6	0x000/0x3FF	Not used	Spare bits
			02	RW	4	3	0	0x0/0xF	testbus_sel	Analogue test bus: channel selection
				RW	1	4	4	0/1	testbus_mux_en	Analogue test bus: multiplexer enable
				RW	1	5	5	0/1	testbus_buf_en	Analogue test bus: buffer enable
				RW	10	15	6	0x000/0x3FF	Not used	Spare bits
			03	RW	16	15	0	0x0000/0xFFFF	Not used	Spare bits

Table 3: Memory map

SPI detailed frames

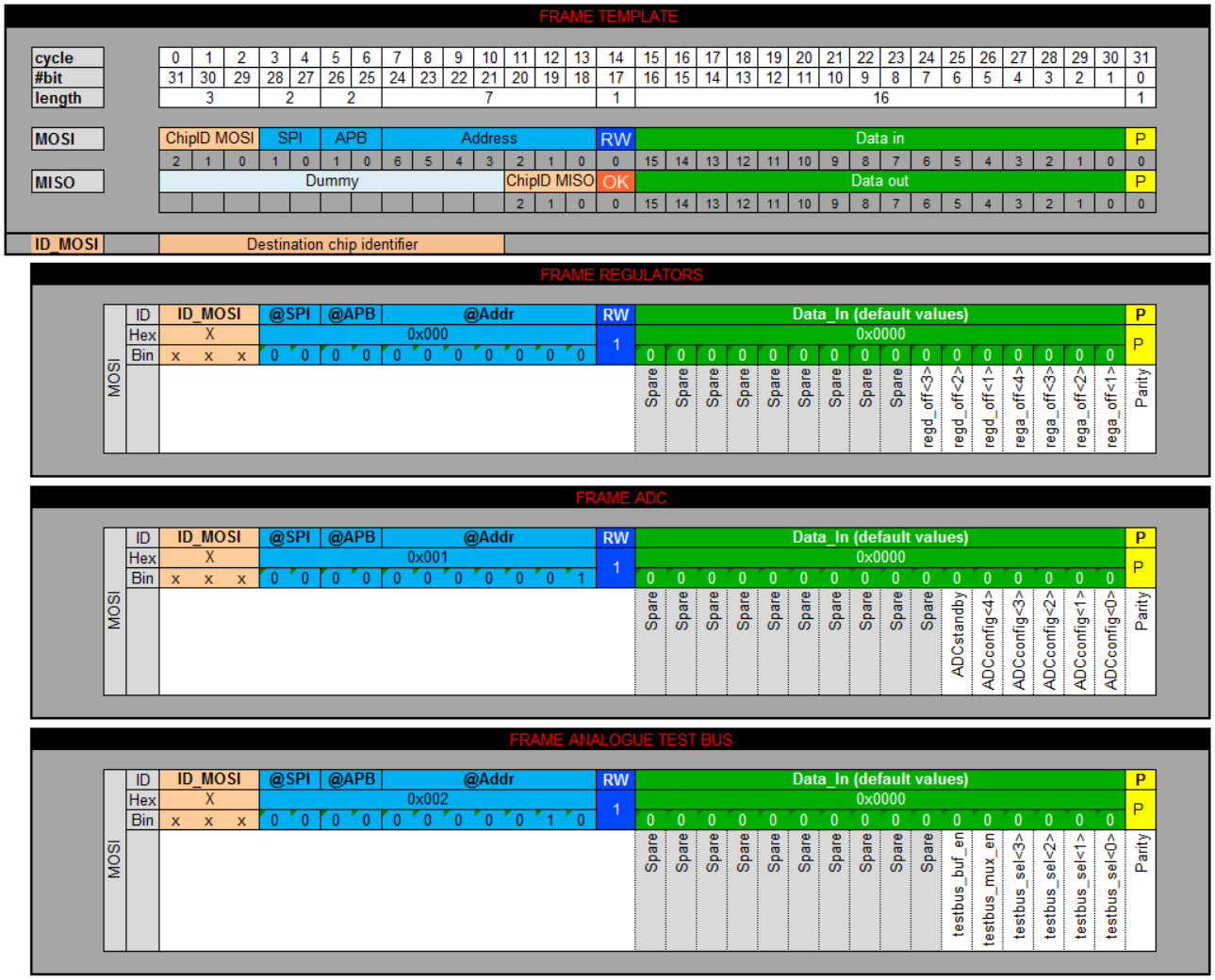


Figure 4: SPI configuration frames

Functional description

The ΣΔ modulator has five operation modes set trough SPI (named Config ADC X, where X is a number from 1 to 5) depending on the bandwidth of the input signal INp/Inm. The sampling rate is set by the frequency of signal CLK.

Depending on the operation mode, the output frame obtained at D has to be decoded differently. In Config ADC 1, 2 and 3 the output frame is obtained from single-bit quantizers; by the other hand, in Config ADC 4 and 5 the output frame is obtained from 5-bits quantizers. Hence, in operation modes 1, 2 and 3 the output frame is composed by 20 samples and in operation modes 4 and 5 it is composed by 4 samples. As a rule of thumb, the oldest sample is located in the MSB(s) while the newest is on the LSB(s). To avoid injecting noise to the system, the outcode obtained in D is updated at once; the rising edge of signal D_ready states the correct instant to sample D. A more detailed distribution of the data inside the output frame is depicted in Figure 5.

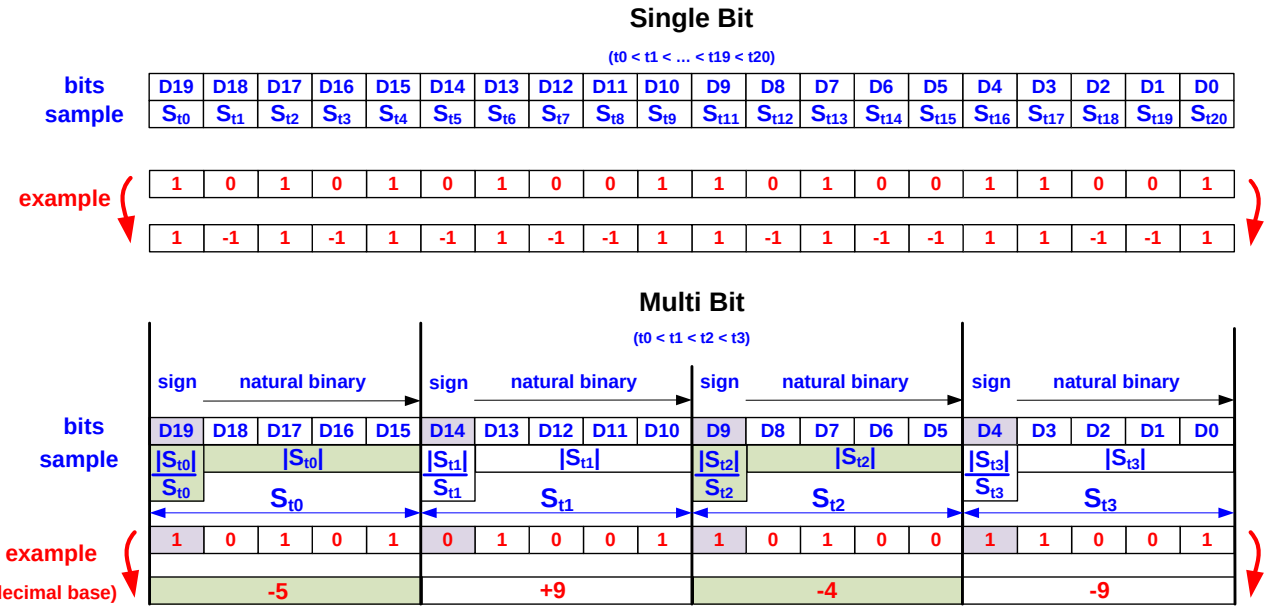


Figure 5: Output frame distribution at D

For all the Config ADC modes, the following input ports should be set:

- **REF_BOOT**: Bootstrap reference. Set as stated in Table 2.
- **REF_DAC**: Internal DAC reference. Set as stated in Table 2.
- **REF_IN**: Common mode reference. Set as stated in Table 2.
- **REF_SW**: Common mode reference. Set as stated in Table 2.
- **BIAS_50uA**: Bias for the ADC analogue core. Set as stated in Table 2.
- **INp** and **INm**: ADC differential voltage input (plus and minus terminals). Set as stated in Table 2.

ARQ-CVB001 allows monitoring internal signals through port TEST_A. There are 6 possible test modes (named Config Testbus X, where X is a number from 1 to 6) compatible with all the Config ADC modes. The internal signal to be monitored at TEST_A is selected through SPI. A voltage buffer is available to avoid loading this internal net. In case that the voltage buffer is enabled, the following signal has to be set:

- **BTST_50uA**: Bias current of the output buffer. Set as stated in Table 2.

Operational modes

The following test cases could be simulated. $SDNR_{max}$ and $SNDR_{-3dBFS}$ are the expected values.

Test case	Nyquist freq. [MHz]	Sampling clock [MHz]	$SDNR_{max}$ [ENOB]	$SNDR_{-3dBFS}$ [ENOB]	Config ADC #
T1	0.1	13.60	18.00	18.8	1
T2	0.16	21.76	17.40	18.4	1
T3	0.22	29.92	16.80	12.8	1
T4	0.29	39.44	16.63	7.3	1
T5	0.35	69.0	16.36	13.7	2
T6	0.42	80.5	16.13	14.1	2
T7	0.49	92.0	15.93	14.4	3
T8	0.56	103.5	15.75	15.0	3
T9	0.64	115.0	15.59	13.9	3
T10	0.71	126.5	15.45	13.3	3
T11	0.78	138.0	15.32	12.3	3
T12	0.86	149.5	15.20	11.4	3
T13	0.93	161.0	15.09	11.0	3
T14	1.28	23.0	14.52	14.1	4
T15	2.00	34.5	14.43	14.5	4
T16	2.74	46.0	14.34	13.2	4
T17	3.51	57.5	14.13	13.5	4
T18	4.28	69.0	13.95	13.7	5
T19	5.07	80.5	13.81	13.8	5
T20	5.87	92.0	13.68	13.3	5
T21	6.68	103.5	13.57	13.7	5
T22	7.5	115	13.47	11.4	5
T23	8.33	126.5	13.38	7.8	5
T24	9.16	138	13.29	7.8	5
T25	10	149.5	13.22	7.1	5

Table 4: examples of possible test cases

Config ADC 1

Signal Inp/Inm bandwidth: [0.05 ; 0.145) MHz

Signal CLK range: [13.6 ; 39.44) MHz

Output frame: D is a stream of 20 single-bit conversions, where its MSB is the oldest data and its LSB is the newest. D post-processing is required to obtain the conversion with the effective number of bits.

Configuration registers:

- **regd_off**: Output data packer and digital core are supplied with one regulator each (maximum current consumption: 15mA each). Possible values: **3b100**, **3b001**.
- **rega_off**: Analogue core is supplied with one regulator (maximum current consumption: 60mA). Possible values: **4b1110**, **4b1101**, **4b1011**, **4b0111**.
- **ADCstandby**: ADC enabled. Value: **1b0.**
- **ADCconfig**: LSSB modulator active. Value: **5b00000**.

Config ADC 2

Signal Inp/Inm bandwidth: [0.175 ; 0.21) MHz

Signal CLK range: [69.0 ; 80.50) MHz

Output frame: D is a stream of 20 single-bit conversions, where its MSB is the oldest data and its LSB is the newest. D post-processing is required to obtain the conversion with the effective number of bits.

Configuration registers:

- **regd_off**: Output data packer is supplied with one regulator whereas the digital core is supplied with two regulators (maximum current consumption: 15mA each). Possible value: **3b000**.
- **rega_off**: Analogue core is supplied with two regulators (maximum current consumption: 60mA each). Possible values: **4b1100**, **4b1010**, **4b1001**, **4b0110, 4b0101, 4b0011**
- **ADCstandby**: ADC enabled. Value: **1b0**
- **ADCconfig**: HSSB modulator active for low input bandwidth. Value: **5b00100**

Config ADC 3

Signal Inp/Inm bandwidth: [0.245 ; 0.465) MHz

Signal CLK range: [92.00 ; 161.0) MHz

Output frame: D is a stream of 20 single-bit conversions, where its MSB is the oldest data and its LSB is the newest. D post-processing is required to obtain the conversion with the effective number of bits.

Configuration registers:

- **regd_off**: Output data packer is supplied with one regulator whereas the digital core is supplied with two regulators (maximum current consumption: 15mA each). Possible value: **3b000**.
- **rega_off:** Analogue core is supplied with two regulators (maximum current consumption: 60mA each). Possible values: **4b1100**, **4b1010**, **4b1001**, **4b0110, 4b0101, 4b0011**
- **ADCstandby**: ADC enabled. Value: **1b0**
- **ADCconfig**: HSSB modulator active for high input bandwidth. Value: **5b00101**

Config ADC 4

Signal Inp/Inm bandwidth: [0.64 ; 1.755) MHz

Signal CLK range: [23.0 ; 57.50) MHz

Output frame: D is the stream of four 5-bits conversions, where its 5 MSBs are the oldest data and its 5 LSBs are the newest. D post-processing is required to obtain the conversion with the effective number of bits.

Configuration registers:

- **regd_off**: Output data packer is supplied with one regulator whereas the digital core is supplied with two regulators (maximum current consumption: 15mA each). Possible value: **3b000**
- **rega_off:** Analogue core is supplied with two regulators (maximum current consumption: 60mA each). Possible values: **4b1100**, **4b1010**, **4b1001**, **4b0110, 4b0101, 4b0011**
- **ADCstandby**: ADC enabled. Value: **1b0**
- **ADCconfig**: LSMB modulator active. Value with active DEM: **5b01000.** Value with disable DEM: **5b11000**

Config ADC 5

Signal Inp/Inm bandwidth: [2.14 5.000) MHz

Signal CLK range: [69.0 149.5) MHz

Output frame: D is the stream of four 5-bits conversions, where its 5 MSBs are the oldest data and its 5 LSBs are the newest. D post-processing is required to obtain the conversion with the effective number of bits.

Configuration registers:

- **regd_off**: Output data packer is supplied with one regulator whereas the digital core is supplied with two regulators (maximum current consumption: 15mA each). Possible value: **3b000**.
- **rega_off**: Analogue core is supplied with four regulators (maximum current consumption: 60mA each). Possible value: **4b0000**
- **ADCstandby**: ADC enabled. Value: **1b0**
- **ADCconfig**: HSMB modulator active. Value with active DEM: **5b01100.** Value with disable DEM: **5b11100**

Config Testbus 1 (vdda0@TEST_A)

TEST_A: The 1.8V supply voltage for common blocks is measured through the test output.

Configuration registers:

- **testbus_buf_en**: enables a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**
- **testbus_sel:** selects the proper signal to measure. Value: **4b0000**

Config Testbus 2 (vdda1@TEST_A)

TEST_A: the 1.8V supply voltage for the modulators is measured through the test output.

Configuration registers:

- **testbus_buf_en**: enables a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**

- **testbus_sel:** selects the proper signal to measure. Value: **4b0001**

Config Testbus 3 (vddd1@TEST_A)

TEST_A: the 1.8V supply voltage for the digital core is measured through the test output.

Configuration registers:

- **testbus_buf_en**: enables a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**
- **testbus_sel:** selection of the proper signal to measure. Value: **4b0010**

Config Testbus 4 (vddd2@TEST_A)

TEST_A: the 1.8V supply voltage for the digital output data packer is mea sured through the test output.

Configuration registers:

- **testbus_buf_en**: enable a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**
- **testbus_sel:** selects the proper signal to measure. Value: **4b0011**

Config Testbus 5 (BG@TEST_A)

TEST_A: the 1.25V bandgap voltage is measured through the test output.

Configuration registers:

- **testbus_buf_en**: enable a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**
- **testbus_sel:** selects the proper signal to measure. Value: **4b0100**

Config Testbus 6 (vssa0@TEST_A)

TEST_A: the 0V ground signal is brought by a tie-down and measured through the test output.

Configuration registers:

- **testbus_buf_en**: enables a voltage buffer to avoid loading the internal net. Possible values: ~~1b0~~ (disabled, not allowed), **1b1** (enabled). Due to a bug in the design, the voltage buffer shall be always enabled (when disabled, its bias circuit consumes around 2mA due to a design bug).
- **testbus_mux_en**: enables the supply of the test-bus multiplexer. Value: **1b1**
- **testbus_sel:** selects the proper signal to measure. Possible values: **4b0101, 4b0110, 4b0111, 4b1000, 4b1001, 4b1010, 4b1011, 4b1100, 4b1101, 4b1110, 4b1111**

Implementation recommendations

A recommended implementation is shown in Figure 6 where some elements are required.

- Voltage DC sources for power supplies, common mode and reference voltage
- Current DC sources for biasing the analogue core circuits and the test output buffer
- Sinusoidal voltage generator for differential input ports
- Square voltage generator for clock input port
- A SPI master block
- A digital circuitry for post processing the output data stream

Supply/Ground Planes

When powering ARQ-CVB001, it is recommended to use two separate power domains: one for the analogue signals (VDDA) and another for the digital ones (VDDD). Although SPI signals have digital nature, they have been placed in the analogue IO power domain to isolate configuration registers from the noise generated by the fast digital output D. Hence VDDD power domain goes from ports 25 to 61, while the rest of ports belong to VDDA power domain.

For better performances, a couple of ground/power planes should be dedicated to each power domain and connected together in a single point below the component. With proper decoupling and smart partitioning of the PCB analogue, digital, and clock sections, optimum performance can be easily achieved.

Routing

Critical paths must be shielded.
Differential paths must be equalized.

Power decoupling

For both power domains, several decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of ARQ-CVB001, with minimal trace length.

Reference Decoupling

The voltage reference pins should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 100 nF ceramic capacitor as near as possible of the Ref pins.
Inductance parasitic must be minimized (<3nH from die pad).

Clock jitter

The quality of the time base is critical at the input sampler of the ΣΔ modulator, where the continuous-to-discrete time transformation is performed. The effect of the clock phase noise can be understood as a non-uniform sampling, whose equivalent signal error is proportional to the input frequency and also to the input amplitude itself. This later dependency tends to saturate the SNR curve when the jitter effect is dominant. In fact, the jitter requirements are stronger for multi bit systems than for single bit systems. A maximum jitter allowed for the external master clock should be $40ps_{rms}$

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the blocks is required. Because the SCLK, CS, and MOSI signals are typically asynchronous to the block clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and ARQ-CVB001 to keep these signals from transitioning at the device inputs during critical operating mode.

As SPI input ports are placed in the IO analogue domain, in order to avoid the noise coming from IO digital domain, another recommendation is to keep the input digital signals through SPI input ports in the analogue domain considering analogue power supply and ground (see Supply/Ground Planes recommendation above).

ESD caution

Dies are very sensitive to electrostatic discharge from other bodies or surfaces at different potentials. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. The ESD robustness of a design depends on the I/O configuration as well.

Thermal dissipation

Airflow increases heat dissipation, effectively reducing the thermal resistance. Also, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the thermal resistance. It is required that the exposed heat sink is soldered to the ground planes.

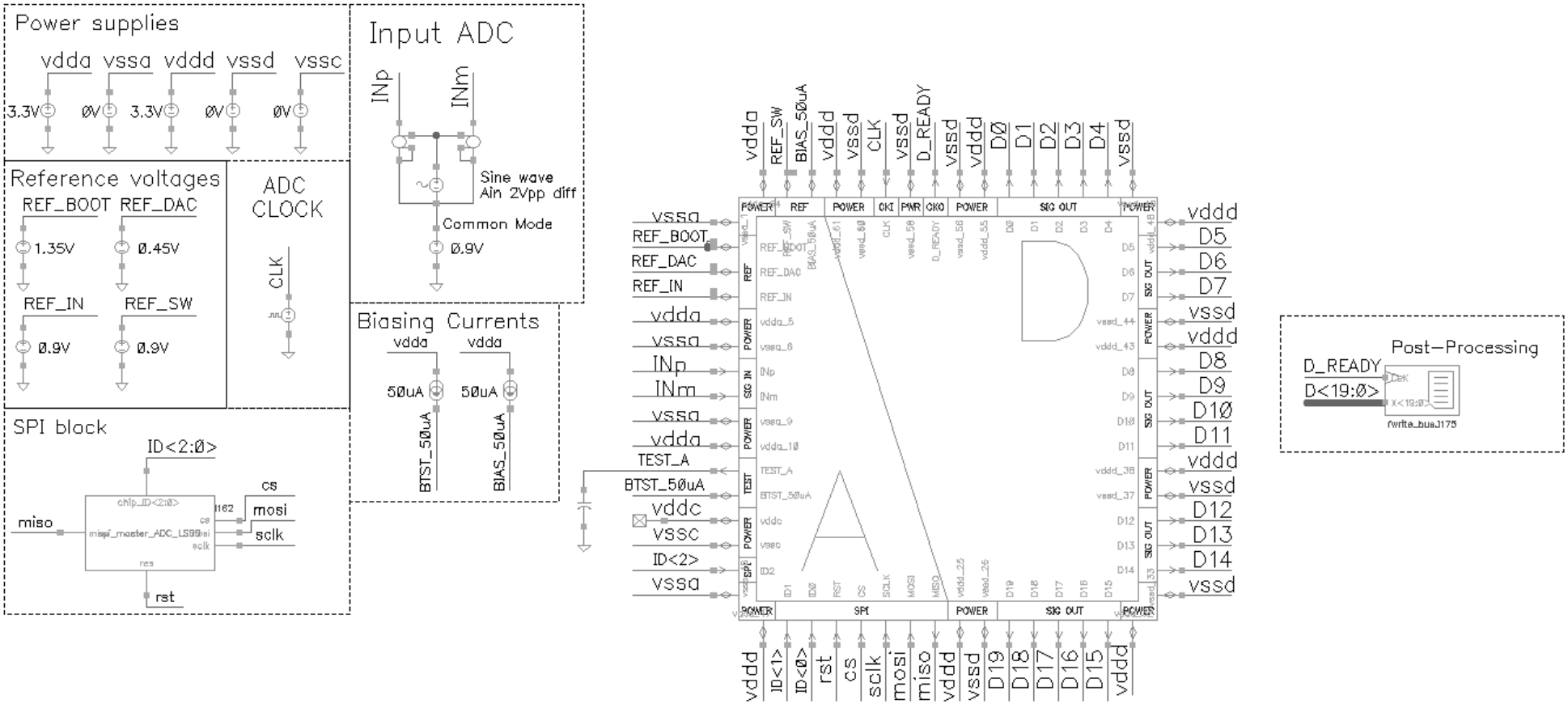


Figure 6: ADC test implementation

Electrical characteristics

General considerations

Description	Symbol	Maximum rating	Units	Recommended
Supply Voltage	VDDD VDDA	4.5	V	Operating from 2.97V to 3.63V Nominal Values 0V, 3.3V
Input Voltage	Vin	-0.5 to VDD + 0.5	V	VDD rating should not be exceeded
ESD	V_{HBM}	2000	V	

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog IO Pads

Pad name	Imax (≤85º)	Imax (≤125º)	Imax (≤145º)	Unit
OANALOG	70	23	14	mA
IANALOG	8.5	2.8	1.7	mA
GNDA33PAD	475	158	95	mA
VDDA33PAD	470	158	95	mA

Table 6: Analog IOPAD electrical characteristics

Digital IO Pads

I/O pad Parameters								
	Symbol	Parameter	Description	Test Conditions	Limites HF			
					Min	typ	Max	Unit
Parametric	IIL	Input Leakage Current at low state	Input current which should be as lower as possible (few uA) in both states of the Input Voltage.	VCC= Max Voltage (WC)			1	uA
	IIH	Input Leakage Current at High state	Input current which should be as lower as possible (few uA) in both states of the Input Voltage.	VCC= Max Voltage (WC)			1	uA

I/O pad Parameters								
	VIH	Input High Voltage	The VIL/VIH test guarantees that the input pins can correctly sense the proper logic states when the VIL/VIH voltages are applied. VIH (Voltage Input High) represents the worst-case voltage applied to an input to represent a logic 1. VIH should be tested at VCCmax to be in WC condition.	VCC= Max Voltage (WC)	2			V
	VIL	Input Low Voltage	The VIL/VIH test guarantees that the input pins can correctly sense the proper logic states when the VIL/VIH voltages are applied. VIL (Voltage Input Low) represents the worst-case voltage applied to an input to represent a logic 0. VIL should be tested at VCCmin to be in WC condition.	VCC= Min Voltage (WC)			0.99	V
	VOL	Output Voltage Current at low state	The VOL test verifies the resistance of output pins while driving valid output levels under a current load. This test ensures that the outputs will provide the specified IOL current while maintaining the correct VOL voltage. VOL (Voltage Output Low) represents the maximum voltage produced by an output when the output is in the low state. VOL is tested with VCC=VCC max (WC condition)	VCC= Min Voltage (WC), Isink= 4 mA			0.352	V
	VOH	Output Voltage Current at High state	The VOH test verifies the resistance of output pins while driving valid output levels under a current load. This test ensures that the outputs will provide the specified IOH current while maintaining the correct VOH voltage. VOH (Voltage Output High) represents the minimum voltage produced by an output when the output is in the high state. VOH is tested with VCC=VCC min (WC condition)	VCC= Min Voltage (WC), Isource=-4 mA	2.49			V
	IOL	Output Low Current	The IOL test verifies the resistance of output pins while driving valid output levels under a current load. This test ensures that the outputs will provide the specified IOL current while maintaining the correct VOL voltage. IOL (current (I) Output Low) represents the current sinking capabilities of an output when the output is in the low state. IOL is tested with VCC=VCC min (WC condition)	VCC= Min Voltage (WC)	4			mA
	IOH	Output High Current	The IOH test verifies the resistance of output pins while driving valid output levels under a current load. This test ensures that the outputs will provide the specified IOH current while maintaining the correct VOH voltage. IOH (current (I) Output High) represents the current sourcing capabilities of an output when the output is in the high state. IOH is tested with VCC=VCC min (WC condition)	VCC= Max Voltage (WC)			-4	mA

Table 7: Digital IOPAD electrical characteristics

ADC performance

Parameter	Value	Unit	Comments
Gain flatness	0.2	dB	From specification. Over the [0.05; 5] MHz signal frequency range.
Gain stability	0.1	dB	From specification. Over the [-10; 85] ^{o}C temperature range.
ENOB	10 6 5.5 5.4	Bits	LSSB in T1 conditions (electrical and temperature measures) HSSB in T5 conditions (electrical measures) LSMB in T14 conditions (simulations) HSMB in T18 conditions (simulations)
THD	62 40 29 28	dB	LSSB in T1 conditions (electrical and temperature measures) HSSB in T5 conditions (electrical measures) LSMB in T14 conditions (simulations) HSMB in T18 conditions (simulations)
SNR	73 44 48 46	dB	LSSB in T1 conditions (electrical and temperature measures) HSSB in T5 conditions (electrical measures) LSMB in T14 conditions (simulations) HSMB in T18 conditions (simulations)
Consumption	10 104 68 270	mA	LSSB in T1 conditions (electrical and temperature measures) HSSB in T5 conditions (simulations) LSMB in T14 conditions (simulations) HSMB in T18 conditions (simulations)

Table 8: ADC electrical parameters

ESD

Dies are very sensitive to electrostatic discharge from other bodies or surfaces at different potentials. In order to prevent damage on the on-chip devices, dedicated ESD discharge paths are implemented inside the I/O pads. These paths prevent that discharge currents flow through high resistive paths in the design which could cause damage on devices due to voltage drops surpassing their junction breakdown voltages.

All 3.3V digital input cells are protected with ESD diodes to the GNDIO and VDDIO tracks. If a fault condition arises in the system a DC current can either flow into or out of the digital input pin. In the first case the pin voltage will increase above the VDDIO level, while in the latter case the input pin is pulled below the GNDIO level. Both situations lead to higher than nominal voltage over the transistor gate oxide.

The pin voltage in function of the current to VDDIO (-) or GNDIO (+) is listed in next table. WC conditions ('fast' process, VDDIO = 3.63 V and T = -55 ˚C) are considered.

Input Current	Input voltage
-20mA	4.458V
-10mA	4.440V
-1mA	4.304V
-500µA	4.259V
-100µA	4.186V

Input Current	Input voltage
-10µA	4.109V
-5µA	4.088V
5µA	-0.434V
10µA	-0.454V
100µA	-0.528V
500µA	-0.590V
1mA	-0.623V
10mA	-0.811V
20mA	-0.844V

Mechanical characteristics

Die size

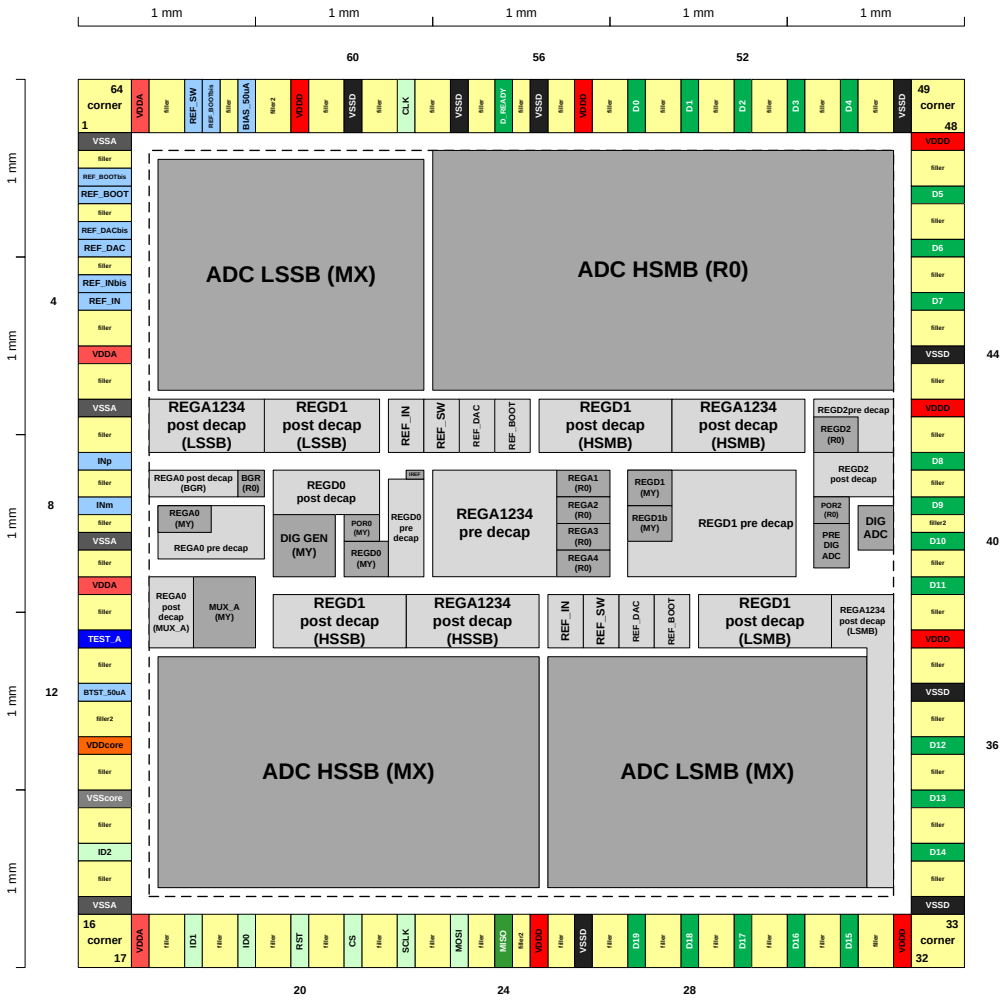


Figure 7: Die/Package Pinout

Legend:

PAD NAME	Analogue input	PAD NAME	Digital input
PAD NAME	Analogue output	PAD NAME	Digital output
PAD NAME	Power for analogue IO	PAD NAME	Power for digital IO
PAD NAME	Ground for analogue IO	PAD NAME	Power for digital IO
FILLER TYPE	Filler or corner		

Thermal Resistance

Parameter	Symbol	Value	Unit	Comments
junction-to-air (still) thermal resistance	θ_{JA}	29	°C/W	
junction-to-case thermal resistance	θ_{JC}	1	°C/W	

Package

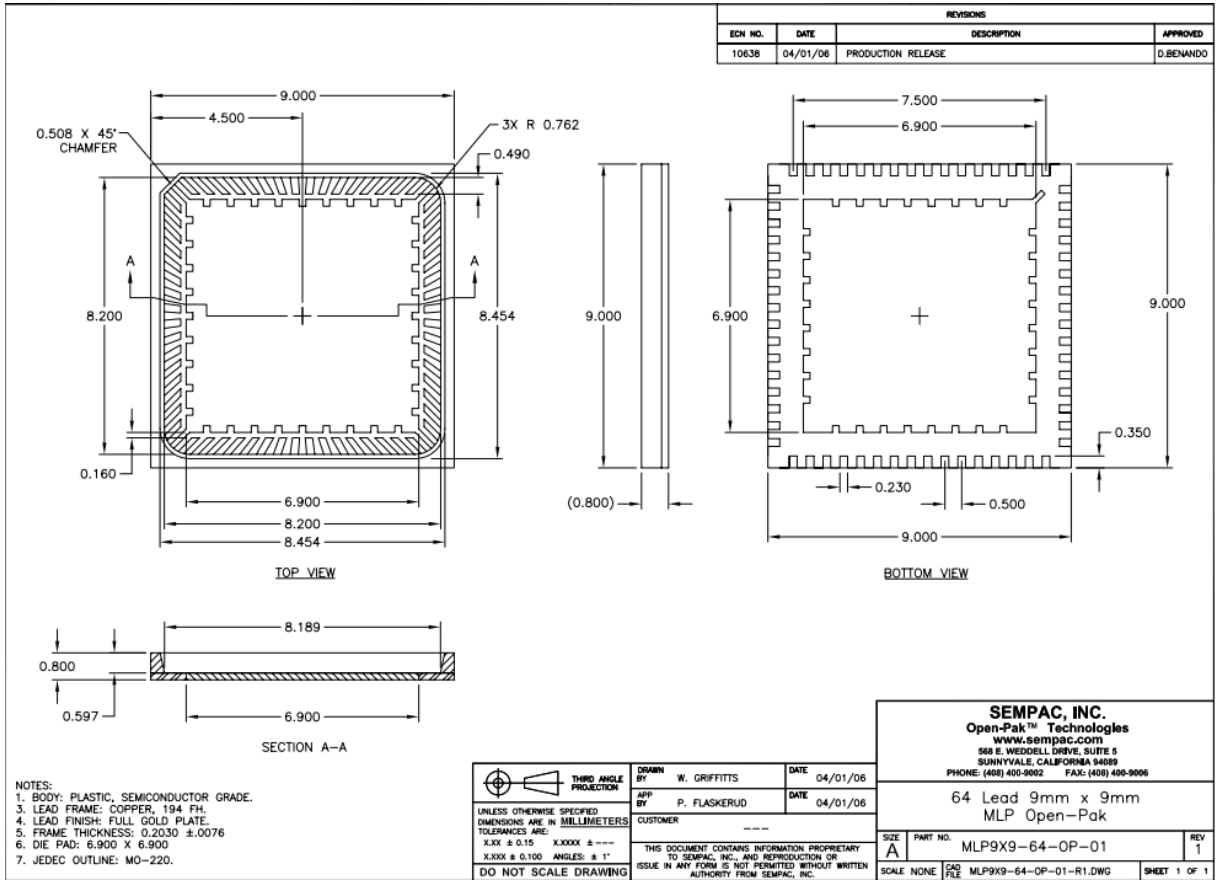


Figure 8: QFN64_9x9 packaging

Bonding diagram

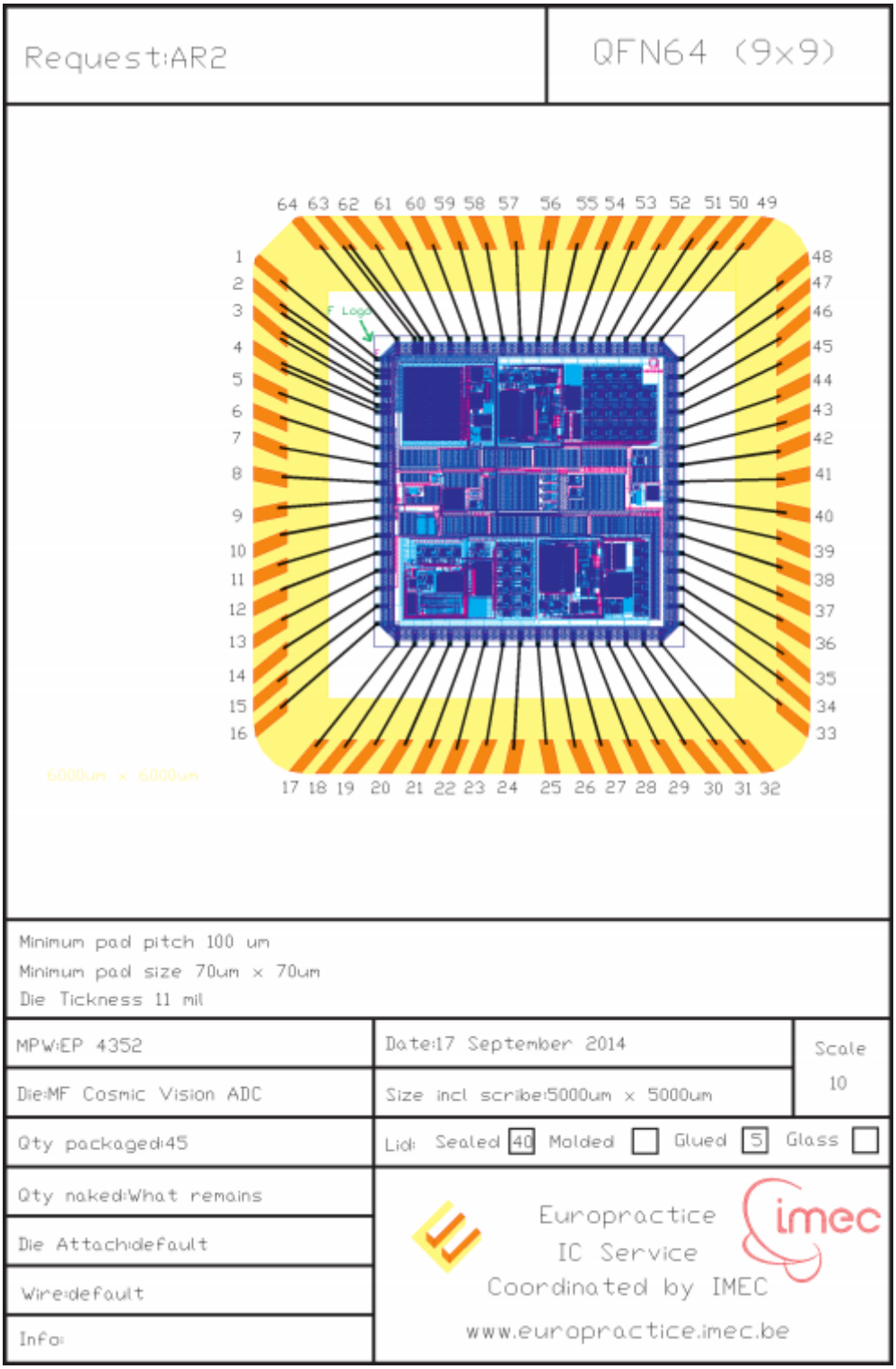


Figure 9: QFN64_9x9 bonding

Environmental conditions

Temperature

Parameter	Symbol	Value (°C)	Comments
Operating	T_{op}	[-10 ; 85]	
Functional	T_{func}	[-55 ; 125]	
Qualified	T_{q}	[-10 ; 110]	
Storage	T_{str}	[-65 ; 150]	
Soldering lead	T_{sol}	300	Not more than 10 seconds.

Table 9: Temperature absolute maximum ratings

Radiation

Parameter	Value	Unit	Additional info
TID	300	Krad	TBC
SEL	80	$MeVcm^2/mg$	TBC
SEE performance	1E-10	Err/Bit/day	For geostationary orbit

More information about radiation hardening features and radiation test conditions is available under request.

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In order to meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in one or more of the following processes:

- Equivalent to QML 38535 LEVEL Q or Level V*
- Equivalent to ESCC 9000 Level C or level B*

For procurement in die form

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

*With Radiation Qualification

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Changes record

Date	Issue	Section	Changes
02-02-2015	Draft A	All	
05-03-2015	Draft B	All	Template modification and information completion.
21-05-2015	Draft C	Functional description	Multibit output frame has inverted signs in Figure 5.
09/06/2015	Draft C	Table 2	TID test bias information included.
30/06/2015	Draft D	Table 2	Typo corrected in expected DC voltage of port 62 (BIAS_50uA).
06/07/2015	Draft D	Table 4	Test cases T22 to T25 have been removed.
07/07/2015	Draft D	Config Testbus 1 (vdda0@TEST_A)	Expected voltage at TEST_A added.
07/07/2015	Draft D	Config Testbus 2 (vdda1@TEST_A)	Expected voltage at TEST_A added.
07/07/2015	Draft D	Config Testbus 3 (vddd1@TEST_A)	Expected voltage at TEST_A added.
07/07/2015	Draft D	Config Testbus 4 (vddd2@TEST_A)	Expected voltage at TEST_A added.
07/07/2015	Draft D	Config Testbus 5 (BG@TEST_A)	Expected voltage at TEST_A added.
07/07/2015	Draft D	Config Testbus 6 (vssa0@TEST_A)	Expected voltage at TEST_A added.
14/10/2015	Draft E	Table 3	Addr 01 and 02 spare bits reset value of the complementary register updated.
15/10/2015	Draft E	Table 4	Moved before the configurations.
26/04/2016	Draft E	Table 2	Pins 2 and 3 typo corrected.
31/08/2016	Issue 1	Table 8	Performance updated with electrical and temperature measurement results.

