ARQ-LVP001

RAD-HARD Octal 500 Mbps Bus LVDS Repeater

FEATURES

- 500.0 Mbps low jitter fully differential data path
- 250 MHz clock channel
- 3.3V power supply
- CMOS/TTL compatible inputs
- Low power consumption
- 24mA output driver short circuit (OUT+, OUT−)
- Cold sparing on all pins
- 3.5ns Propagation delay in temperature range
- Extended LVDS Input Common Mode [-4;5]V
- Receiver input threshold ≤ ± 100 mV
- 25mV (typ.) Input hysteresis
- Fail-safe protection circuit
- Radiation tolerant: 300 Krad(Si)
- Latch-up free up to 60 MeVcm^2/mg
- ESD tolerance: 8KV
- Packaging: 48-pin Ceramic Quad Flat Pack (CQFP)
- ANSI TIA/EIA 644a LVDS Standard Compliant
- Space level

DESCRIPTION

ARQUIMEA's ARQ-LVP001 device is an Octal Bus Repeater for Low Voltage Differential Signals (LVDS) intended for low power and high-speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. LVDS I/O enables high speed data transmission for point-to-point or multi-drop interconnects. This device is designed for use as a high speed differential repeater.

The ARQ-LVP001 is a repeater designed specifically for the bridging of multiple backplanes in a system. The ARQ-LVP001 utilizes low voltage differential signaling to deliver high speed while consuming minimal power with reduced EMI. The ARQ-LVP001 repeats signals between backplanes and accepts or drives signals onto the local bus.

The individual LVDS outputs can be put into Tri-State by use of the enable pins.

All pins have Cold Spare buffers. These buffers will be high impedance when VDD is tied to VSS.

The extended common mode range allows high voltage drops between ground planes without affecting performance.

APPLICATIONS

The ARQ-LVP001 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer (including Clock). Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows isolation of segments or long distance applications.

The intended application of these devices and signaling technique is for both spacewire point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.
The transmission media may be printed-circuit board traces, backplanes, or cables.

RADIATION HARDENING

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
TID	300	-	-	Krad	Only validated on former design ARQ-LVR001
SEL	60	-	-	MeVcm^2/mg	
SEE performance for a GEO orbit	1E-13 TBC	-	-	Err/Bit/day	

More information about radiation hardening features and radiation test conditions is available under request.

AVAILABLE OPTIONS

PRODUCT	QUALITY LEVEL	PACKAGE (*)	OPERATING TEMPERATURE	ORDERING NUMBER	VARIANT DETAIL	TRANSPORT MEDIA
ARQ-LVP001	Standard	48 pin CQFP	-55ºC to 125ºC	ARQ-LVP001-02	Without Fail-Safe	50-pieces tray
ARQ-LVP001	Standard	48 pin CQFP	-55ºC to 125ºC	ARQ-LVP001-03		50-pieces tray
ARQ-LVP001	ESCC9000	48 pin CQFP	-55ºC to 125ºC	ARQ-LVP001S03		50-pieces tray

(*) Other packaging options, including raw die format, are also available under request.

ARQ_12104_DSH_004_Issue_02, Date: 10-09-2017

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GLOSSARY

BER	*Bit Error Ratio*
CMRR	*Common Mode Rejection Ratio*
CQFP	*Ceramic Quad Flat Pack*
ESD	*Electrostatic Discharge*
GEO	*Geostationary Earth Orbit*
IC	*Integrated Circuit*
I/O	*Input/Output*
LET	*Linear Energy Transfer*
LVDS	*Low Voltage Differential Signaling*
LVTTL	*Low Voltage Transistor-Transistor Logic*
PSRR	*Power Supply Rejection Ratio*
RL	*Load Resistor*
SEE	*Single Event Effect*
SEL	*Single Event Latch-up*
TID	*Total Ionizing Dose*
tf	*Fall Time*
tr	*Rise Time*
TTL	*Transistor-Transistor Logic*
VCM	*Common-mode voltage*
VID	*Differential Input Voltage*
VOS	*Offset voltage*
VT	*Differential output voltage*

OVERVIEW

The ARQ-LVP001 provides the basic bus repeater function. The device operates as a 9 channel LVDS buffer.
Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications.
The intended application of these devices and signaling technique is for both point-to-point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media.

BLOCK DIAGRAM

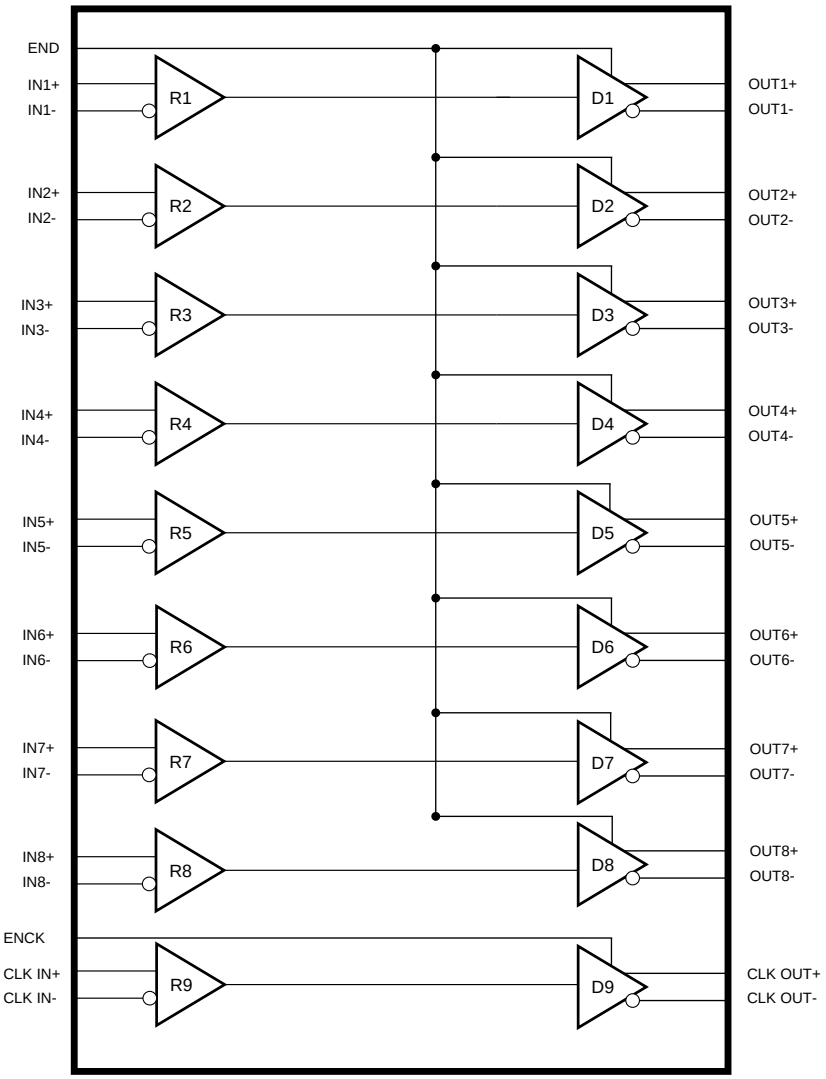

Figure 1: Block diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V_{DD}	DC supply voltage	-0.5 to 4.6V
V_I	TTL/CMOS Input Voltage	-0.5V to 6V
V_{IN}	LVDS Input Voltage	-5V to 6V
T_{STG}	Storage temperature	-65 to +150^{O}C
T_J	Maximum junction temperature	+175^{O}C
Tc	Maximum Case temperature	+125ºC
ESD	ESD Last Passing Voltage – HBM	8kV
P_D	Power dissipation	400mW

Table 1: Absolute Maximum Rating

Note: Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	VALUE
V_{DD}	Power supply voltage	3.0 to 3.6V
V_{IN}	DC input voltage, logic inputs (END or ENCK)	0 to 5V
	DC input voltage, receiver inputs	-4.6V to 5.6V
V_{CM}	LVDS Input Common Mode Voltage	-4V to 5V
T_C	Case temperature range	-55 to +125 ^{O}C

Table 2: Recommended Operating Conditions

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, -55°C < TC < +125°C

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
TTL/CMOS DC SPECIFICATIONS (EN)					
V_{IH}	High-level input voltage		2.0	5V	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
I_{IH}	High-level input current	V_{IN} = 3.6V; V_{DD} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN} = 0V; V_{DD} = 3.6V	-10	+10	µA
I_{CS}	Cold Spare Leakage current	V_{IN} = 3.6V, V_{DD} = V_{SS}	-3,6	+3,6	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)					
V_{OD}	Differential Output Voltage	R_L = 100Ω	247	453	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	R_L = 100Ω		10	mV
V_{OS}	Offset Voltage	R_L = 100Ω $V_{OS} = \frac{V_{OH}+V_{OL}}{2}$	1.125	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	R_L = 100Ω		50	mV
ΔV_{OSB}	Imbalance of Differential Offset Voltage during Voltage transition	R_L = 100Ω, C_L = 1pf		150	mV
I_{OZ}	Output Tri-State Current	Tri-State output (channel disabled), V_{OUT} = V_{DD} or GND	-20	+20	µA
I_{CSOUT}	Cold Sparing Leakage Current	V_{OUT} = 3.6V, V_{DD} = V_{SS}	-20	+20	µA
I_{OS}	Output Short Circuit Current	V_{OUT+}=V_{OUT-}=0V		6	mA
		V_{OUT+}=V_{OUT-}		4	mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH}	Differential Input High Threshold	V_{CM} = -4V to +5V	+100	+600	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = -4V to +5V	-600	-100	mV
V_{ID_HYS}	Differential Input hysteresis	V_{CM} = -4V to +5V	22	28	mV
V_{ID_FS}	Differential Input Fail-safe threshold	Low Differential Threshold voltage or Open circuit maintained more than 500ns	20		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 350 mV	-4	+5	V
I_{IN}	Input Current	V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN+}=V_{TLmin}, V_{IN-}=V_{THmax}	-10	+10	µA
		V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN-}= V_{TLmin}, V_{IN+}=V_{THmax}	-10	+10	µA
ΔI_{IN}	Input Current Balance (I_{IN+}-I_{IN-})	V_{DD} = +3.6V, V_{CM} = -4V to +5V, V_{IN+}=V_{IN-}=V_{CM}	-6	6	uA
I_{CSIN}	Cold Sparing Leakage Current	V_{IN} = +3.6V, V_{DD} = V_{SS}	-20	+20	µA
SUPPLY CURRENT					
I_{CLLD}	Total Dynamic Supply Current	R_L=100Ω, END/ENCK=V_{DD}, V_{DD}=3.6V, Fq=250MHz		100	mA
I_{CLLS}	Total Static Supply Current	R_L=100Ω, END/ENCK=V_{DD}, V_{DD}=3.6V, Fq=DC		80	mA
I_{CCZ}	Tri-State Supply Current	END, ENCK = V_{SS}, V_{DD} = 3.6V		10	mA
PSRR	Power Supply Rejection Ratio	R_L=100Ω, END/ENCK=V_{DD}, V_{DD}=3.6V, Fq=250MHz		-50	dB

Table 3: DC Electrical Characteristics

AC SWITCHING CHARACTERISTICS

Unless otherwise stated, these specifications apply for VDD = 3.3V±0.3V, TA = -55°C to +125°C.

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
t_{PHZ}	Disable Time (Active to Tri-State) High to Z	R_L = 100Ω, C_L = 10pf		4.5	ns
t_{PLZ}	Disable Time (Active to Tri-State) Low to Z	R_L = 100Ω, C_L = 10pf		4.5	ns
t_{PZH}	Enable Time (Tri-State to Active) Z to High	R_L = 100Ω, C_L = 10pf		250	ns
t_{PZL}	Enable Time (Tri-State to Active) Z to Low	R_L = 100Ω, C_L = 10pf		250	ns
t_{LHT}	Input/Output Low-to-High Transition Time, 20% to 80%	R_L = 100Ω, C_L = 1pf	260	600	ps
t_{HLT}	Input/Output High-to-Low Transition Time, 80% to 20%	R_L = 100Ω, C_L = 1pf	260	600	ps
t_{PLHD}	Propagation Low to High Delay	R_L = 100Ω, C_L = 10pf		3,5	ns
T_{PHLD}	Propagation High to Low Delay	R_L = 100Ω, C_L = 10pf		3,5	ns
T_{SKEW}	Differential Skew T_{PHLD} - T_{PLHD}	R_L = 100Ω, C_L = 10pf		150	ps
T_{CCS}	Output Channel-to-Channel Skew	R_L = 100Ω, C_L = 10pf		500	ps
T_{DDS}	Output Device-to-Device Skew	R_L = 100 Ω, C_L = 10pf		750	ps
t_{PJ}	Periodic Jitter	V_{ID} = 200mV, 50% duty cycle at 200MHz, trise≤ 1ns (20% - 80%)		15	ps
t_{CCJ}	Cycle to Cycle Jitter	V_{ID} = 200mV, 50% duty cycle at 200MHz, trise≤ 1ns (20% - 80%)		40	ps
t_{PPJ}	Peak to Peak Jitter	V_{ID} = 27-1 PRBS pattern at 400Mbps, trise ≤ 1ns (20% - 80%)		250	ps
t_{DJ}	Deterministic Jitter	V_{ID} = 27-1 PRBS pattern at 400Mbps, trise ≤ 1ns (20% - 80%)		200	ps

Table 4: AC Electrical Characteristics

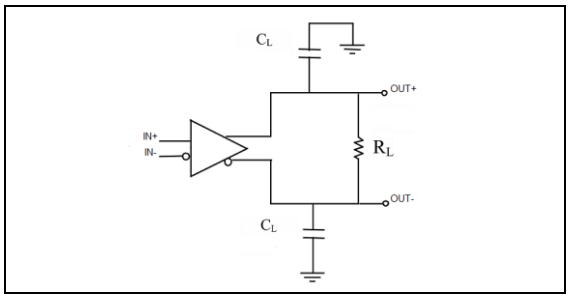

Figure 2: LVDS Output load

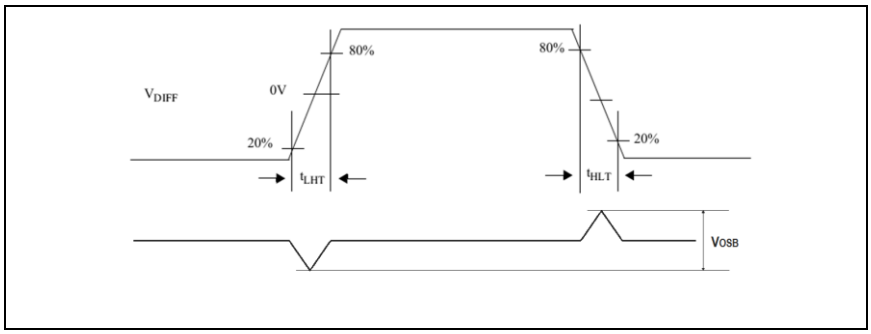

Figure 3: LVDS Output Transition time

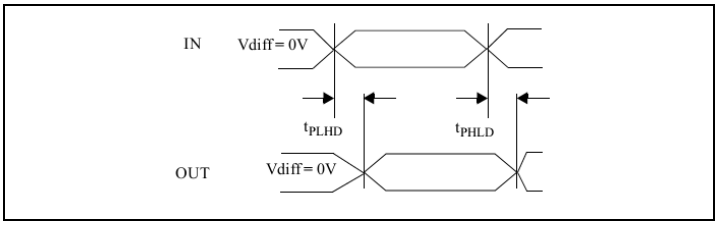

Figure 4: LVDS Propagation delay L->H and H->L

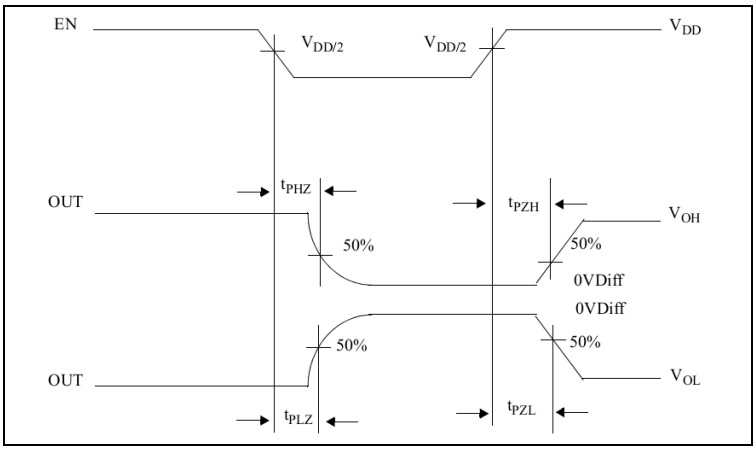

Figure 5: Output active to TRISTATE and TRISTATE to active

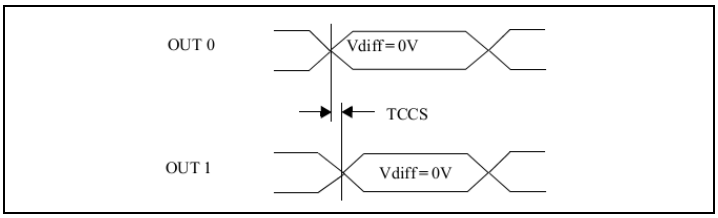

Figure 6: Output channel to channel skew

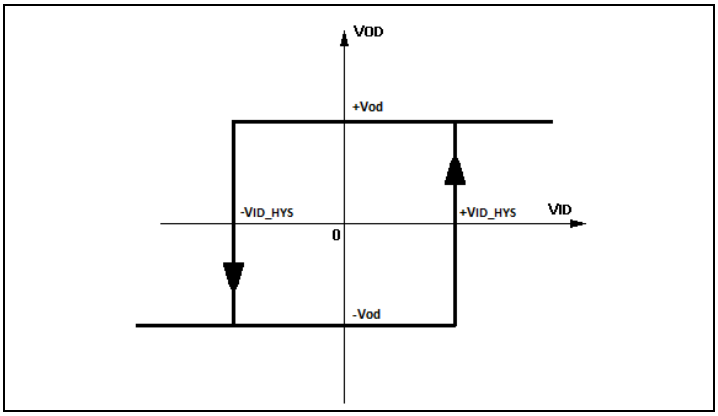

Figure 7: Input Differential Hysteresis

APPLICATIONS INFORMATION

Transmission media:

The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The signal path should be matched in length to avoid any skew in differential lines or between channels.

Input Fail-Safe (comparator and timer)**:**

The ARQ-LVP001 also supports Fail-Safe operation when OPEN or SHORTED inputs are present. Receiver output goes HIGH after 500ns for all fail-safe conditions.

PCB layout and Power System Bypass:

Circuit board layout and stack-up for the ARQ-LVP001 should be designed to provide noise-free power to the device.

Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. A 0.25Ohm resistor is recommended in the power supply line path. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use value of 0.1µF. Tantalum capacitors may be 2.2µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the ARQ-LVP001, as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance and extends the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation, as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity in signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

PINOUT DESCRIPTION

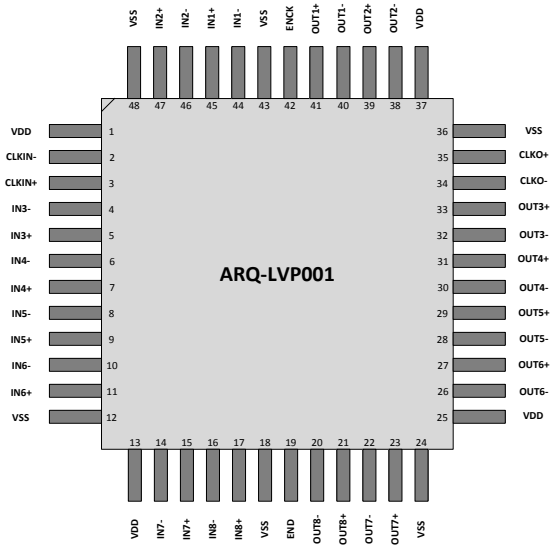

Figure 8: Pinout diagram

№ pin	Name	Type	Description
5, 7, 9, 11, 15, 17, 45, 47	INn+	Input	Non-Inverting LVDS input
4, 6, 8 ,10, 14, 16, 44, 46	INn-	Input	Inverting LVDS input
21, 23, 27, 29, 31, 33, 39, 41	OUTn+	Output	Non-Inverting LVDS output
20, 22, 26, 28, 30, 32, 38, 40	OUTn-	Output	Inverting LVDS output
19	END	Input	Logic low on enable puts the LVDS data output into Tri-State and reduces supply current
42	ENCK	Input	Logic low on enable puts the LVDS clock output into Tri-State and reduces supply current
12, 18, 24, 36, 43, 48	VSS		Ground
1, 13, 25, 37	VDD		Power supply
3	CLKIN+	Input	Non-Inverting Clock LVDS Input
2	CLKIN-	Input	Inverting Clock LVDS Input
35	CLKO+	Output	Non-Inverting Clock LVDS Output
34	CLKO-	Output	Inverting Clock LVDS Output

Table 5: Pinout description

PACKAGE

CQFP48 Drawing

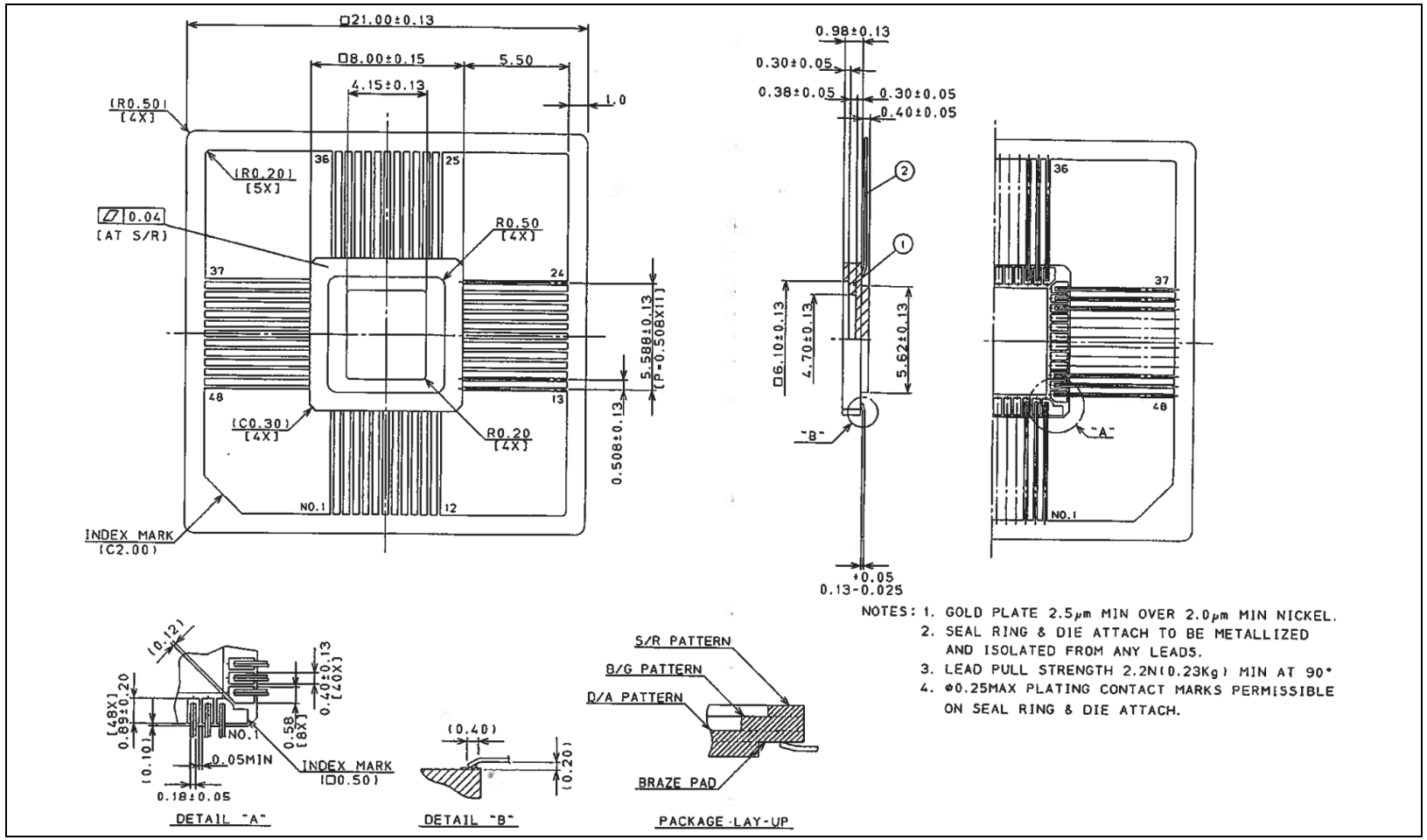

Figure 9: CQFP-48 Package drawing

QUALITY STANDARDS

ARQUIMEA INGENIERÍA S.L.U. develops its activities under the premises of quality and sustainability, offering efficient, liable and innovative technologies and solutions to its customers.

ARQUIMEA's Quality Management System meets the requirements of ISO 9100:2010 Aerospace Series, and has been audited and certified by the Spanish Association for Standardization and Certification, AENOR.

In order to meet the highest quality and reliability, ARQUIMEA designs and develops its aerospace product line according to military and space standards.

Our space microelectronic devices are available in one or more of the following processes:

- Equivalent to QML 38535 LEVEL Q or Level V*
- Equivalent to ESCC 9000*

For procurement in die form

- In accordance with ECSS-Q-ST-60-05C
- Equivalent to QML 38534 LEVEL H or Level K*

*With Radiation Qualification

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REVISION HISTORY

Date Released	Issue	Section	Changes
12-01-2016	Draft A	All	Initial Release copied From ARQ-LVR001 datasheet
23-09-2016	Draft B	ELECTRICAL CHARACTERISTICS AC SWITCHING CHARACTERISTICS	Parameter update after Electrical measurement at Room temperature
13-02-2017	01	FEATURES, APPLICATIONS INFORMATION	Fail-safe feature not available in this version
10-09-2017	02	ELECTRICAL CHARACTERISTICS	Hysteresis feature and Failsafe Threshold Added

Space Technology Partner

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