ESA R&D n° 20167/06/NL/FM

Further Development of the Spacecraft Controller on a Chip

IPMON module
Specification and architecture definition

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00/00	07/02/28			
01/00	07/03/14			Added architecture.
01/01	07/03/21			Architecture modification.
02/00	07/06/05			Modification of the trigger function. Added generics to configure IPMON.
02/01	07/07/25			Changed generics by constants. Update after coding and simulation.
02/02	07/12/20			- Added a generic defining the index of IPMON on AHB bus. - Fixed typos. - Added requirements 5065 and 5093 to mask accesses from TCDD master to ATC PROM slave for both trace and statistics.
02/03	08/01/30			Corrected registers label and registers description order in § 6.

03/00	08/04/15			- Added new functionalities (trace buffer counter, statistics buffer initialization, enable conditional start, idle mode, trig condition on Wait States and Grant delays). - Changed the width of internal registers, trace word and statistics word fields. - Clarified some points of specification (first and last accesses included in trace/statistics in case of conditional trig, difference between it_error and it_cnt_ovflow and associated behaviour, definition of split time and of lock time, block diagram) - Added asynchronous reset and output values at reset

PAGE ISSUE RECORD

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1 INTRODUCTION

This document is the specification of the IPMON module. This module is part of the SCoC3 design. This document is written in the frame of the ESA R&D "Further development of the Spacecraft Controller on a Chip" reference 20167/06/NL/FM.

Requirements are specified throughout this document in table format as follows:

Id	Requirement Text	Verification Method	Upper Links

- the absolute requirement identifier (Id), defined on 4 digits. The first digit corresponds to the current chapter number.
- the requirement text. If tables are considered as part of the requirement, they are referenced clearly in the text, inserted after and separated from the requirement table, and are managed as free text attached to the identifier requirement.
- the verification method as one of the following : R/review of design; I/inspection; A/analysis; T/test, S/similarity, D/definition (not be tracked).
- the trace to the upper level requirements (Upper Links), shall be managed with the following format:
  - **AAAANNNN** where AAAA is a label associated to the upper document and NNNN the requirement identifier of this upper level.
  - Or **CREATED** key word if the requirement has no link with upper level

All document elements, which are not presented in the table format explained above, are not requirements and will not be verified or tracked.

The IPMON module shall perform monitoring on AHB bus.

The document contains the following sections :

- Applicable and reference documents followed by the list of acronyms
- A general description of the module in its environment, and of its content
- A description of the module requirements. This section starts with general requirements, followed by specific requirements of functionality.
- A description of the interfaces
- A detailed description of the architecture

2 DOCUMENTS AND ACRONYMS

2.1 APPLICABLE DOCUMENTS

AD-1	ECSS Q60-02A: Space Product Assurance – ASIC and FPGA Development Standard (17 July 2007)
AD-2	VHDL Modelling Guidelines, ftp://ftp.estec.esa.nl/pub/vhdl/doc/ModelGuide.pdf
AD-3	ESA R&D "Further Development of the Spacecraft Controller on a Chip". Statement of Work
AD-4	Advanced Microcontroller Bus Architecture (AMBA™) Specification, revision 2.0, ARM IHI 0011A

2.2 REFERENCE DOCUMENTS

RD-1	Technical Documentation from Call-Off Order #3 (Spacecraft Controller On-a Chip) of ESA contract #13345/99/NL/FM (Building Blocks for System On-a Chip), known to both parties
RD-2	Contract #13345/99/NL/FM (Building Blocks for System On-a Chip)
RD-3	LEON3 and GRLIB Documentation v1.0.15 April, 2007
RD-4	Synthesisable IP cores available from ESA
RD-5	ASIC Design and Manufacturing Requirements, ESA document WDN/PS/700
RD-6	Minutes of informal meeting R&D.SOC.MN.00395.V.ASTR from 15. December 2005, known to both parties
RD-7	Inputs for Improvement of Prosilogs AHB Monitor Tool (M. Carlqvist, R. Weigand) Issue 1, Revision 0 Draft.

2.3 ACRONYMS

AD	Applicable Document
ADR	Architectural Design Review
AIT	Assembly Integration and Test
AHB	AMBA High speed Bus
AMBA	Advanced Microcontroller Bus Architecture
ASIC	Application Specific Integrated Circuit
ASIM	Application Specific Integrated Microsystem
ASSP	Application Specific Standard Product
BLADE	Board for LEON and Avionics DEvelopment
CDR	Critical Design Review
CPU	Central Processor Unit
DDR	Detailed Design Review
DFF	D-Type Flip Flop
DRC	Design Rule Check
DSP	Digital Signal Processor
EDAC	Error Detection And Correction
EDA	Electronic Design Automation
EGSE	Electrical Ground Support Equipment
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
FDIR	Failure Detection Isolation and Recovery
FPGA	Field Programmable Gate Array
GEO	Geosynchronous Equatorial Orbit
GRLIB	Gaisler Research Library,
HDL	Hardware Description Language
I/O	Input/Output
ID	Identification
IDR	Initial Design Review
IEEE	Institute of Electrical and Electronics Engineers
IP, IPR	Intellectual Property, Intellectual Property Rights
IPMON	Performance Monitoring (IP block)
ITT	Invitation To Tender
JTAG	Joint Test Action Group (refer to IEEE std 1149.1)
LEO	Low Earth Orbit
LET	Linear Energy Transfer
OBDH	On Board Data Handling
OBMU	On Board Management Unit
PCB	Printed Circuit Board
PDF	Portable Document Format
PDR	Preliminary Design Review
PM	Performance Monitoring (in fact called IPMON)
PM	Processor Module
RD	Reference Document
RTEMS	
RTOS	Real Time Operating System (example: RTEMS)
SOC	System On a Chip
SCoC	Spacecraft Controller on a Chip
SEE	Single Event Effect (or SEP Single Event Phenomena)
SEL	Single Event Latch up
SEP	see SEE
SET	Single Event Transient
SEU	Single Event Upset
SRAM	Static Random Access Memory
SRR	Specification Requirement Review
TC	TeleCommand
TID	Total Integrated Dose
TM	TeleMetry
TRP	Technological Research Programme
VHDL	VHSIC Hardware Description Language,
VLSI	Very Large Scale Integration
WP	Work Package
WWW	World Wide Web

3 GENERAL DESCRIPTION OF THE MODULE

The IP Monitoring (IPMON) module is used to spy an AHB Bus, recording trace and statistics data. This IP is designed in the context of the SCOC3 project but can be used as a generic AHB spy module.

The IPMON is used on an AHB bus (Figure 1):

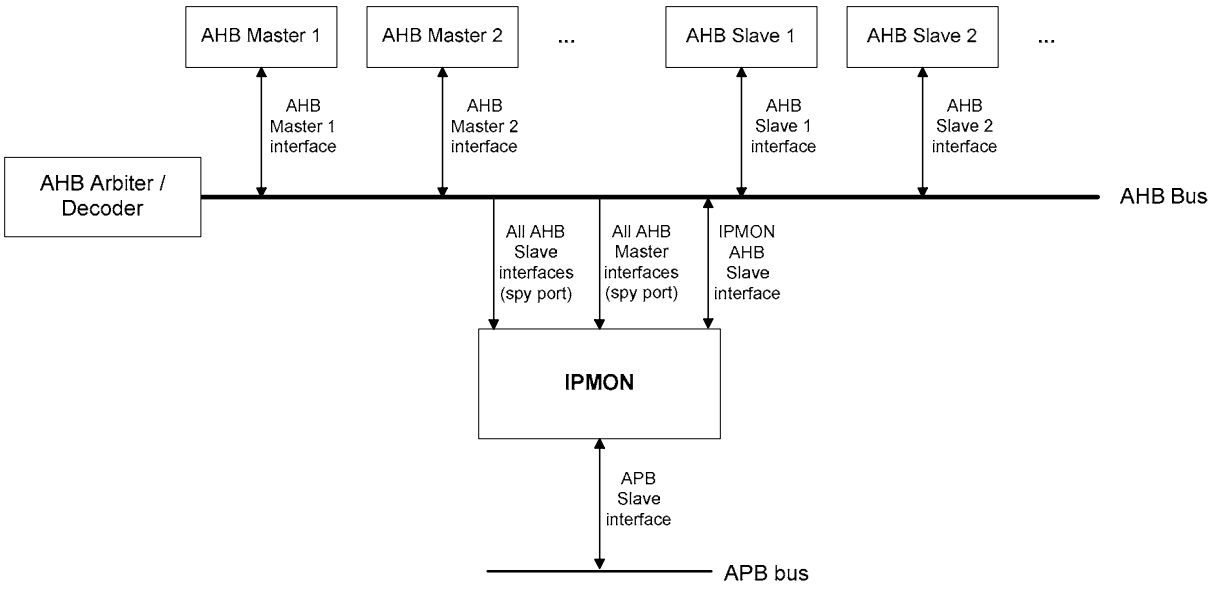

Figure 1 – IPMON on AHB environment

4 GENERAL REQUIREMENTS

4000	The IPMON shall spy the AHB bus.		

4010	The IPMON shall implement an AHB slave interface.		

4020	The IPMON shall integrate a Statistics block.		

4030	The IPMON shall integrate a Trace block inspired by the DSU philosophy [RD3].		

4040	The IPMON shall have configurable trigger conditions to launch statistics block		

	and/or trace block.		

4050	The IPMON shall have internal memory blocks to save trace and statistics data.		

4060	The IPMON shall manage from 1 to 16 masters and from 1 to 16 slaves for trace and statistics (configurable using constants).		

4070	The IPMON shall manage only 32-bit word size when accessed on its AHB slave interface.		

5 SPECIFIC REQUIREMENTS OF FUNCTIONNALITY

5.1 AHB SLAVE INTERFACE

5000	Deleted.		

5010	The AHB slave interface shall be used to read all trace and statistics data contained in the Trace buffer and in the Statistics buffer.		

5.2 APB INTERFACE

5020	The IPMON shall implement an APB slave interface.		

5030	The APB interface shall be used to configure the IPMON registers.		

5.3 TRACE FUNCTION

5040	The IPMON shall integrate a Trace function used to record the traffic on the AHB bus. 'NON-SEQ' and 'SEQ' AHB transfers shall be traced, whereas 'IDLE' or 'BUSY' transfers shall not be traced.		

5050	The Trace function shall start and end recording the traffic according to the Trigger function control.		

5060	The IPMON shall integrate an AHB trace buffer inspired by the DSU function [RD3].		

5061	The IPMON AHB trace buffer shall use a dedicated memory of between 64 and 1024 words of 128 bits (number of words configurable using a constant).		

5062	The 128-bit trace word shall be organized as depicted in Figure 2.		

Bits	Field Name	Description
127..98	Time tag	Trace time counter (reset at the beginning of each trace function activation)
97..87	Grant delay	Delay between Hbusreq = '1' and Hgrant = '1'
86..78	Wait states	Number of wait states (Hready low)
77	Hwrite	AHB Hwrite value
76	Htrans(0)	LSB of AHB Htrans value ('0' for NON-SEQ accesses, '1' for SEQ accesses)
75..74	Hsize(1 downto 0)	LSBs of AHB Hsize value ("00" for 8-bit accesses, "01" for 16-bit accesses, "10" for 32-bit accesses).
73..71	Hburst	AHB Hburst value
70..67	Hmaster	AHB Hmaster value
66	Hmastlock	AHB Hmastlock value
65..64	Hresp	AHB Hresp value
63..32	Data	AHB HRDATA or HWDATA value
31..0	Haddr	AHB HADDR value

Figure 2: 128-bit trace word arrangement

5063	The internal register used to count the number of Wait States shall be 9-bit wide. The internal registers used to count the Grant Delays shall be 11-bit wide. The width of the internal register used to count the split time shall be configurable using a constant (SCOC3 default value: 1 bit).		

5064	The Trace function shall generate two interrupts to the IPMON Interrupt function in case of the following events : • The Trace function stopped due to Freeze_trace pin activation. • The Trace function stopped.		

5065	In the SCOC3 project, the IPMON shall not record traces for accesses between TCDD master and its prom memory (ATC). • This function can be enabled or not (for other projects) using a constant. • The TCDD master number on the AHB bus is given to the IPMON by a generic. • The ATC prom memory mapping is (constants in IPMON package) : o START_ADD = 0x0040_0000 o END_ADD = 0x0082_FFFF		

5066	Each time the trace function is activated, the index of the trace buffer shall restart at address 0. When more than 1024 128-bit words are written in the trace buffer, a roll over shall occur. The 'TR_BUF_CNT' field of the Trace Status Register shall indicate the number of words written in the trace buffer and whether a roll over occurred or not.		

5.4 STATISTIC FUNCTION

5070	Deleted.		

5080	The statistics block shall compute the following statistics for each master/slave pair : • Cumulated number of errors • Cumulated number of OK, • Cumulated number of split, • Cumulated number of retries, • Cumulated number of wait states, • Cumulated latency for the master (Grant delay),		

	• Cumulated number of accesses (SEQ and NON-SEQ), • Cumulated lock time, • Cumulated split time, • Cumulated lock numbers.		

5081	The statistics for a master/slave pair shall be stored in a data word organized as depicted in Figure 3.		

Bits	Field Name	Description
MSBs	ERROR number	Cumulated number of ERROR responses (field size = NBITS_ERROR_REG bits)
	OKAY number	Cumulated number of OKAY responses (field size = NBITS_OKAY_REG bits)
	Split number	Cumulated number of SPLIT responses (field size = NBITS_SPLIT_REG bits)
	Retry number	Cumulated number of RETRY responses (field size = NBITS_RETRY_REG bits)
	Wait states number	Cumulated number of wait states (field size = NBITS_WS_REG bits)
	Master latency	Cumulated latency for the master (Grant delay) (field size = NBITS_MAST_LAT_REG bits)
	Access number	Cumulated number of accesses (SEQ and NON-SEQ) (field size = NBITS_NB_ACC_REG bits)
	Cumulated lock time	Cumulated lock time (field size = NBITS_LOCK_DELAY_REG bits)
	Cumulated split time	Cumulated split time (field size = NBITS_SPLIT_DELAY_REG bits)
LSBs	Lock number	Cumulated number of locks (field size = NBITS_NB_LOCK_REG bits)

Figure 3: 128-bit statistic word arrangement

The number of bits of each field of the 128-bit statistic word is configurable using constants (refer to section 7). The total number of bits of these 10 fields shall be exactly equal to 128. The user who customizes these values is in charge of verifying this rule.

5082	The statistics data words shall be stored in memory in a dedicated statistics Buffer. The buffer size depends on the number of masters and slaves on the AHB bus. This size is between 1 (for 1 master/slave pair) and 256 (for 16 masters and 16 slaves) words of 128 bits. The address in this buffer shall be		

	calculated by appending the slave number (4 bits) and the master number (4 bits).		

5083	The statistics buffer shall be automatically initialized at the end of each soft reset.		

5084	The user shall be able to trigger the initialization of the statistics buffer by writing the INIT_STAT_BUFFER field in the Control Register.		

5085	During the initialization of the statistics buffer (as indicated by the value of the INIT_STAT_BUFFER field of the Control Register), no other functionalities of the IPMON shall be usable: - it shall not be possible to activate trace and statistics functions - the IPMON AHB slave interface shall answer HRESP=ERROR responses		

5086	When the statistics function is activated multiple times without initializing the statistics buffer, the statistics shall be cumulated.		

5090	The IPMON shall perform the statistics during a programmable maximum integration time.		

5091	The programmable maximum integration time shall be configurable through the APB bus by using the IPMON Statistic Delay Register, as defined in section 6.		

5092	The Statistic function shall generate two interrupts to the IPMON Interrupt function in case of the following events : • One of the 10 registers composing the statistics word reached its maximum value (in case one of these registers tries to overflow, no roll over shall occur and the register shall be saturated to its maximum value). • The statistics function stopped.		

5093	In the SCOC3 project, the IPMON shall not record statistics for accesses between TCDD master and its prom memory (ATC). • This function can be enabled or not (for other projects) using a constant. • The TCDD master number on the AHB bus is given to the IPMON by a generic. • The ATC prom memory mapping is (constant in IPMON package) : o START_ADD = 0x0040_0000 o END_ADD = 0x0082_FFFF		

5.5 TRIGGER FUNCTION

5100	The IPMON shall integrate a trigger function used to control the activation of the Trace and Statistics functions.		

5101	There shall be two ways to start and stop Trace and Statistics functions: • unconditionally, writing the APB_TRIG Register: The trig order (start or stop Trace or Statistics function) shall be immediately executed • conditionally, using 'Trigger Units': it shall be possible to program Trace or Statistics functions to be triggered when a specific transfer occurs on the bus		

5110	The Trigger function shall implement the following trigger conditions for the Trace and statistics functions : • Trig on Wait States/Grant delay value • Trig on address/data value, • Trig on HRESP value, • Trig on HWRITE value, • Trig on HSLAVE number, • Trig on HMASTER number.		

5120	The trigger conditions of requirement 5110 are grouped in a register named 'Trigger Unit' (refer to section 6). The IPMON shall implement between 1 and 4 trigger units (configurable using a constant). The trigger unit registers shall be configurable through the APB bus.		

5130	The trigger function shall generate 4 trigger events : • Start Trace (ST) • End of Trace (ET) • Start Statistics (SS) • End of Statistics (ES)		

5140	It shall be possible that each of the 4 trigger events can be triggered by any combination of the trigger units. This shall be configurable through the Event Configuration registers (defined in section 6).		

5141	The Start Trace and Start Statistics events shall be generated conditionally (by Trigger Units) only when the 'Enable Conditional Start' fields of the Control Register are equal to 1. Once such a generation occurred, these fields shall be set to 0. Therefore, after they have stopped, trace or statistics functions shall not start again automatically if the same trigger condition occurs on the bus.		

5142	In case one of the internal registers used to compute trace and statistics data (Wait States, Grant Delay, or Split time counter) reaches its maximum value, the trace and the statistics functions shall stop and an interrupt (it_error) shall be generated.		

5150	Finally, the trace function shall start when : • ST event is activated and conditional start is enabled **or** Bit APB_ST of the APB_TRIG_REG is activated And shall stop when : • ET event is activated **or** Bit APB_ET of the APB_TRIG_REG is activated **or** the IPMON is accessed on its AHB slave interface **or** an Internal counter overflowed (it_error) **or** Freeze_trace pin is activated		

5160	Finally, the statistics function shall start when : • SS event is activated and conditional start is enabled **or** Bit APB_SS of the APB_TRIG_REG is activated And shall stop when : • ES event is activated **or** Bit APB_ES of the APB_TRIG_REG is activated **or** the IPMON is accessed on its AHB slave interface **or** Statistics Delay Counter reached 0 **or** an Internal counter overflowed (it_error) **or** one of the 10 registers composing the statistics word overflowed (cnt_ovflow).		

5170	The trigger function shall manage 2 status registers called: • IPMON_TRACE_STATUS_Reg • IPMON_STAT_STATUS_Reg They shall contain, for each trigger event, the combination of the trigger units which were active when the event was triggered. A read of these registers shall		

	clear their content when the trace/statistics function is not active (if the trace/statistics function is active, the TRACE_STATUS_REG/STAT_STATUS_REG shall not be cleared).		

5180	When the trace/statistics functions are **started conditionally**, the access which triggered the activation shall **not be included** in the trace/statistics. When the trace/statistics functions are **stopped conditionally**, the access which triggered the stop shall be **included** in the trace/statistics. When the trace/statistics functions are **stopped** by an access to the IPMON **AHB slave interface**, the access to the IPMON AHB slave interface shall **not be included** in the trace/statistics. When the statistics function is **stopped** by a **cnt_ovflow interrupt,** the access which caused the counter overflow shall be **included** in the statistics (with at least one field saturated to its maximum value).		

5190	At the end of a hard reset (rstn input pin), the IPMON shall stay in a "soft reset" mode, to lower power consumption. To use the IPMON, the soft reset mode shall be left, by writing the IPM_RST field of the Control Register.		

5.6 INTERRUPT FUNCTION

5200	The IPMON shall include an interrupt function that manages 5 interrupt sources.		

5210	In case of an interrupt, the corresponding bit of the IPMON Interrupt Status Register shall be raised as defined in section 6.		

5220	A read of the IPMON Interrupt Status Register shall clear the IPMON Interrupt Status Register.		

5230	The 5 interrupt bits of the IPMON Interrupt Status Register shall be ORed to generate the IT_IPMON signal, taking into account the mask defined in the IPMON Interrupt Mask Register.		

6 REGISTERS DEFINITION

6000	The IPMON registers shall be programmable via the APB bus.		

6010	The IPMON registers shall be compliant with the definitions given in section 6.		

Abbrev	Register name	Address
IPMON_CTRL_Reg	IPMON Control Register	0x00
IPMON_ST_CONF_Reg	IPMON Start Trace Event Configuration Register	0x04
IPMON_ET_CONF_Reg	IPMON End Trace Event Configuration Register	0x08
IPMON_SS_CONF_Reg	IPMON Start Statistics Event Configuration Register	0x0C
IPMON_ES_CONF_Reg	IPMON End Statistics Event Configuration Register	0x10
IPMON_APB_TRIG_Reg	IPMON APB Trig Register	0x14
IPMON_STAT_DELAY_Reg	IPMON Statistics Delay Register	0x18
IPMON_IT_MASK_Reg	IPMON Interrupt Mask Register	0x1C
IPMON_IT_STATUS_Reg	IPMON Interrupt Status Register	0x20
IPMON_TRACE _STATUS_Reg	IPMON Trace Status Register	0x24
IPMON_STAT _STATUS_Reg	IPMON Statistics Status Register	0x28
IPMON_GP1_TU1_Reg	IPMON Global Purpose Register 1 associated with TU1	0x2C
IPMON_GP2_TU1_Reg	IPMON Global Purpose Register 2 associated with TU1	0x30
IPMON_TU1_Reg	IPMON Trigger Unit 1 Register	0x34
IPMON_GP1_TU2_Reg (*)	IPMON Global Purpose Register 1 associated with TU2	0x38
IPMON_GP2_TU2_Reg (*)	IPMON Global Purpose Register 2 associated with TU2	0x3C
IPMON_TU2_Reg (*)	IPMON Trigger Unit 2 Register	0x40
IPMON_GP1_TU3_Reg (*)	IPMON Global Purpose Register 1 associated with TU3	0x44
IPMON_GP2_TU3_Reg (*)	IPMON Global Purpose Register 2 associated with TU3	0x48
IPMON_TU3_Reg (*)	IPMON Trigger Unit 3 Register	0x4C
IPMON_GP1_TU4_Reg (*)	IPMON Global Purpose Register 1 associated with TU4	0x50
IPMON_GP2_TU4_Reg (*)	IPMON Global Purpose Register 2 associated with TU4	0x54
IPMON_TU4_Reg (*)	IPMON Trigger Unit 4 Register	0x58

Figure 4: List of the IPMON registers

(*) if defined by the Nt constant. Reading a non defined register (i.e. : IPMON_TU3_Reg if only 2 trigger units are defined by the Nt constant) returns 0, and writing such a register does not have effect.

Control Register (IPMON_CTRL_Reg) : 0x00

Bits	Field Name	Description	r/w	Reset Value
31..4	RESERVED	Reserved	r	0
3	EN_COND_START_TR	Enable Conditional Start Trace : The Start Trace event can be generated conditionally (by Trigger Units) only when this field is equal to 1. Once such a generation occurred, this field is set to 0. This field does not concern trace trig by APB.	r/w	0
2	EN_COND_START_ST	Enable Conditional Start Stat : The Start Stat event can be generated conditionally (by Trigger Units) only when this field is equal to 1. Once such a generation occurred, this field is set to 0. This field does not concern stat trig by APB.	r/w	0
1	INIT_STAT_BUFFER	Initialize Statistics Buffer : The statistics buffer is initialized when '1' is written in this field or at the end of a reset. While this field is equal to 1, the buffer is being initialized and : - trace/stat functions can't be activated - no access should occur on IPMON AHB slave interface	r/w	0
0	IPM_RST	Soft Reset of the IPMON : resets all the registers. At the end of a hard reset, the IPMON is in Soft Reset mode (low power consumption mode). Write '0' in this field to quit the Soft Reset mode.	r/w	1

Figure 5: IPMON_CTRL_Reg register definition

Event Configuration Registers (IPMON_ST_CONF_Reg, IPMON_ET_CONF_Reg, IPMON_SS_CONF_Reg, IPMON_ES_CONF_Reg) : 0x04, 0x08, 0x0C, 0x10

Bits	Field Name	Description	r/w	Reset Value
31..16	RESERVED	Reserved	r	0
15	TU4 & TU3 & TU2 & TU1	Trig event when the conditions of TU4 and TU3 and TU2 and TU1 are true	r/w	0
14	TU4 & TU3 & TU2	Trig event when the conditions of TU4 and TU3 and TU2 are true	r/w	0
13	TU4 & TU3 & TU1	Trig event when the conditions of TU4 and TU3 and TU1 are true	r/w	0
12	TU4 & TU3	Trig event when the conditions of TU4 and TU3 are true	r/w	0
11	TU4 & TU2 & TU1	Trig event when the conditions of TU4 and TU2 and TU1 are true	r/w	0
10	TU4 & TU2	Trig event when the conditions of TU4 and TU2 are true	r/w	0
9	TU4 & TU1	Trig event when the conditions of TU4 and TU1 are true	r/w	0
8	TU4	Trig event when the conditions of TU4 are true	r/w	0
7	TU3 & TU2 & TU1	Trig event when the conditions of TU3 and TU2 and TU1 are true	r/w	0
6	TU3 & TU2	Trig event when the conditions of TU3 and TU2 are true	r/w	0
5	TU3 & TU1	Trig event when the conditions of TU3 and TU1 are true	r/w	0
4	TU3	Trig event when the conditions of TU3 are true	r/w	0
3	TU1 & TU2	Trig event when the conditions of TU2 and TU1 are true	r/w	0
2	TU2	Trig event when the conditions of TU2 are true	r/w	0
1	TU1	Trig event when the conditions of TU1 are true	r/w	0
0	RESERVED	Reserved	r	0

Figure 6: IPMON_XX_CONF_Reg register definition

When several conditions are set to 1, the event is triggered when **any** of them is true.

For example:

- Writing 1 in bit 6 of register IPMON_ST_Conf_Reg allows the Start Trace event to be triggered when the conditions of Trigger Unit 2 **and** of Trigger Unit 3 are true.
- Writing 1 in bits 1 and 2 of register IPMON_ST_Conf_Reg allows the Start Trace event to be triggered when the conditions of Trigger Unit 1 **or** of Trigger Unit 2 are true.

APB Trig register (IPMON_APB_TRIG_Reg) : 0x14

Bits	Field Name	Description	r/w	Reset Value
31..4	RESERVED	Reserved	r	0
3	APB_ES	Trig End of Statistics by APB bus	r/w	0
2	APB_SS	Trig Start of Statistics by APB bus	r/w	0
1	APB_ET	Trig End of Trace by APB bus	r/w	0
0	APB_ST	Trig Start of Trace by APB bus	r/w	0

Figure 7: IPMON_APB_TRIG_Reg definition

The fields of the APB Trig register are automatically reset to 0 when the trig order has been taken into account.

Statistics Delay Register (IPMON_STAT_DELAY_Reg) : 0x18

Bits	Field Name	Description	r/w	Reset Value
31..0	IPM_STAT_DELAY	Defines the maximum integration time (in clock cycles) for statistics.	r/w	0

Figure 8: IPMON_STAT_DELAY_Reg definition

Interrupt Mask Register (IPMON_IT_MASK_Reg) : 0x1C

Bits	Field Name	Description	r/w	Reset Value
31..5	RESERVED	Reserved	r	0
4	IPM_IT_ MASK_ERROR	When '0', mask IPM_IT_ERROR for the generation of the IT signal	r/w	0
3	IPM_IT_MSK_TRACE_FREEZE	When '0', mask IPM_IT_TRACE_FREEZE for the generation of the IT signal	r/w	0
2	IPM_IT_MSK_TRACE_STOP	When '0', mask IPM_IT_TRACE_STOP for the generation of the IT signal	r/w	0
1	IPM_IT_MSK_STAT_CNT	When '0', mask IPM_IT_STAT_CNT for the generation of the IT signal	r/w	0
0	IPM_IT_MSK_STAT_STOP	When '0', mask IPM_IT_STAT_STOP for the generation of the IT signal	r/w	0

Figure 9: IPMON_IT_MASK_Reg definition

Interrupt Status Register (IPMON_IT_STATUS_Reg) : 0x20

Bits	Field Name	Description	r/w	Reset Value
31..5	RESERVED	Reserved	r	0
4	IPM_IT_ERROR	Indicates that one of the internal registers (Wait States, Grant Delay, or Split time counter) has reached its maximum value, thus stopping both trace and statistics functions	r	0
3	IPM_IT_TRACE_FREEZE	Indicates that trace function has stopped because external Freeze_Trace pin was activated	r	0
2	IPM_IT_TRACE_STOP	Indicates that trace function has stopped	r	0
1	IPM_IT_STAT_CNT	Indicates that one of the 10 registers composing the statistics word has reached its maximum value, thus stopping the statistics function	r	0
0	IPM_IT_STAT_STOP	Indicates that statistics function has stopped	r	0

Figure 10: IPMON_IT_STATUS_Reg definition

The Interrupt Status Register is reset when it is read by APB.

Trace Status Register (IPMON_TRACE_STATUS_Reg) : 0x24

Bits	Field Name	Description	r/w	Reset Value
31..19	RESERVED	Reserved	r	0
19..8	TR_BUF_CNT	Number of 128-bit words written in the trace buffer. Value between 0 and 2048 : - When 0 : no trace words have been written in the buffer. - When between 1 and 1024 : from 1 to 1024 words have been written in the trace buffer. - When between 1025 and 2048 : strictly more than 1024 words have been written, and the trace buffer rolled over. This field minus 1024 indicates the number of words written since the last roll over.	r	0
7..4	ET_STATUS	Reports which Trigger Units were active when the Trace function stopped (Bit 4 for TU1, bit 5 for TU2, etc.). Note that this field represents the status of **all** the Trigger Units (not only the status of the Trigger Units which triggered the End Trace event).	r	0
3..0	ST_STATUS	Reports which Trigger Units were active when the Trace function started (Bit 0 for TU1, Bit 1 for TU2, etc.). Note that this field represents the status of **all** the Trigger Units (not only the status of the Trigger Units which triggered the Start Trace event).	r	0

Figure 11: IPMON_TRACE_STATUS_Reg definition

IPMON_TRACE_STATUS_Reg fields are reset when they are read by APB while Trace function is stopped (if Trace function is active, they are not reset).

Statistics Status Register (IPMON_STAT_STATUS_Reg) : 0x28

Bits	Field Name	Description	r/w	Reset Value
31.. 8	RESERVED	Reserved	r	0
7..4	ES_STATUS	Reports which Trigger Units were active when the Statistics function stopped (Bit 4 for TU1, bit 5 for TU2, etc.). Note that this field represents the status of **all** the Trigger Units (not only the status of the Trigger Units which triggered the End Statistics event).	r	0
3..0	SS_STATUS	Reports which Trigger Units were active when the Statistics function started (Bit 0 for TU1, Bit 1 for TU2, etc.). Note that this field represents the status of **all** the Trigger Units (not only the status of the Trigger Units which triggered the Start Statistics event).	r	0

Figure 12: IPMON_STAT_STATUS_Reg definition

IPMON_STAT_STATUS_Reg fields are reset when they are read by APB while Statistics function is stopped (if the Statistics function is active, they are not reset).

Global Purpose 1 Register (IPMON_GP1_TU1_Reg, IPMON_GP1_TU2_Reg, IPMON_GP1_TU3_Reg, IPMON_GP1_TU4_Reg) : 0x2C, 0x38, 0x44, 0x50

Bits	Field Name	Description	r/w	Reset Value
31..0	IPM_GP1_TUx	Defines Address or Data or first Address or Data value for trigger Address/Data field	r/w	0

Figure 13: IPMON_GP1_TUx_Reg register definition

Global Purpose 2 Register (IPMON_GP2_TU1_Reg, IPMON_GP2_TU2_Reg, IPMON_GP2_TU3_Reg, IPMON_GP2_TU4_Reg) : 0x30, 0x3C, 0x48, 0x54

Bits	Field Name	Description	r/w	Reset Value
31..0	IPM_GP2_TUx	Defines Address or Data mask or last Address or Data value for trigger Address/Data field	r/w	0

Figure 14: IPMON_GP2_TUx_Reg register definition

Trigger Unit Registers (IPMON_TU1_Reg, IPMON_TU2_Reg, IPMON_TU3_Reg, IPMON_TU4_Reg) : 0x34, 0x40, 0x4C, 0x58

Bits	Field Name	Description	r/w	Reset Value
31	RESERVED	Reserved	r	0
30..20	IPM_WS_GD_VAL	Wait States/Grant delay value for the "trig on Wait States/Grant delay" condition.	r/w	0
19	IPM_SEL_WS_GD	The "trig on Wait States/Grant delay"condition concerns: - Grant Delays when '1' - Wait States when '0'	r/w	0
18	IPM_TG_WS_GD	Trig on Wait States/Grant delays. Depending on bit 19: - Trig when a transfer completed with more Wait States than the value defined by bits 30..20 - or Trig when the Grant Delay of the master defined by bits 4..1 is greater than the value defined by bits 30..20 (this condition can trig even when the transfer is performed by another master, if field 'IPM_TG_HMAST' is '0').	r/w	0
17..16	IPM_ADD_DT	Defines the type of trigger for the "trig on Address/data" condition (see Figure 16)	r/w	0
15	IPM_TG_ADD_DT	Trig when a transfer is performed at specific addresses or with specific data (see Figure 16)		0
14..13	IPM_HRESP	Defines the Hresp response for the "Trig on Hresp" condition	r/w	0
12	IPM_TG_HRESP	Trig when a specific Hresp response (defined by bits 14..13) is provided during a transfer	r/w	0
11	IPM_HWRITE	Defines Hwrite for the "Trig on Hwrite" condition	r/w	0
10	IPM_TG_ HWRITE	Trig when the transfer is a read or a write operation (according to bit 11)	r/w	0
9..6	IPM_HSLAVE	Defines the slave number for the "Trig on Hslave" condition	r/w	0
5	IPM_TG_HSLAVE	Trig when a specific slave (defined by bits 9..6) is accessed	r/w	0
4..1	IPM_HMAST	Defines a master number (used for the conditions "Trig on HMaster" and "Trig on Grant Delay")	r/w	0
0	IPM_TG_HMAST	Trig when a specific master (defined by bits 4..1) performs a transfer	r/w	0

Figure 15: IPMON_TUx_Reg registers definition

When different conditions are enabled at the same time (with IPM_TG_* fields), the Trigger Unit triggers when **all** theses conditions are true (and not when **any** of these conditions is true).

Bit 15 is used to enable trigger on a specific Address / Data with mask or on a specific Address / Data range with first/last values, as defined in the following table:

Bits 17-16	Trig on	GP1	GP2
00	Address (with mask)	Defines address	Defines address mask
01	Address range	Defines first address	Defines last address
10	Data (with mask)	Defines data	Defines data mask
11	Data range	Defines first data	Defines last data

Figure 16: IPMON_GPx_TUy_Reg bits 16-17 definition

7 CONFIGURATION OPTIONS

Constants defined in pack_ipmon.vhd file	Function	Allowed Range	Default value (SCOC3)
Nmaster	Number of AHB masters	1 - 16	12
Nslave	Number of AHB slaves	1 - 16	4
Nwt	Number of words for the trace buffer	64 - 1024	1024
Nt	Number of trigger units	1 - 4	4
NBITS_ERROR_REG	Number of bits of the ERROR register in the 128 bits statistic word	The sum of these fields shall be exactly 128	13
NBITS_OKAY_REG	Number of bits of the OKAY register in the 128 bits statistic word		17
NBITS_SPLIT_REG	Number of bits of the SPLIT register in the 128 bits statistic word		1
NBITS_RETRY_REG	Number of bits of the RETRY register in the 128 bits statistic word		1
NBITS_WS_REG	Number of bits of the WAIT STATE register in the 128 bits statistic word		22
NBITS_MAST_LAT_REG	Number of bits of the MASTER LATENCY register in the 128 bits statistic word		22
NBITS_NB_ACC_REG	Number of bits of the ACCESS NUMBER register in the 128 bits statistic word		18
NBITS_LOCK_TIME_REG	Number of bits of the LOCK TIME register in the 128 bits statistic word		19
NBITS_SPLIT_TIME_REG	Number of bits of the SPLIT TIME register in the 128 bits statistic word		1
NBITS_NB_LOCK_REG	Number of bits of the LOCK NUMBER register in the 128 bits statistic word		14
NBITS_INT_SPLIT_TIME_CNT	Number of bits of the internal Split Time counter	1 - 128	1
TCDD_to_ATCPROM_trace_en	Choose false to mask accesses from TCDD to ATC prom in traces and statistics	true/false	false
ATCPROM_START_ADD	ATC prom memory start address		0x00400000
ATCPROM_END_ADD	ATC prom memory end address		0x0082FFFF

Figure 17: Configuration options using constants

Generic	Function	Allowed Range	Default (SCOC3)
TCDDMASTER	TCDD master number on the AHB bus	0 – (Nmaster-1)	8
tech	Technology mapping (to implement appropriate memories)	ATC18s / VIRTEX2 / VIRTEX4	ATC18s

Figure 18: Configuration options using generics

8 INTERFACES

Signal	*Direction*	*Source / destination*	*Function*	*Asynchronous reset value*	*Synchronous reset value*
clk	In		IPMON clock		
rstn	In		IPMON synchronous reset		
arstn	In		IPMON asynchronous reset		
IT_IPMON	Out		IPMON interruption signal	-	'0'
Freeze_Trace	In		IPMON External trace function stop		
AHB slave interface input (Readout port)					
HSEL	In	Slave	Slave selection signal active to '1'		
HADDR[31:0]	In	Slave	Slave Address bus		
HWRITE	In	Slave	Indicates a write transfer '0' : read access '1' : write access		
HTRANS[1:0]	In	Slave	Defines transfer type: "00" : IDLE "01" : BUSY "10" : NONSEQ "11" : SEQ		
HSIZE[2:0]	In	Slave	Defines data transfer size		
HBURST[2:0]	In	Slave	Indicates burst type		
HWDATA[31:0]	In	Slave	Write data on slave I/F		
HPROT[3:0]	In	Slave	Indicates protection control		
HREADY	In	Slave	HREADY slave input		
HMASTER[3:0]	In	Slave	Indicates which bus master is currently performing access		
HMASTLOCK	In	Slave	Indicates that the current master is performing a locked sequence of transfers		

AHB slave interface output (Readout port)					
HREADYOUT	Out	Slave	Indicates that a transfer has finished on the bus	’0’	’0’
HRESP[1:0]	Out	Slave	Provides transfer response: “00” : OKAY “01” : ERROR “10” : RETRY “11” : SPLIT	“00”	“00”
HRDATA[31:0]	Out	Slave	Read data on slave I/F	-	0
HSPLIT[15:0]	Out	Slave	Indicates to the arbiter which bus masters should be allowed to re-attempt a split transaction	0	0
AHB master input (from 0 to Nm-1) (Spy ports)					
HGRANT	In	Master	Indicates that the master is currently the highest priority master		
HREADY	In	Master	Indicates that a transfer has finished on the bus		
HRESP[1:0]	In	Master	Provides transfer response “00” : OKAY “01” : ERROR “10” : RETRY “11” : SPLIT		
HRDATA[31:0]	In	Master	Read data Master bus		
AHB Master output (from 0 to Nm-1) (Spy ports)					
HBUSREQ	In	Master	Indicates that the master requests the bus		
HLOCK	In	Master	Indicates that the master requires locked access to the bus		
HTRANS[1:0]	In	Master	Defines transfer types “00” : IDLE “01” : BUSY “10” : NONSEQ “11” : SEQ		

HADDR[31:0]	In	Master	Master Address bus		
HWRITE	In	Master	Indicates a write transfer '0' : read access '1' : write access		
HSIZE[2:0]	In	Master	Defines data transfer size		
HBURST[2:0]	In	Master	Indicates burst type		
HPROT[3:0]	In	Master	Indicates protection control		
HWDATA[31:0]	In	Master	Write data Master bus		
AHB slave interface input (from 0 to Ns-1) (Spy ports)					
HSEL	In	Slave	Slave selection signal active to '1'		
HADDR[31:0]	In	Slave	Slave Address bus		
HWRITE	In	Slave	Indicates a write transfer '0' : read access '1' : write access		
HTRANS[1:0]	In	Slave	Defines transfer type "00" : IDLE "01" : BUSY "10" : NONSEQ "11" : SEQ		
HSIZE[2:0]	In	Slave	Defines data transfer size		
HBURST[2:0]	In	Slave	Indicates burst type		
HWDATA[31:0]	In	Slave	Write data on slave I/F		
HPROT[3:0]	In	Slave	Indicates protection control		
HREADY	In	Slave	HREADY slave input		
HMASTERS3:0]	In	Slave	Indicates which bus master is currently performing access		
HMASTLOCK	In	Slave	Indicates that the current master is performing a locked sequence of transfers		
AHB slave interface output (from 0 to Ns-1) (Spy ports)					
HREADYOUT	In	Slave	Indicates that a transfer has finished on the bus		
HRESP[1:0]	In	Slave	Provides transfer response "00" : OKAY		

			"01" : ERROR "10" : RETRY "11" : SPLIT		
HRDATA[31:0]	In	Slave	Read data on slave I/F		
HSPLIT[15:0]	In	Slave	Indicates to the arbiter which bus masters should be allowed to re-attempt a split transaction		
APB input					
PSEL	In		This signals indicates that the slave is selected (active high).		
PENABLE	In		The enable signal is used to indicate the second cycle of an APB transfer (active high).		
PADDR[31:0]	In		APB address bus		
PWRITE	In		This signals indicates transfer type write access at '1' and read access at '0'.		
PWDATA[31:0]	In		Write data bus		
APB output					
PRDATA[31:0]	Out		Read data bus	-	0

9 ARCHITECTURE DESCRIPTION

The IPMON is composed of the following different blocks:

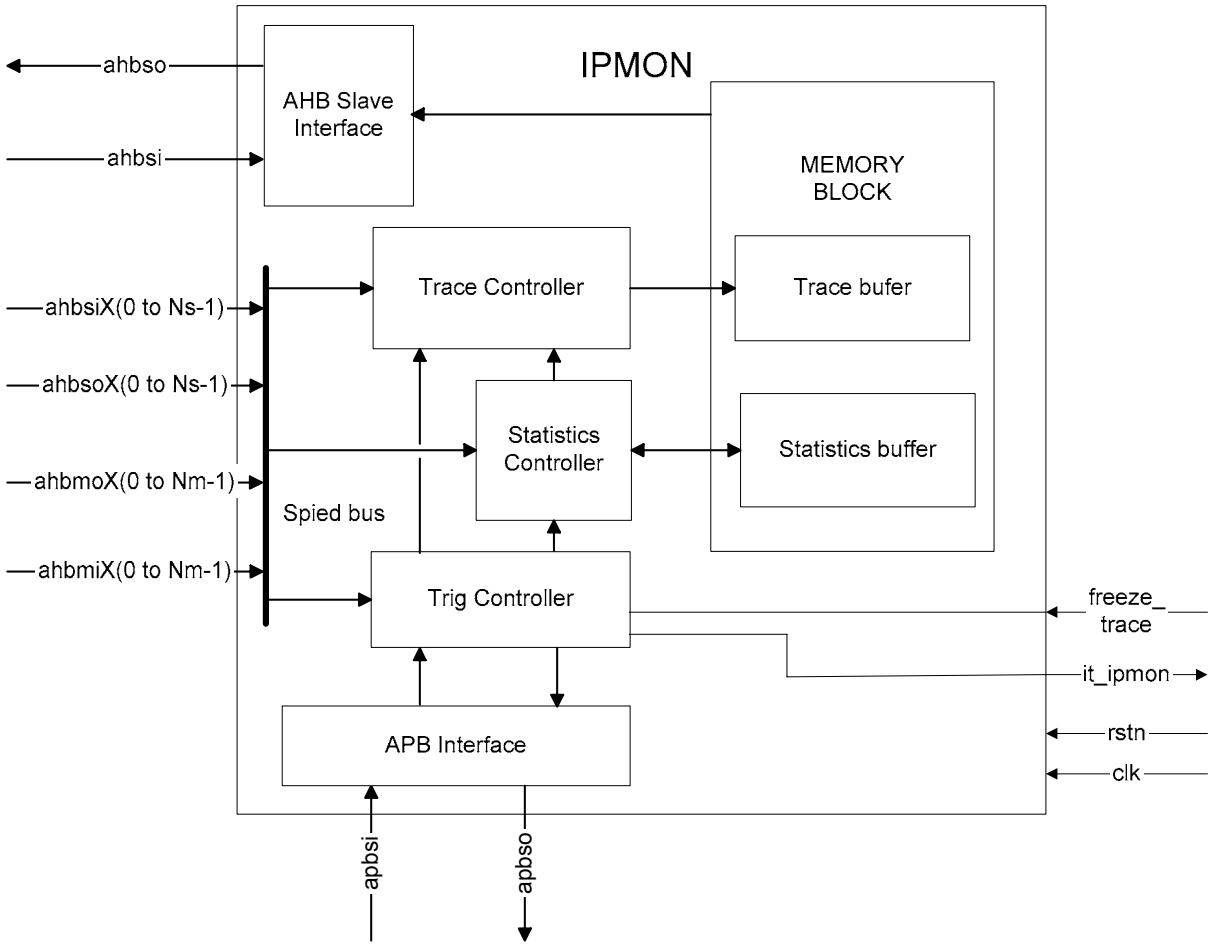

Figure 19: IPMON block diagram

- The AHB slave interface is used to read statistics and trace data into Memory block,
- The Trace Controller is used to trace AHB signals from AHB bus,
- The Statistics Controller is used to calculate statistics data from AHB bus,
- The Memory block is used to store trace and statistics data,
- The Trig Controller is used to command Trace Controller and Statistics Controller with trigger conditions,
- The APB Interface is used to configure trigger registers and read Status registers.

9.1 STATISTICS BLOCK DESCRIPTION

The statistics module calculates statistics data for each master/slave pair. These data are stored in the Statistics buffer (part of the memory block module). One 128-bit statistics word is stored for each master/slave pair (Figure 20).

For each SEQ or NON-SEQ AHB exchange, the statistics module reads the corresponding word in the memory, computes the new statistics and then writes the updated word in memory.

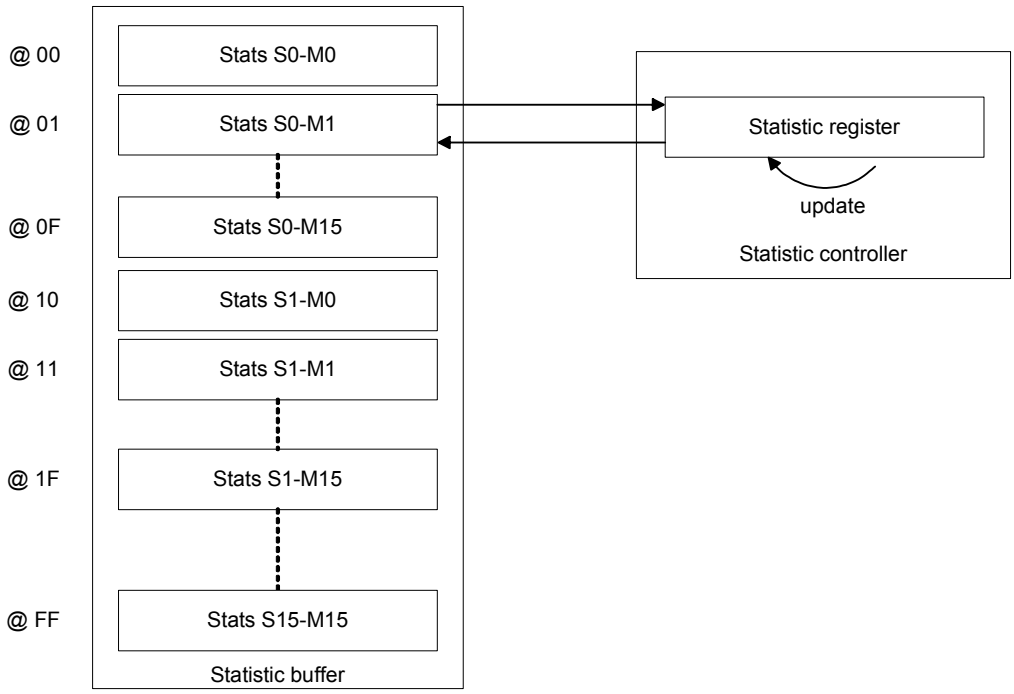

Figure 20: Statistic buffer arrangement and data update mechanism

The address MSB are given by the slave number and the address LSB are given by the master number.

The buffer size is 1 to 256 words of 128 bits (up to 16 masters and 16 slaves).

The 128-bit statistics word is organized as follows (Figure 21):

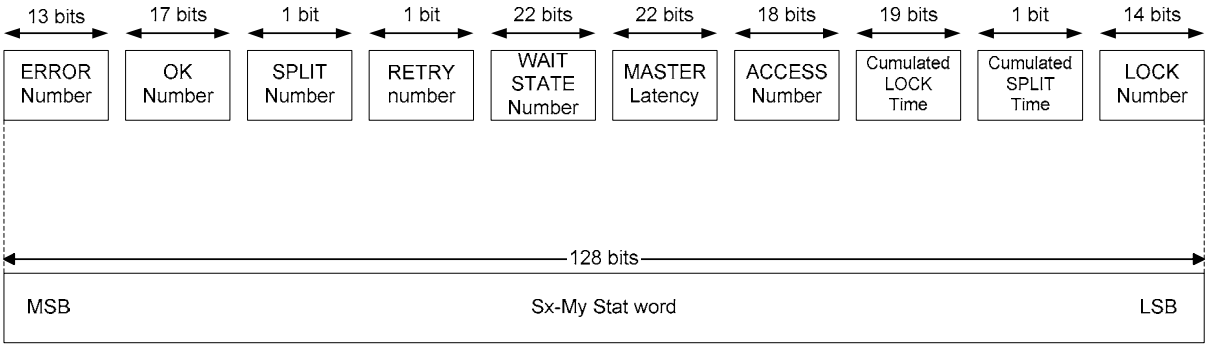

Figure 21: 128-bit statistics word

The number of bits of each field is configurable using constants. Figure 21 shows the SCOC3 configuration.

The fields 'OK number', 'ERROR number', 'RETRY number' and 'SPLIT number' correspond to the cumulated number of responses with HRESP equal to 'OK', 'ERROR', 'RETRY' or 'SPLIT'.

'Wait States number' is the cumulated number of Wait States (HREADY low).

'Master latency' is the cumulated Grant Delay (delay between HBUSREQ = '1' and HGRANT = '1').

The access number is the number of accesses with HTRANS = NON-SEQ or HTRANS = SEQ (IDLE and BUSY transfers are not taken into account).

'Lock number' is the number of locked accesses (accesses with HMASTLOCK = '1').

The Lock time is the length of a locked transfer (the number of clock cycles of its data phase). 'Cumulated Lock time' is the cumulated lock time for a master/slave pair.

The Split time is the number of clock cycles between an HRESP=SPLIT response and the address phase of the next transfer for the master which has been split. 'Cumulated Split time' is the cumulated split time for a master/slave pair. The IPMON can only manage one SPLIT access at a time.

The internal register used to count the number of wait states is 9-bit wide.

The internal registers used to count the grant delays are 11-bit wide.

The width of the internal register used to count the split time is configurable (SCOC3 default value: 1-bit wide).

The 10 registers composing the statistics word represent cumulated values (as opposed to internal registers). When one of these 10 registers reaches its maximum value or tries to overflow, it is saturated to its maximum value (no roll over occurs) and the statistics data is stored in the memory (it is therefore possible to identify which field of which statistics word caused the interrupt). Besides, the statistics function stops and an interrupt is generated.

The following figure shows the update of the registers:

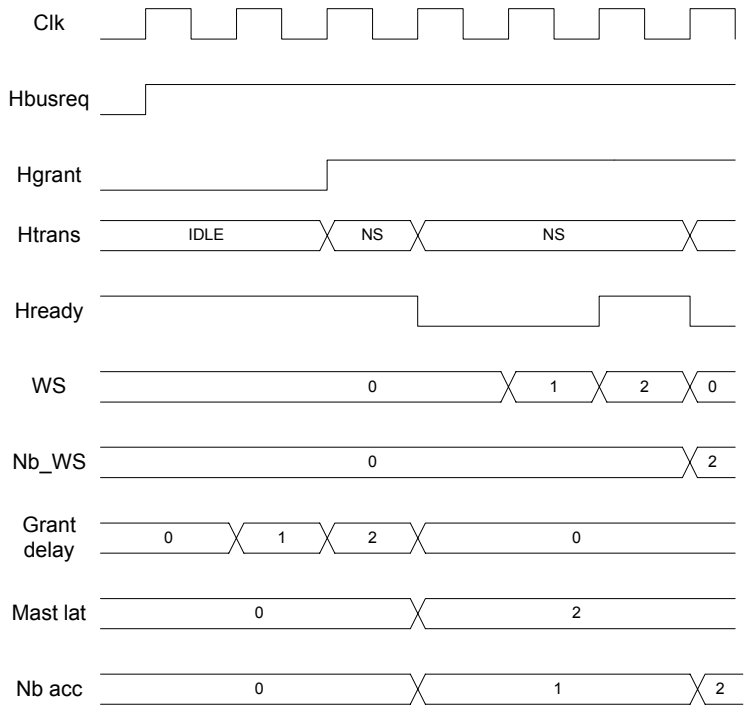

Figure 22: Update of the registers

The IPMON implements a statistics delay register (STAT_DEL_REG) to program a maximum integration time for statistics. This is a 32 bits counter which is decreased at the clock frequency and which stops the statistic function when reaching zero. With 32 bits, we can integrate statistics for more than 130 seconds with a frequency of 32 MHz.

9.2 TRACE BLOCK DESCRIPTION

The Trace Block traces SEQ and NON-SEQ accesses on the AHB bus. These data are stored in a Trace buffer.

The time tag value is reset at the beginning of each trace function activation.

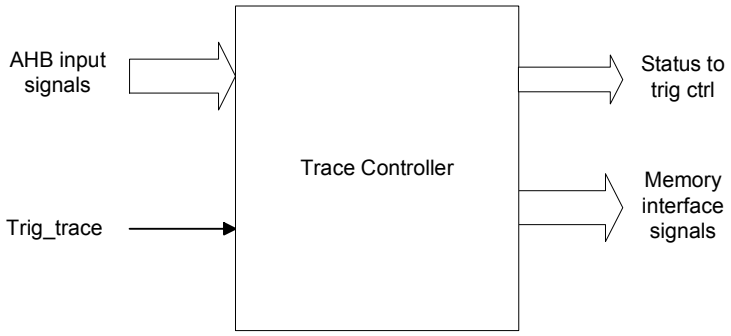

Figure 23: Trace controller block diagram

The size of the Trace buffer is programmable (using a constant) from 64 to 1024 words of 128 bits. The following figure shows the trace buffer arrangement (Figure 24):

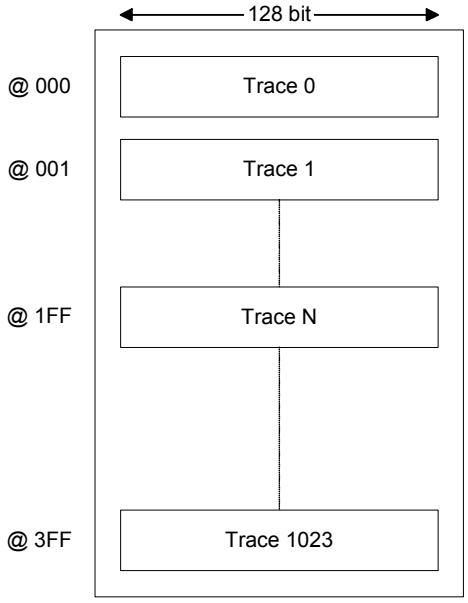

Figure 24: Trace buffer arrangement

9.3 MEMORY BLOCK DESCRIPTION

This block stores trace and statistics data into two different buffers.

These buffers are read and/or written by the Trace controller or by the Statistics controller and also through the AHB Slave interface.

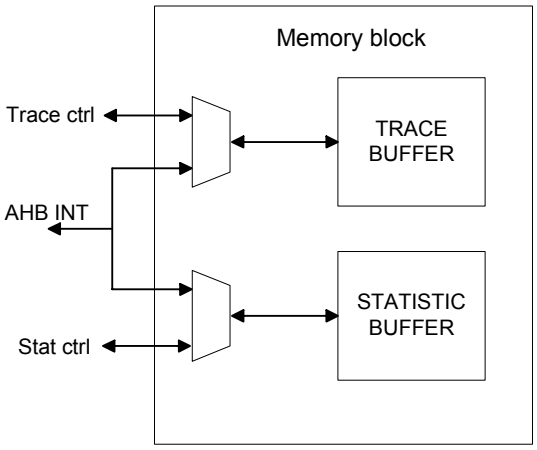

Figure 25: Memory block diagram

The Trace buffer is a single port memory because only one function (Trace controller or AHB slave interface) accesses this memory at a given time.

The Statistic buffer is a two port memory in order to chain read and write accesses.

A multiplexer is used to read or write into the buffers through the AHB slave interface, the Trace controller or the Statistic controller.

9.4 APB INTERFACE DESCRIPTION

The APB interface enables to configure trigger registers and to read status registers.

The IPMON has 23 registers (3 of them giving status information).

The write and read accesses are managed by APB signals. The following figure shows the APB interface architecture (Figure 26):

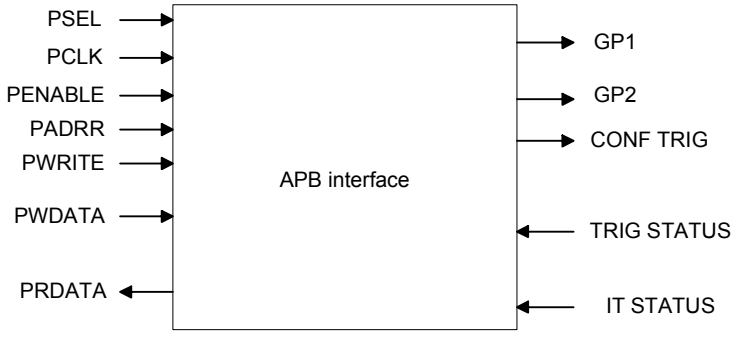

Figure 26: APB interface

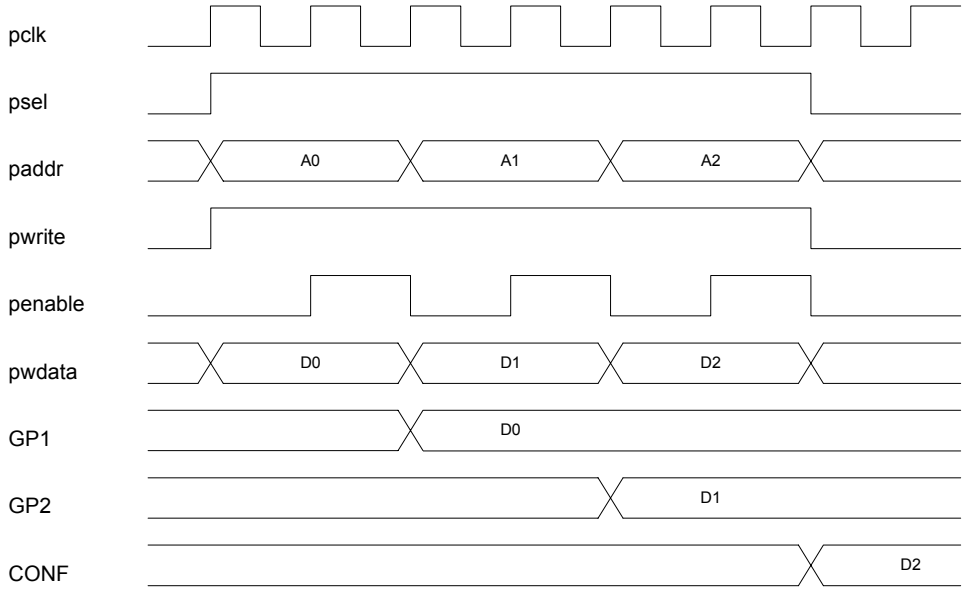

Figure 27: APB write access

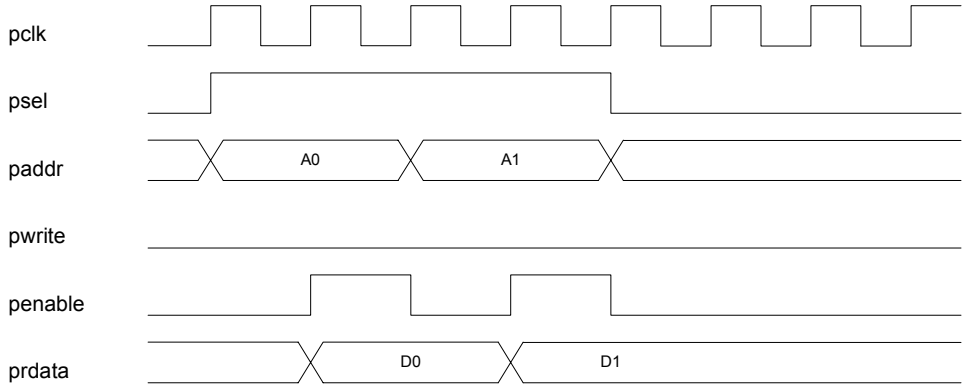

Figure 28: APB read access

9.5 AHB INTERFACE DESCRIPTION

The AHB interface enables to read trace and statistics data into the memory block module.

This interface is an AHB slave interface.

This interface is connected to the AHB bus and to the interface of the memory block (Figure 29).

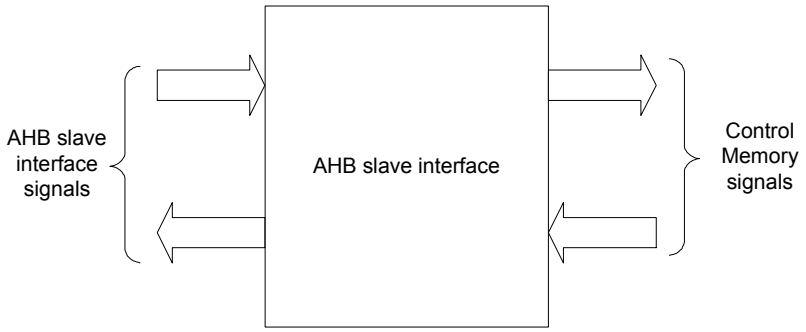

Figure 29: AHB Slave Interface

The AHB slave interface shall manage two different memory areas, corresponding to the Trace buffer and to the Statistics buffer. An internal selection signal ("Sel_ram") is used to address the appropriate memory (Figure 30).

Sel_ram	AHB Address OFFSET	definition
00/11	N.A.	Trace buffer and Statistic buffer connected on Trace controller and Statistic controller
01	0x00000 – 0x03FFF	Trace buffer trough AHB interface
10	0x20000 - 0x20FFF	Statistic buffer through AHB interface

Figure 30: AHB address mapping

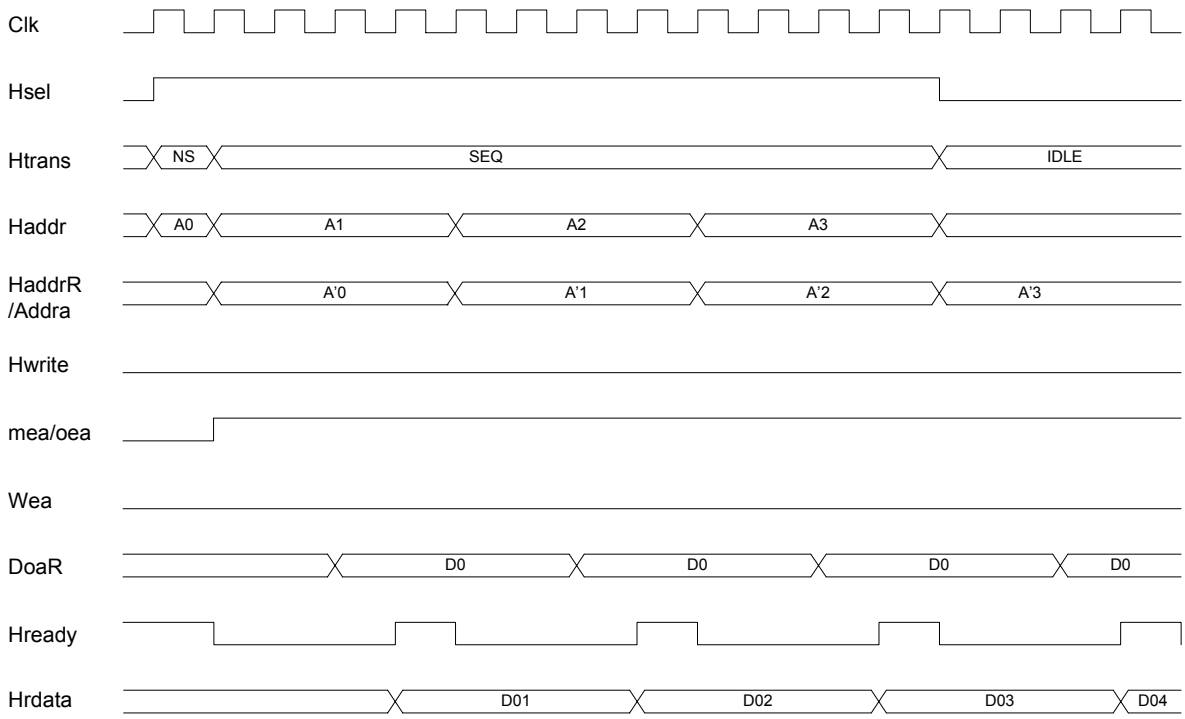

Figure 31: AHB Slave Interface access

9.6 TRIGGER BLOCK DESCRIPTION

This module defines the trigger conditions for the trace controller and for the statistics controller.

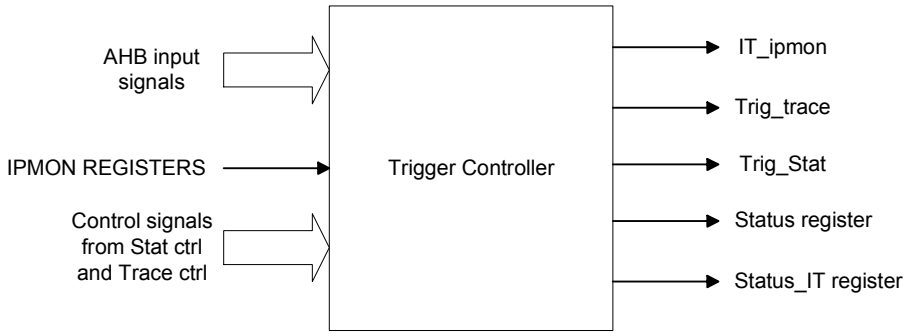

Figure 32: Trigger control interface

Figure 33 shows the relation between the trigger units and the trigger events. The number of Trigger Units is configurable between 1 and 4 according the constant Nt. Each of them can be configured to trig one of the 4 events generated. This configuration is done in the 4 events configuration registers

(IPMON_ST_CONF_Reg, IPMON_ET_CONF_Reg, IPMON_SS_CONF_Reg and IPMON_ES_CONF_Reg). These registers are look-up tables that allow any combination of and/or any trigger conditions.

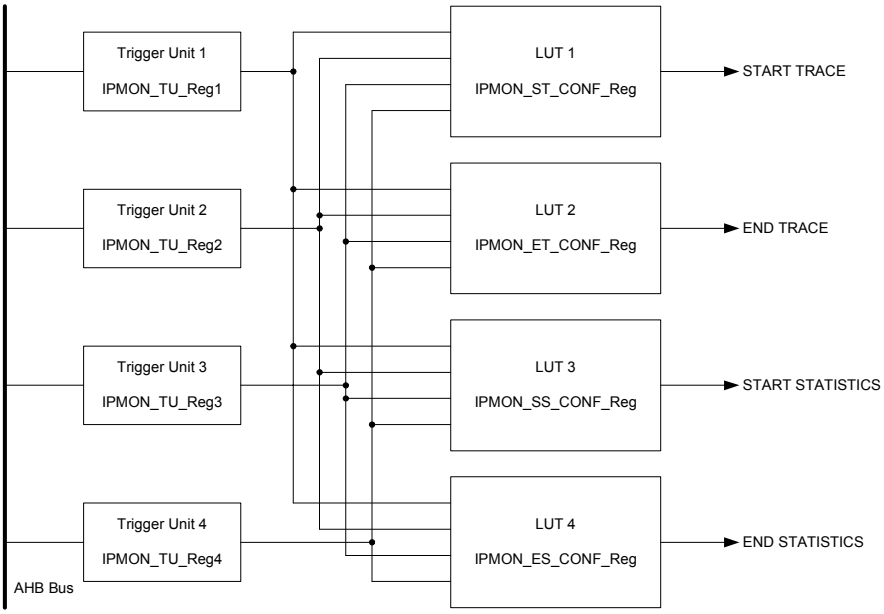

Figure 33: Trigger conditions and trigger events relation

Finally, Trace and Statistics functions are enabled as shown in Figure 34:

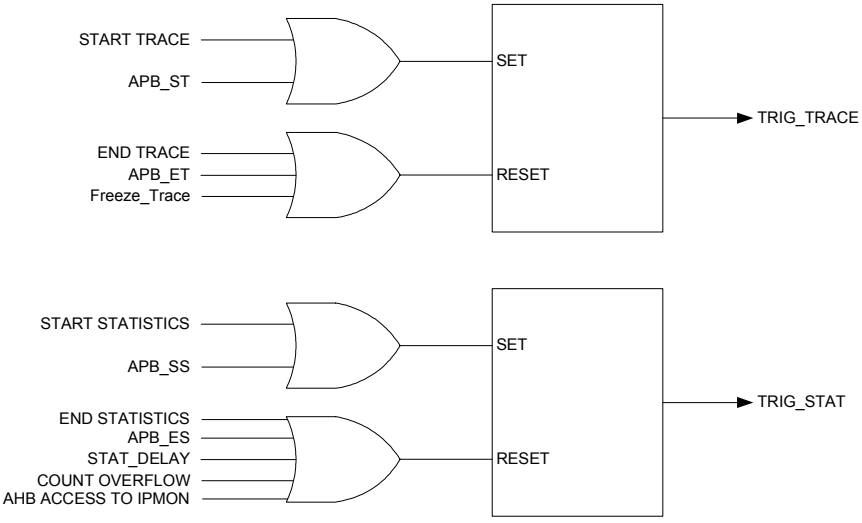

Figure 34: Trace and Statistics functions enable

Three status registers are defined in this block, two for the trigger statuses and the other for the interruption status.

The Interrupt status register is reset when read through the APB interface.

The Interruption signal is generated with an "OR" function of all the interruption status fields. This interruption signal is active high.

The interruption signal can be masked with the IPM_IT_MSK Register. This mask doesn't change the value of the IPM_IT_STATUS register.

The two trigger status register are updated as soon as a specific event occurs. For example, bits 0 to 3 of register IPMON_TRACE_TRIG_STATUS_Reg are updated when the START TRACE signal is activated.

10 TESTABILITY

No functional test mode is required.

A BIST test of memory will be implemented.

11 SEU PROTECTION

The RAM memories are not protected since it is not planed to use this function in flight.

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