ESA IP Cores Automated Benchmarking

ESA RFP/3-16019/19/NL/GLC/vr

(IUMA/0904- AO16019)

IP Cores mapping and implementation results

By

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21 marzo 2023

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DOCUMENT HISTORY

Date	Version	Author	Description	Status
09-09-2020	1.0	Yubal Barrios	Draft document	On-going
15-09-2020	1.1	Yubal Barrios	Results for SpaceFibre IP and error report for the PTME IP	On-going
16-09-2020	1.2	Roberto Sarmiento	Review	On-going
16-09-2020	1.3	Yubal Barrios	Review	On-going
17-09-2020	1.4	Yubal Barrios	Results included in Section 3.2.5	On-going
18-09-2020	1.5	Roberto Sarmiento	Review	Delivered MTR
07-10-2020	1.6	Yubal Barrios	Review	Delivered CCN1 PDR
16-12-2020	1.7	Yubal Barrios	Minor changes after PDR-CCN review	On-going
18-06-2021	1.8	Yubal Barrios	Results included for LEON2FT and NoC-IP.	On-going
21-06-2021	1.9	Diego Ventura	Results included for AHBR and FTADDRv0. Issues concerning PDEC3AMBA and PTCD added as well.	On-going
22-06-2021	2.0	Yubal Barrios	Review	On-going
15-11-2021	2.1	Roberto Sarmiento	Review	Delivered CCN1 FR
21-12-2021	2.2	Antonio Sánchez	Answer to FR-CCN actions	On-going
21-06-2022	2.3	Yubal Barrios	Inclusion of targets proposed in CCN2	On-going
30-06-2022	2.4	Yubal Barrios	Results updated for new targets	On-going
29-07-2022	2.5	Antonio Sanchez	Review. Acronyms table updated	On-going
02-08-2022	2.6	Yubal Barrios	Review	Delivered CCN2 PDR3
06-09-2022	2.7	Yubal Barrios	Changes after PDR3 RIDs	On-going
21-03-2023	2.8	Yubal Barrios	Review for publication on ESA website	Delivered

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LIST OF ACRONYMS

Acronym	Meaning
Abeto	Automated Benchmarking Tool
AHB	Advanced High-performance Bus
ALU	Arithmetic Logic Unit
AMBA	Advanced Microcontroller Bus Architecture
API	Application programming Interface
BRAVE	Big Reprogrammable Array for Versatile Environments
CAN	Controller Aera Network
DFF	D-type Flip Flop
DMR	Double Modular Redundancy
DSP	Digital Signal Processing
EDA	Electronic Design Automation
EDAC	Error Detection And Correction
FPGA	Field-Programmable Gate Array
FIFO	First-In, First-Out
FSM	Finite State Machine
GUI	Graphical User Interface
IP	Intellectual Property
I/O	Input/output
LUT	Look-Up Table
P&R	Place-and-Route
RAM	Random Access Memory
RTL	Register Transfer Level
RX	Receive channel
SoC	System-on-Chip
SpW	SpaceWire
TMR	Triple Modular Redundancy
TX	Transmit channel
VC	Virtual Channel
VHDL	VHSIC Hardware Description Language

1 INTRODUCTION

1.1 Document scope

This document corresponds to the deliverable *IP Cores mapping and implementation results* of the ESA Contract ESA RFP/3-16019/19/NL/GLC/vr entitled *ESA IP Cores Automated Benchmarking* .

1.2 Applicable documents

[AD-1] ESA, IPL-P & D/TEC. *ESA IP Cores automated benchmarking*. Statement of Work. ESA-TECEDM-SOW-TSS19-04ED. April 1st, 2019.

[AD-2] D1, *IP Cores database Potential Improvements*, IUMA, September 2019.

[AD-3] D4, *Abeto User Manual*, IUMA, September 2020.

1.3 Reference Documents

[RD-1] *NG-MEDIUM NX1H35AS Datasheet*, v2.2, NanoXplore, September 2020.

[RD-2] *NG-LARGE NX1H140TSP Datasheet,* v1.2, NanoXplore, September 2020.

[RD-3] *NG-ULTRA NX2H540TSC Datasheet,* v1.0, NanoXplore, July 2020.

[RD-4] *From eFPGA cores to RHBD System-on-Chip FPGA,* 4th SEFUW, NanoXplore, April 2018.

[RD-5] *NXmap User Manual,* v.3.0.0, NanoXplore, April 2020.

[RD-6] *Synopsys Synplify Pro, User Guide,* Synopsys Inc., January 2020.

[RD-7] *HurriCANe User Manual,* v.5.2.4, SITAEL, November 2011.

[RD-8] *SpaceWire CODEC IP, Implementation in (Radiation Tolerant) Actel FPGAs,* Issue 1.02, Space Technology Centre, University of Dundee, March 2009.

[RD-9] *Extended SHyLoC IP Datasheet*, IUMA, March 2019.

[RD-10] *D4-NoC IP datasheet*, version 1.6, Recore Systems, November 2017.

[RD-11] *DDR Controller Architecture Description and Preliminary Data sheet*, Issue 2.0, Cobham Gaisler, May 2020.

1.4 Document description

This document contains the mapping and implementation results of the ESA IP Cores currently integrated in the Abeto framework (see [AD-2]), targeting the novel NanoXplore FPGA family and alternative space-grade FPGAs.

2 INTRODUCTION TO THE NANOXPLORE ENVIRONMENT

2.1 NanoXplore FPGAs

The NanoXplore FPGA devices are a novel alternative in the space industry; this technology is supported by the Agency, since it offers a family of radiation-hardened reprogrammable FPGAs developed in Europe, avoiding the dependencies with foreign technologies that have dominated the space market during the last decades.

Different radiation hardening techniques are combined in the BRAVE FPGA family, such as a specific manufacturing process, Error Detection And Correction (EDAC) for dedicated memory blocks, Triple Modular Redundancy (TMR) flip-flops, Double Modular Redundancy (DMR) clock-tree, or a background scrubber to preserve the integrity of the FPGA memory configuration.

The youngest and smallest device of the Big Reprogrammable Array for Versatile Environments (BRAVE) family, named NG-MEDIUM, is based on 65nm CMOS technology and includes 35k 4-input Look-Up Tables (LUTs) and D type Flip-Flops (DFFs), 2.8 Mb of dedicated RAM and 112 Digital Signal Processing (DSP) blocks, among other elements [RD-1].

With higher offer of logic resources, the NG-LARGE is almost four times bigger than the NG-MEDIUM (137k LUTs and 129k DFFs), 9.4 Mb of embedded RAM and 384 dedicated DSPs, together with an ARM Cortex-R5 core [RD-2].

The biggest device of the family is the NG-ULTRA, which is a System-on-Chip (SoC) with almost four times the resources included in the NG-LARGE (536k LUT and 505k DFFs), 32.2 Mb of dedicated memory and 1344 DSPs. In addition, this device also integrates a Quad-core ARM Cortex-R52[RD-3].

A comparison of the different FPGAs of the BRAVE family is summarised in Figure 1, in terms of maximum clock frequency versus logic resources [RD-4].

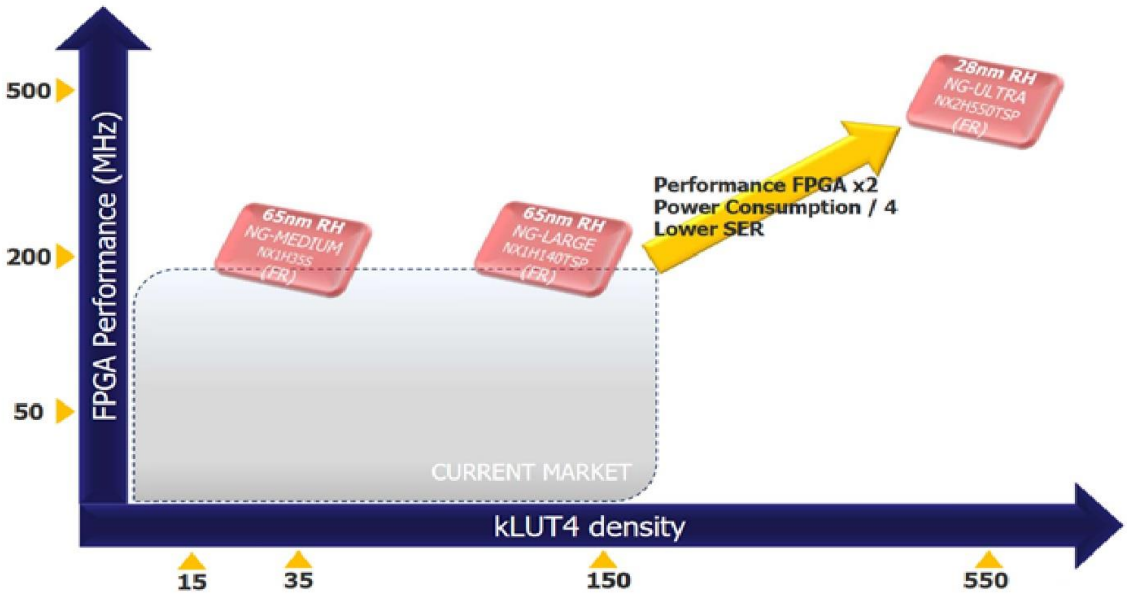

Figure 1: Comparison of BRAVE FPGAs.

2.2 NXmap synthesis tool

NXmap is the main software tool of the NanoXplore design suite, allowing to create, synthetize and implement a design on a BRAVE FPGA. It also provides static timing analysis and bitstream generation. The NXmap design suite includes both a GUI and a Python API, named NXpython. This software supports both VHDL and Verilog languages for the architecture descriptions, while the synthesis scripts use a Python-based syntax [RD-5]. A general overview of the design flow using the NXmap tools is shown in Figure 2.

In addition, other software tools are provided, such as NXcore, a GUI that presents all IP cores available for NanoXplore FPGA families, allowing to the user to graphically define the parameters of some IP cores and generate the preconfigured and encrypted VHDL code that can be used as input of NXmap; the NXscope, which works as an embedded logic analyser; and the NXbase2, a command-line tool able to upload bitstream files into the NanoXplore devices using a JTAG-based communication with the workstation (Nxboard is the GUI alternative).

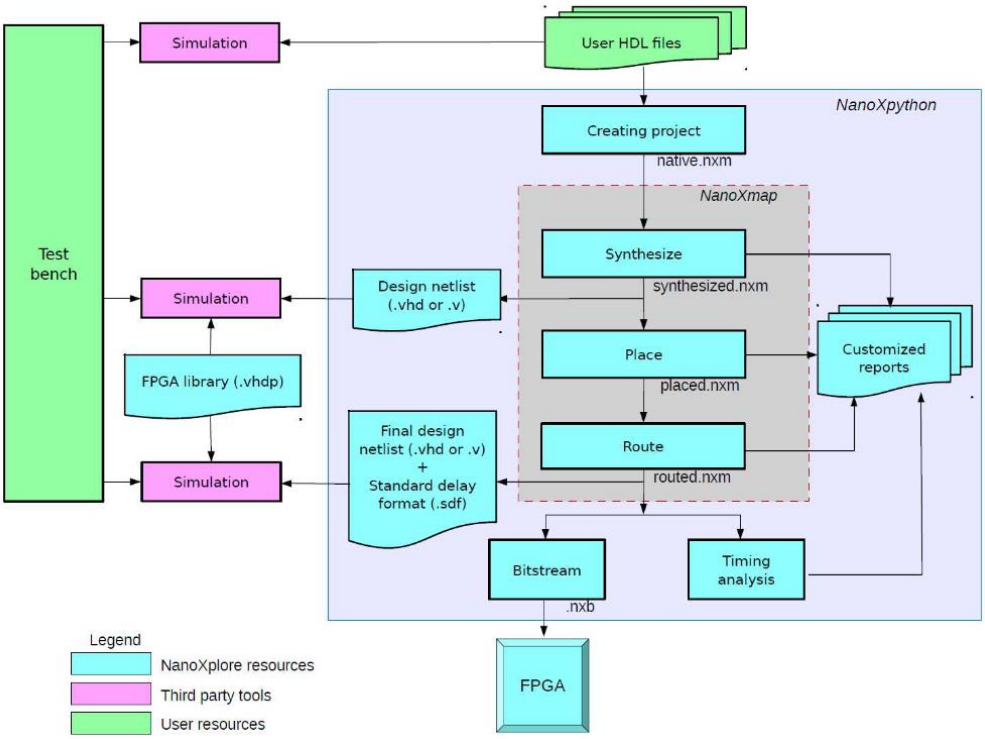

Figure 2: NanoXplore design flow [RD-5].

3 MAPPING AND IMPLEMENTATION RESULTS

The NG-MEDIUM FPGA is selected from the BRAVE family as implementation device for obtaining mapping results of the ESA IP Cores currently integrated in Abeto, since it provides enough resources to map most of those IPs. Nevertheless, the more complex IPs, such as SHyLoC, do not fit well in this device for some configurations; in these specific cases, results are also provided for NG-LARGE. Additionally, implementation results are provided for other well-known space-grade FPGAs, such as Xilinx Kintex UltraScale XQRKU060 and Microsemi RTG4 150.

Version 3.9.0.5 of the NanoXplore NXmap software tool has been used to obtain mapping results for the BRAVE family. For questions of flexibility and for the sake of reducing the acquisition time of these results, only the Python API (i.e., NXpython3) is used. On the other hand, mapping results for Xilinx Kintex UltraScale and Microsemi RTG4 technologies are obtained with Synopsys Synplify Premier P-2019.09-SP1.

The default configuration defined for each IP Core in the source code has been used for obtaining the synthesis results, unless otherwise stated. It is not guaranteed that these results are the best in terms of resources utilization or maximum clock frequency since alternative configurations can provide more optimized results.

3.1 Synthesis options

NXmap provides a high number of options to guide the synthesis and implementation stages. These options are detailed in [RD-5]. Table 3-1 summarises the options we have set to achieve the maximum clock frequency possible without compromising the logic resources utilization.

TABLE 3-1: MAIN OPTIONS DEFINED FOR THE SYNTHESIS AND P&R STAGES IN NXMAP

Option	Value	Description
'RoutingEffort'	'Medium'	Routing Optimization level (can be 'Low', 'Medium' or 'High'): • **Low:** no optimization • **Medium:** balanced optimizations • **High:** further optimizations but time consuming
'ManageUnconnectedOutputs'	'Ground'	Undriven outputs of HDL modules are treated as 'Error', 'Ground' or 'Power'.
'ManageUnconnectedSignals'	'Ground'	Undriven internal signals of HDL modules are treated as 'Error', 'Ground' or 'Power'.
'DefaultRAMMapping'	'RAM'	Default mapping of RAM (can be 'AUTO', 'RF', 'RAM' or 'RAM_ECC').
'MappingEffort'	'Medium'	Effort for an optimized mapping (can be 'Low', 'Medium' or 'High'): • **Low:** almost no optimization • **Medium:** balanced optimizations • **High:** almost all optimizations

'VariantAwareSynthesis'	'Yes'	If set to 'Yes' synthesis will automatically map to equivalent resource when specific resource is depleted. For example, using DSP when there is no more CY available (can be 'Yes' or 'No').

For Synplify, the main options considered during the synthesis are the ones reflected in Table 3-2. As for the NanoXplore devices, the option values are selected trying to maximize the clock frequency. In addition, Synplify provides several attributes that can be defined to guide the synthesis process [RD-6], whose application requires a deep knowledge of each particular IP. For this reason, these attributes are not used in this analysis.

TABLE 3-2: MAIN OPTIONS FOR THE SYNTHESIS IN SYNPLIFY

Option	Value	Description
'FSM Compiler'	'1'	Performs state machine optimization techniques, including re-encoding state representations.
'FSM Explorer'	'0	Automatically explores different encoding styles for state machines and picks the style best suited to your design.
'Resource Sharing'	'0'	In presence of mutually exclusive operators in a statement, the synthesis tool shares resources for those operators, including adders subtractors and multipliers.
'Pipelining'	'1'	Pipelining multipliers allows to operate at a faster frequency. It moves registers that follow a multiplier into it, provided that those registers are in the RTL code (not available for Microsemi RTG4).
'Retiming'	'1'	When enabled, this process automatically moves registers across combinational gates/LUTs to improve timing, while ensuring identical logic behaviour.

3.2 Resources utilization for the Abeto IP Cores

3.2.1 DummyIP

As it is explained in [AD-3], the dummyIP is a basic example of IP core that implements a Gray counter of configurable width. This is the reason why it only consumes a few logic resources, achieving at the same time a high clock frequency, as it is shown in Table 3-3, Table 3-4 and Table 3-5 for NG-MEDIUM, XQRKU060 and RTG4 150, respectively. These results have been obtained fixing the counter width to 4.

TABLE 3-3: MAPPING RESULTS FOR THE DUMMYIP ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	0 (0%)
Registers	32256	8 (0%)
Block RAMs (48Kb)	56	0 (0%)
DSP Blocks	112	0 (0%)
LUTs	32256	12 (0%)
Maximum Frequency (MHz)		266.88

TABLE 3-4: SYNTHESIS RESULTS FOR THE DUMMYIP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	11 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	12 (0%)
Maximum Frequency (MHz)		1267.6

TABLE 3-5: SYNTHESIS RESULTS FOR THE DUMMYIP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	0 (0%)
Sequential Cells	151824	7 (0%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	9 (0%)
Maximum Frequency (MHz)		394.8

3.2.2 EDAC IP (edac-0-7)

Results for the EDAC IP Core are presented in Table 3-6, Table 3-7 and Table 3-8 for NG-MEDIUM, XQRKU060 and RTG4 150, respectively. As it is also a simple IP, it consumes only some LUTs, not using any other element available on the target FPGAs. Only some registers are also consumed in the case of Xilinx XQRKU060 FPGA. Results in terms of clock frequency are not provided since this IP does not introduce delays by using sequential logic.

TABLE 3-6: MAPPING RESULTS FOR THE EDAC IP ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	0 (0%)
Registers	32256	0 (0%)
Block RAMs (48Kb)	56	0 (0%)
DSP Blocks	112	0 (0%)
LUTs	32256	224 (1%)
Maximum Frequency (MHz)		N/A

TABLE 3-7: SYNTHESIS RESULTS FOR THE EDAC IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	211 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	139 (0%)
Maximum Frequency (MHz)		N/A

TABLE 3-8: SYNTHESIS RESULTS FOR THE EDAC IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	17 (0%)
Sequential Cells	151824	0 (0%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	246 (0%)
Maximum Frequency (MHz)		N/A

3.2.3 CAN IP (HurriCANe_5.2.5)

The CAN controller provided by SITAEL aerospace has been mapped without considering the AMBA interface, in order to obtain the implementation results of the core itself. These results are summarised in Table 3-9, Table 3-10 and Table 3-11 for NG-MEDIUM, XQRKU060 and RTG4 150, respectively. These results are consistent with the ones provided for Xilinx and Actel FPGAs in [RD-7], considering the differences among the FPGA technologies.

TABLE 3-9: MAPPING RESULTS OF THE HURRICANE IP (V5.2.5) ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	157 (2%)
Registers	32256	500 (2%)
Block RAMs (48Kb)	56	0 (0%)
DSP Blocks	112	0 (0%)
LUTs	32256	742 (3%)
Maximum Frequency (MHz)		60.48

TABLE 3-10: SYNTHESIS RESULTS OF THE HURRICANE IP (V5.2.5) ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	554 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	718 (0%)
Maximum Frequency (MHz)		90.7

TABLE 3-11: SYNTHESIS RESULTS OF THE HURRICANE IP (V5.2.5) ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	97 (0%)
Sequential Cells	151824	529 (0%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	918 (1%)
Maximum Frequency (MHz)		47.8

3.2.4 SpaceWire codec - Dundee (spwb2-3)

The SpaceWire CODEC IP developed by the University of Dundee has been mapped with the configuration values summarized in Table 3-12. It consumes just a few logic resources, as reflected in Table 3-13, Table 3-14 and Table 3-15 for NG-MEDIUM, XQRKU060 and RTG4 150, respectively. These results are consistent with the ones presented in [RD-8] for the Actel RTAX1000S technology. In fact, higher frequencies are obtained for the clocks under analysis, since the RTAX1000S FPGA is a device belonging to older manufacturing processes and focusing on low-complexity solutions for the space industry. There are not high differences in the obtained results for NG-MEDIUM and RTG4, because of their similar internal resources architecture and availability.

TABLE 3-12: CONFIGURATION VALUES USED FOR MAPPING THE SPACEWIRE CODEC IP

Parameter	Value	Description
CFG_RXBUF_ADDRLEN	5	Amount of buffer space available to receive buffer determined by address length of buffer. Buffer size is $2^{rxbuf\_addrlen}$
CFG_RATE_NUMBITS	6	Number of bits used for transmitting rate and slow rate inputs
CFG_SLOWCLK_10MHZ	1	10MHz clock gives better resolution on the disconnect and state machine timers
CFG_DDROUT	1	Set to one if DDR outputs should be used
CFG_PIPELINE	1	Set to one if pipelining is used
CFG_SYNCRDCLK	1	Clock used to read from read buffer: (1) *sysclk* internally (0) RDCLK internally
CFG_DISCARD_EMPTY_PKT	1	Receiver discards empty packets: (1) Empty packets discarded from receiver (0) Empty packets not discarded and appear in receive buffer
CFG_SLOW_CE_SEL	0	Which slow clock enable, internal or external: (1) SLOW_CE is external (0) 10MHz clock enable is internally generated from CFG_SLOWRATE_SYSCLK
CFG_TICK_IN_KEEP	0	What to do with time-codes when the link is not running: (1) Keep time-codes until the link starts or another time-code is received (0) Discard time-codes until the link starts

TABLE 3-13: MAPPING RESULTS FOR THE SPACEWIRE CODEC IP ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	109 (2%)
Registers	32256	301 (1%)
Block RAMs (48Kb)	56	1 (2%)
DSP Blocks	112	0 (0%)
LUTs	32256	413 (2%)
Maximum Frequency (SYSCLK)(MHz)		91.13
Maximum Frequency (RX_CLK)(MHz)		195.46

TABLE 3-14: SYNTHESIS RESULTS FOR THE SPACEWIRE CODEC IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	371 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	400 (0%)
Maximum Frequency (SYSCLK)(MHz)		277.8
Maximum Frequency (RX_CLK)(MHz)		287.4

TABLE 3-15: SYNTHESIS RESULTS FOR THE SPACEWIRE CODEC IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	74 (0%)
Sequential Cells	151824	367 (0%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	502 (0%)
Maximum Frequency (SYSCLK)(MHz)		148.7
Maximum Frequency (RX_CLK)(MHz)		246.2

3.2.5 SpaceWire codec - Astrium (spw_v12)

On the other side, the SpaceWire IP Core provided by ASTRIUM has been mapped defining two different scenarios: with and without including the AMBA interface. The parameter values used for both cases are summarised in Table 3-16. While results for the baseline configuration are provided for the NG-MEDIUM device (Table 3-17), the alternative configuration which includes the AMBA interface has been synthesised on the NG-LARGE FPGA (Table 3-18), since the NG-MEDIUM has not enough I/Os for this particular case. Results for XQRKU060 and RTG4 150, shown in Table 3-19 and Table 3-20, respectively, take also into account the AMBA interface. Results obtained for the configuration that includes AMBA interface are consistent with the ones reported by the developers for the Xilinx XCV2000E FPGA, in terms of resources utilization and considering the inherent differences among FPGAs technologies.

TABLE 3-16: CONFIGURATION VALUES FOR MAPPING THE SPW_V12 CODEC IP

Parameter	Value	Description
RXFIFOABITS	6	Address width of the RX FIFO
TXFIFOABITS	3	Address width of the TX FIFO
AHBFIFOABITS	2	Address width of the AHB FIFO
RXFIFODBITS	9	Data width of the RX FIFO
TXFIFODBITS	9	Data width of the TX FIFO

AHBFIFODBITS	32	Data width of the AHB FIFO
RXFIFODEPTH	$2^6 = 64$	Number of words of the RX FIFO
TXFIFODEPTH	$2^3 = 8$	Number of words of the TX FIFO
AHBFIFODEPTH	$2^2 = 4$	Number of words of the AHB FIFO
CMAX	std_logic_vector((CWIDTH-1) downto 0)	N/A
CWIDTH	7	Size of the counter used to store the number of RX FIFO empty space
DELAYWIDTH	8	Size of the counter used for the 6.4 µs delay generation

TABLE 3-17: MAPPING RESULTS FOR THE SPW_V12 CODEC IP WITHOUT AMBA ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	100 (2%)
Registers	32256	359 (2%)
Block RAMs (48Kb)	56	0 (0%)
DSP Blocks	112	0 (0%)
LUTs	32256	385 (2%)
Maximum Frequency (clk_sw)(MHz)		89.5
Maximum Frequency (clk_txin)(MHz)		118.15
Maximum Frequency (d_in)(MHz)		162.68
Maximum Frequency (s_in)(MHz)		162.18

TABLE 3-18: MAPPING RESULTS FOR THE SPW_V12 CODEC IP WITH AMBA ON NG-LARGE

Parameters	Total Resources	Resources utilization
Carry Cells	32256	470 (2%)
Registers	129024	899 (1%)
Block RAMs (48Kb)	192	0 (0%)
DSP Blocks	384	0 (0%)
LUTs	129024	1742 (2%)
Maximum Frequency (clk_sw)(MHz)		64.06
Maximum Frequency (clk_txin)(MHz)		146.99
Maximum Frequency (d_in)(MHz)		168.12
Maximum Frequency (s_in)(MHz)		167.31

TABLE 3-19: SYNTHESIS RESULTS FOR THE SPW_V12 CODEC IP WITH AMBA ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	1160 (0%)
Block RAMs (36Kb)	1080	4 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	1472 (0%)
Maximum Frequency (clk_sw)(MHz)		187.9
Maximum Frequency (clk_txin)(MHz)		321.1
Maximum Frequency (d_in)(MHz)		423.7
Maximum Frequency (s_in)(MHz)		434.2

TABLE 3-20: SYNTHESIS RESULTS FOR THE SPW_V12 CODEC IP WITH AMBA ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	538 (0%)
Sequential Cells	151824	1162 (1%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	1861 (1%)
Maximum Frequency (clk_sw)(MHz)		132.8
Maximum Frequency (clk_txin)(MHz)		163.5
Maximum Frequency (d_in)(MHz)		194.0
Maximum Frequency (s_in)(MHz)		241.1

3.2.6 SpaceFibre codec (spfi-port-gaisler_v2_12)

The compile-time configuration of the SpaceFibre IP has been modified, setting the number of Virtual Channels (VCs) from 4 to 1. This change has been done after verifying that the version with 4 VCs does not fit well for any of the BRAVE FPGAs (including the NG-ULTRA), since they do not have enough I/O pads. Even for this simple configuration, results are provided for the NG-LARGE device, being not possible to map the design in the NG-MEDIUM for the small quantity of available I/O pins (i.e., 374). The rest of configuration values are summarised in Table 3-21, while the obtained results are presented in Table 3-22, Table 3-23 and Table 3-24 for NG-LARGE, XQRKU060 and RTG4 150, respectively. The resources utilization for NG-LARGE and RTG4 is quite similar, results that are supported by the equivalent internal architecture of both FPGAs.

TABLE 3-21: CONFIGURATION VALUES FOR MAPPING THE SPFI-PORT-GAISLER_V2_12 CODEC IP

Parameter	Value	Description
Global Configuration Options		
g_use_async_rst	False	If set, all resets are asynchronous, otherwise synchronous.
g_tech	0	This generic can be used for technology-specific internal components such as memories.
Interface Layer		
g_use_8b10b	True	If set, internal 8B10B encoding and decoding is activated.
g_use_sep_txclk	False	If set, the SerDes transmission clock is decoupled from the SpaceFibre port clock. An additional transmit buffer is instantiated for this reason.
g_16_20_bit_mode	False	If set, the SerDes interface is 16+2 bit (without 8B10B) or 20 bit (with 8B10B) wide instead of 36/40 bit. If set, *g_use_sep_txclk* must also be set.
Lane Layer		
g_ticks_2us	125	Clock ticks corresponding to 2 µs.
g_tx_skip_freq	5000	Frequency of SKIP word transmission in clock cycles.
g_prbs_init1	True	If set, the INIT1 sequence during lane initialisation is embedded into a stream of pseudo-random numbers.
Retry Layer		
g_depth_rbuf_data	8	Log(Depth) of the data retry buffer.
g_depth_rbuf_fct	4	Log(Depth) of the FCT retry buffer.
g_depth_rbuf_bc	8	Log(Depth) of the broadcast retry buffer.
Virtual Channel Layer		
g_no_vc	1	Number of virtual channels.
g_depth_vc_rx_buf	10	Log(Depth) of virtual channel input buffer.
g_depth_vc_tx_buf	10	Log(Depth) of virtual channel output buffer.
g_remote_fct_cnt_max	9	Width of the remote FCT counter.
g_width_bw_credit	20	Width of the bandwidth credit counter.
g_min_bw_credit	52428	Minimum bandwidth credit threshold limit.
g_idle_time_limit	62500	Bandwidth idle time limit in clock cycles.

TABLE 3-22: MAPPING RESULTS FOR THE SPFI-PORT-GAISLER_V2_12 CODEC IP ON NG-LARGE

Parameters	Total Resources	Resources utilization
Carry Cells	32256	516 (2%)
Registers	129024	1899 (2%)
Block RAMs (48Kb)	192	12 (7%)
DSP Blocks	384	0 (0%)
LUTs	129024	4933 (4%)
Maximum Frequency (clk)(MHz)		48.57
Maximum Frequency (se_rx_clk)(MHz)		65.24

TABLE 3-23: SYNTHESIS RESULTS FOR THE SPFI-PORT-GAISLER_V2_12 CODEC IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	2236 (0%)
Block RAMs (36Kb)	1080	5 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	3668 (1%)
Maximum Frequency (clk)(MHz)		210.7
Maximum Frequency (se_rx_clk)(MHz)		227.8

TABLE 3-24: SYNTHESIS RESULTS FOR THE SPFI-PORT-GAISLER_V2_12 CODEC IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	480 (0%)
Sequential Cells	151824	2254 (1%)
Block RAMs (64x18)	209	6 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	4666 (3%)
Maximum Frequency (clk)(MHz)		99.3
Maximum Frequency (se_rx_clk)(MHz)		125.6

3.2.7 SHyLoC 2.0

Implementation results of the SHyLoC 2.0 CSCSDS123 IP core are provided with different sets of generic parameters. A set of baseline configuration values is common to all the preliminary mapping cases. The parameter EN_RUNCFG and those related to the image configuration are varied in such a way that situations are created that are representative of different acquisition

scenarios (multispectral, hyperspectral and ultraspectral), as shown in Table 3-25. The configurations for mapping are selected based in the acquisition scenarios in the five possible CCSDS 123 predictor architectures (BIP; BIP-MEM; BSQ; BIL and BIL-MEM). For more details about the used configuration sets, see [RD-9].

Since some of the configuration sets do not fit well in the NG-MEDIUM technology (Table 3-26), results are also provided for the NG-LARGE device (Table 3-27). This situation is repeated for Microsemi RTG4, where high-demanding memory architectures do not fit well on the available resources (Table 3-29). Grey cells mean that not enough memory resources are available in that specific technology for those set of parameters, not providing the synthesis tool the use of the rest of logic resources in the case of the BRAVE FPGA family. In addition, synthesis results have been obtained for Xilinx XQRKU060, which are shown in Table 3-28.

TABLE 3-25: CCSDS123 IP – ACQUISITION SCENARIOS FOR MAPPING

IMAGE	EN_RUNCFG	Nx_GEN	Ny_GEN	Nz_GEN	D_GEN
MULTISPECTRAL	0	1024	1024	6	8
HYPERSPECTRAL	0	512	680	224	16
ULTRASPECTRAL	0	90	135	1501	14
RUNTIME CONFIG	1	512 (512)*	680 (1024)*	224 (256)*	16

** The depth of all FIFOs in the design is constrained to a power of two.*

TABLE 3-26: CCSDS123 IP- MAPPING RESULTS ON NG-MEDIUM NX1H35S

Parameters	Total Resources	Set 1	Set 2	Set 3	Set 4	Set 4-e
Carry Cells	8064	2360 (30%)	2778 (35%)	2936 (37%)	2743 (35%)	3114 (39%)
Registers	32256	2713 (9%)	3482 (11%)	3120 (10%)	3124 (10%)	3896 (13%)
Block RAMs (48Kb)	56	33 (59%)	34 (61%)	27 (49%)	43 (77%)	44 (79%)
DSP Blocks	112	6 (6%)	6 (6%)	4 (4%)	6 (6%)	6 (6%)
LUTs	32256	4096 (13%)	5522 (18%)	4839 (16%)	4340 (14%)	5753 (18%)
Maximum Frequency (Clk_AHB) (MHz)		---	32.5	33.2	---	24.0
Maximum Frequency (Clk_S) (MHz)		35.5	35.9	33.9	31.9	33.5
Parameters	**Total Resources**	**Set 5**	**Set 6**	**Set 7**	**Set 8**	**Set 8-e**
Carry Cells	8064		3834 (48%)	3653 (46%)		4128 (52%)
Registers	32256		3951 (13%)	3414 (11%)		4370 (14%)
Block RAMs (48Kb)	56	95 (169%)	34 (61%)	27 (49%)	105 (187%)	44 (79%)
DSP Blocks	112		6 (6%)	4 (4%)		6 (6%)
LUTs	32256		6550 (21%)	5720 (18%)		6766 (21%)
Maximum Frequency (Clk_AHB) (MHz)			27.9	32.9		25.8
Maximum Frequency (Clk_S) (MHz)			30.1	32.4		26.1

Parameters	Total Resources	Set 9	Set 10	Set 11	Set 12	Set 12-e
Carry Cells	8064		3857 (48%)	3567 (45%)		4126 (52%)
Registers	32256		3956 (13%)	3343 (11%)		4318 (14%)
Block RAMs (48Kb)	56	143 (255%)	34 (61%)	27 (49%)	153 (273%)	44 (79%)
DSP Blocks	112		6 (6%)	4 (4%)		6 (6%)
LUTs	32256		6219 (20%)	5437 (17%)		6377 (20%)
Maximum Frequency (Clk_AHB) (MHz)			28.7	31.0		28.3
Maximum Frequency (Clk_S) (MHz)			29.4	29.9		29.0
Parameters	Total Resources	Set 13	Set 14	Set 15	Set 16	Set 16-e
Carry Cells	8064		4440 (56%)	4256 (53%)		4729 (59%)
Registers	32256		4574 (15%)	4001 (13%)		4967 (16%)
Block RAMs (48Kb)	56	97 (173%)	36 (65%)	29 (52%)	107 (191%)	46 (83%)
DSP Blocks	112		8 (8%)	6 (6%)		8 (8%)
LUTs	32256		8168 (26%)	7510 (24%)		8396 (27%)
Maximum Frequency (Clk_AHB) (MHz)			26.4	31.3		29.1
Maximum Frequency (Clk_S) (MHz)			29.2	30.0		24.9

TABLE 3-27: CCSDS123 IP - MAPPING RESULTS ON NG-LARGE NX1H140TSP

Parameters	Total Resources	Set 1	Set 2	Set 3	Set 4	Set 4-e
Carry Cells	32256	2360 (8%)	2778 (9%)	2936 (10%)	2743 (9%)	3114 (10%)
Registers	129024	2713 (3%)	3482 (3%)	3120 (3%)	3124 (3%)	3896 (4%)
Block RAMs (48Kb)	192	33 (18%)	34 (18%)	27 (15%)	43 (23%)	44 (23%)
DSP Blocks	384	6 (2%)	6 (2%)	4 (2%)	6 (2%)	6 (2%)
LUTs	129024	4084 (4%)	5524 (5%)	4843 (4%)	4339 (3%)	5746 (5%)
Maximum Frequency (Clk_AHB) (MHz)		---	27.5	40.5	---	30.8
Maximum Frequency (Clk_S) (MHz)		43.1	42.9	36.6	35.8	38.4
Parameters	Total Resources	Set 5	Set 6	Set 7	Set 8	Set 8-e
Carry Cells	32256	3353 (11%)	3834 (12%)	3653 (12%)	3678 (12%)	4128 (13%)
Registers	129024	3165 (3%)	3951 (4%)	3414 (3%)	3581 (3%)	4370 (4%)
Block RAMs (48Kb)	192	95 (50%)	34 (18%)	27 (15%)	105 (55%)	44 (23%)

DSP Blocks	384	6 (2%)	6 (2%)	4 (2%)	6 (2%)	6 (2%)
LUTs	129024	4881 (4%)	6538 (6%)	5734 (5%)	5348 (5%)	6784 (6%)
Maximum Frequency (Clk_AHB) (MHz)		---	27.7	34.3	---	27.1
Maximum Frequency (Clk_S) (MHz)		32.5	30.8	36.9	29.4	29.8
Parameters	**Total Resources**	**Set 9**	**Set 10**	**Set 11**	**Set 12**	**Set 12-e**
Carry Cells	32256	3333 (11%)	3857 (12%)	3567 (12%)	3634 (12%)	4126 (13%)
Registers	129024	3181 (3%)	3956 (4%)	3343 (3%)	3540 (3%)	4318 (4%)
Block RAMs (48Kb)	192	143 (75%)	34 (18%)	27 (15%)	153 (80%)	44 (23%)
DSP Blocks	384	6 (2%)	6 (2%)	4 (2%)	6 (2%)	6 (2%)
LUTs	129024	4812 (4%)	6222 (5%)	5428 (5%)	4912 (4%)	6376 (5%)
Maximum Frequency (Clk_AHB) (MHz)		---	28.4	28.8	---	30.3
Maximum Frequency (Clk_S) (MHz)		33.1	30.2	31.9	30.1	24.9
Parameters	**Total Resources**	**Set 13**	**Set 14**	**Set 15**	**Set 16**	**Set 16-e**
Carry Cells	32256	3855 (12%)			4198 (14%)	
Registers	129024	3674 (3%)			4064 (4%)	
Block RAMs (48Kb)	192	97 (51%)			107 (56%)	
DSP Blocks	384	8 (3%)			8 (3%)	
LUTs	129024	6943 (6%)			7058 (6%)	
Maximum Frequency (Clk_AHB) (MHz)		65.5			68.9	
Maximum Frequency (Clk_S) (MHz)		31.7			30.8	

TABLE 3-28: CCSDS123 IP - SYNTHESIS RESULTS ON XQRKU060

Parameters	Total Resources	Set 1	Set 2	Set 3	Set 4	Set 4-e
Block RAMs	1080	2 (0%)	0 (0%)	2 (0%)	5 (0%)	3 (0%)
DSP48	2760	8 (0%)	8 (0%)	6 (0%)	8 (0%)	8 (0%)
Registers	663360	2226 (0%)	2907 (0%)	2810 (0%)	2689 (0%)	3499 (0%)
LUTs	331680	3283 (1%)	3972 (1%)	3863 (1%)	3816 (1%)	4466 (1%)
Maximum Frequency (Clk_AHB) (MHz)		---	305.6	174.1	---	153.5
Maximum Frequency (Clk_S) (MHz)		149.4	157.6	139.5	166.4	164.1

Parameters	Total Resources	Set 5	Set 6	Set 7	Set 8	Set 8-e
Block RAMs	1080	74 (7%)	10 (1%)	2 (0%)	74 (7%)	10 (1%)
DSP48	2760	12 (0%)	12 (0%)	7 (0%)	10 (0%)	10 (0%)
Registers	663360	2475 (0%)	3230 (0%)	3213 (0%)	3111 (0%)	3954 (1%)
LUTs	331680	3959 (1%)	4628 (1%)	4581 (1%)	4754 (1%)	5470 (2%)
Maximum Frequency (Clk_AHB) (MHz)		---	301.0	190.8	---	153.8
Maximum Frequency (Clk_S) (MHz)		151.6	150.3	140.7	160.6	152.7
Parameters	Total Resources	Set 9	Set 10	Set 11	Set 12	Set 12-e
Block RAMs	1080	123 (11%)	11 (1%)	2 (0%)	123 (11%)	11 (1%)
DSP48	2760	12 (0%)	12 (0%)	8 (0%)	10 (0%)	10 (0%)
Registers	663360	2445 (0%)	3210 (0%)	3117 (0%)	3017 (0%)	3865 (1%)
LUTs	331680	3920 (1%)	4605 (1%)	4506 (1%)	4605 (1%)	5247 (2%)
Maximum Frequency (Clk_AHB) (MHz)		---	264.6	177.1	---	144.7
Maximum Frequency (Clk_S) (MHz)		149.7	138.2	119.9	152.8	126.2
Parameters	Total Resources	Set 13	Set 14	Set 15	Set 16	Set 16-e
Block RAMs	1080	74 (7%)	10 (1%)	2 (0%)	74 (7%)	10 (1%)
DSP48	2760	13 (0%)	13 (0%)	10 (0%)	13 (0%)	13 (0%)
Registers	663360	3092 (0%)	4048 (1%)	3946 (1%)	3573 (1%)	4587 (1%)
LUTs	331680	5271 (2%)	5895 (2%)	5840 (2%)	5844 (2%)	6565 (2%)
Maximum Frequency (Clk_AHB) (MHz)		571.3	267.7	190.5	618.9	154.6
Maximum Frequency (Clk_S) (MHz)		151.6	149.8	135.1	148.0	149.8

TABLE 3-29: CCSDS123 IP - SYNTHESIS RESULTS ON RTG4 150

Parameters	Total Resources	Set 1	Set 2	Set 3	Set 4	Set 4-e
Carry Cells	151824	2017 (1%)	2288 (1%)	2489 (2%)	2179 (1%)	2420 (2%)
Sequential Cells	151824	2485 (2%)	3081 (2%)	2800 (2%)	2755 (2%)	3413 (2%)
Block RAMs (1Kx18 + 64x18)	209 + 210	4+31 (8%)	0+33 (8%)	1+25 (6%)	10+38 (11%)	6+40 (11%)
DSP Blocks	462	7 (2%)	7 (2%)	7 (2%)	7 (2%)	7 (2%)
LUTs	151824	5317 (4%)	6198 (4%)	6276 (4%)	5639 (4%)	6983 (5%)
Maximum Frequency (Clk_AHB) (MHz)		---	101.5	81.7	---	72.0

Maximum Frequency (Clk_S) (MHz)		72.8	83.6	80.4	74.2	69.6
Parameters	Total Resources	Set 5	Set 6	Set 7	Set 8	Set 8-e
Carry Cells	151824	3604 (2%)	3299 (2%)	3044 (2%)	3764 (2%)	3376 (2%)
Sequential Cells	151824	3076 (2%)	3713 (2%)	3181 (2%)	3438 (2%)	4128 (3%)
Block RAMs (1Kx18 + 64x18)	209 + 210	129+62 (46%)	1+64 (16%)	1+36 (9%)	135+65 (48%)	7+67 (18%)
DSP Blocks	462	13 (3%)	13 (3%)	11 (2%)	13 (3%)	13 (3%)
LUTs	151824	7935 (5%)	7985 (5%)	7382 (5%)	8175 (5%)	8743 (6%)
Maximum Frequency (Clk_AHB) (MHz)		---	95.9	85.2	---	76.3
Maximum Frequency (Clk_S) (MHz)		64.6	79.9	80.8	56.6	76.2
Parameters	Total Resources	Set 9	Set 10	Set 11	Set 12	Set 12-e
Carry Cells	151824	5092 (3%)	4162 (3%)	2954 (2%)	4125 (3%)	3290 (2%)
Sequential Cells	151824	2994 (2%)	3615 (2%)	3079 (2%)	3172 (2%)	3844 (3%)
Block RAMs (1Kx18 + 64x18)	209 + 210	266+212 (114%)	10+214 (102%)	0+30 (7%)	275+30 (132%)	19+32 (12%)
DSP Blocks	462	7 (2%)	7 (2%)	6 (2%)	7 (2%)	7 (2%)
LUTs	151824	9661 (6%)	8878 (6%)	7182 (5%)	8774 (6%)	8278 (5%)
Maximum Frequency (Clk_AHB) (MHz)		---	84.8	79.5	---	82.5
Maximum Frequency (Clk_S) (MHz)		69.2	69.4	79.5	69.3	76.6
Parameters	Total Resources	Set 13	Set 14	Set 15	Set 16	Set 16-e
Carry Cells	151824	3960 (2%)	3665 (2%)	3447 (2%)	4078 (2%)	3756 (2%)
Sequential Cells	151824	3641 (2%)	4397 (3%)	3789 (2%)	3977 (2%)	4787 (3%)
Block RAMs (1Kx18 + 64x18)	209 + 210	129+64 (46%)	1+66 (16%)	1+38 (9%)	135+67 (48%)	7+69 (18%)
DSP Blocks	462	16 (3%)	16 (3%)	14 (3%)	16 v	16 (3%)
LUTs	151824	10027 (7%)	10268 (7%)	9648 (6%)	10293 (7%)	10877 (7%)
Maximum Frequency (Clk_AHB) (MHz)		132.8	96.3	85.3	132.8	76.3
Maximum Frequency (Clk_S) (MHz)		66.1	79.6	74.2	73.9	74.2

3.2.8 Packet Telemetry Encoder (ptme-nTE-08-e)

Mapping results for Packet Telemetry Encoder (PTME) IP, currently included in Abeto, are not reflected in this document. An error is reported in NXMap at the beginning of the implementation stage, related to the number of I/O pads. The number of I/Os presented in this IP is 1417 using the standard configuration and 1007 if the FPGA-targeted configuration is applied (results obtained synthesising the design for the Xilinx Kintex UltraScale XCKU040 in Synopsys Synplify Premier). In addition, it is not possible to reduce the number of I/O pads even if the IP configuration is simplified, since the NXmap tool is not able to bypass the non-used IPs (only it is possible to select between reporting an error when a I/O is not used, aborting the mapping process, or connecting it to ground/pull-up/pull-down).

Nevertheless, preliminary results in terms of resources utilization are provided for NG-LARGE at the end of the synthesis stage, which are shown in Table 3-30. These results correspond to the FPGA-targeted configuration. As it is expected, timing information is not provided by the tool in this stage.

On the other hand, for the technologies synthetized with Synplify Premier timing results are provided, in addition to the resources utilization. These results are shown in Table 3-31 and Table 3-32 for XQRKU060 and RTG4 150, respectively. As it can be observed, the logic resources utilization is similar, independently of the target FPGA.

TABLE 3-30: SYNTHESIS RESULTS FOR THE PTME IP ON NG-LARGE.

Parameters	Total Resources	Resources utilization
Carry Cells	32256	769 (3%)
Registers	129024	1923 (2%)
Block RAMs (48Kb)	192	0 (0%)
DSP Blocks	384	0 (0%)
LUTs	129024	2344 (2%)

TABLE 3-31: SYNTHESIS RESULTS FOR THE PTME IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	1058 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	2014 (0%)
Maximum Frequency (MHz)		101.0

TABLE 3-32: SYNTHESIS RESULTS FOR THE PTME IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	454 (0%)
Sequential Cells	151824	2400 (2%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)

LUTs	151824	2641 (2%)
Maximum Frequency (MHz)		66.2

3.2.9 LEON2FT microprocessor (leon2ft_2020.1_daifpu_swar)

IMPLEMENTATION RESULTS FOR LEON2FT RAD-HARD MICROPROCESSOR ARE SHOWN IN TABLE 3-33. IN THIS CASE, NG-MEDIUM HAS BEEN SELECTED AS TARGET DEVICE FROM THE BRAVE FAMILY, SINCE THE IP DATABASE INCLUDES A PYTHON SCRIPT TO DIRECTLY RUN THE SYNTHESIS ON NANOXPLORE NXMAP TARGETING THIS FPGA (THE SCRIPT IS LOCATED AT *BOARDS/ NX-DK625V2*). SOME SYNPLIFY PROJECTS ARE PROVIDED FOR OTHER FPGA TECHNOLOGIES, WHICH HAVE BEEN ADAPTED TO TARGET XQRKU060 AND RTG4 150, WHOSE RESULTS ARE REFLECTED IN

Table 3-34 and Table 3-35, respectively. The desired configuration is selected by launching the *xconfig* tool included into the IP database, which generates a VHDL file denoted as *device.vhd*. Concretely, the LEON2FT has been synthetized with the configuration summarized next:

- SWAR extension enabled with an ALU with a slice width of 16.
- Floating Point Unit, selecting by default the DAIFPU-DUAL-DPSP implementation.
- MMU in combined mode.
- An AMBA AHB Master enabled.
- TMR in internal registers and clocks.
- External memory EDAC enabled.

It is remarkable that NXmap is not able to efficiently balance the use of DSPs and logic to perform complex arithmetic operations, such as the ones computed by the Floating-Point Unit. That balance is properly done by the Synplify tool for the target FPGAs that are not part of the BRAVE family.

TABLE 3-33: MAPPING RESULTS FOR THE LEON2FT ON NG-MEDIUM

Parameters	Total Resources	Resources utilization
Carry Cells	8064	866 (11%)
Registers	32256	12033 (38%)
Block RAMs (48Kb)	56	16 (29%)
DSP Blocks	112	0 (0%)
LUTs	32256	12410 (39%)
Maximum Frequency (clk_i)(MHz)		46.8

TABLE 3-34: SYNTHESIS RESULTS FOR THE LEON2FT ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	6572 (1%)
Block RAMs (36Kb)	1080	26 (2%)
DSP Blocks	2760	13 (0%)
LUTs	331680	17935 (5%)
Maximum Frequency (MHz)		235.3

TABLE 3-35: SYNTHESIS RESULTS FOR THE LEON2FT ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	3698 (2%)
Sequential Cells	151824	7007 (5%)
Block RAMs (64x18)	209	16 (8%)
DSP Blocks	462	19 (4%)
LUTs	151824	26054 (17%)
Maximum Frequency (MHz)		113.8

3.2.10 Network-on-Chip (NoCIP_v1)

Mapping results for the NoC-IP are just provided for the BRAVE family by defining the NG-LARGE-EMBEDDED part, which isolates the logic resources utilization from the I/O ring, not defining the pads. The simplest possible configuration has been defined, which implements a 2x2 mesh without AMBA AHB support. Preliminary results are summarised in Table 3-36.

TABLE 3-36: SYNTHESIS RESULTS FOR THE NOC-IP ON NG-LARGE

Parameters	Total Resources	Resources utilization
Carry Cells	32256	0 (0%)
Registers	129024	3055 (3%)
Block RAMs (48Kb)	192	160 (84%)
DSP Blocks	384	0 (0%)
LUTs	129024	13024 (11%)
Maximum Frequency (clkm)(MHz)		30.91

Synthesis results show a high memory consumption of 160 block RAMs. Analysing the IP documentation [RD-10], each instance of the NoC IP implements a considerable number of small FIFOs, with a depth of 2 by default. According to synthesis reports, these FIFOs are implemented using independent block RAMs, which is suboptimal considering the reduced size of each FIFO. To sum up, synthesis performed by NanoXMap with the default settings is suboptimal. For this

IP core, the synthesis tool should be instructed to implement small FIFOs as registers since the registers consumption is very low, thus saving the block RAM resources for other memories in the design.

3.2.11 SpaceWire Node (SpWNodeIP_v1)

The SpW Node IP has not been successfully mapped since multiple issues appeared during the synthesis. First, an issue is reported about the maximum number of I/O pads available in the target device in the case of the NG-LARGE FPGA, which was solved by changing the configuration of the IP to a simpler one. Then, errors are provided during the compilation of the VHDL source code, reporting syntax errors in multiple *force* and *if/else* instructions. Because of these issues are not related to the synthesis process itself and are associated to the source code, which require IP developers' actions that are out of our scope, this IP is not finally considered to be mapped.

3.2.12 AHB-to-AHB Bridge (AHBR)

Implementation results for AHB-to-AHB Bridge (AHBR) IP on NG-LARGE are shown in Table 3-37. This IP has been mapped considering the initial design without any kind of modification or alternative configuration. After comparing obtained synthesis results with the ones provided in the AHBR IP documentation for RTAX400s_cqfp352-s, few significant differences were found. Whilst the number of combinational cells used is bigger for the RTAX synthesis, sequential cells and block RAMs numbers are identical for both implementations, same as maximum frequency. Results obtained for XQRKU060 and RTG4 150, which are reflected in Table 3-38 and Table 3-39, respectively, are in consonance with the ones obtained for NG-LARGE.

TABLE 3-37: MAPPING RESULTS FOR THE AHBR IP ON NG-LARGE

Parameters	Total Resources	Resources utilization
Carry Cells	32256	82 (1%)
Registers	129024	607 (1%)
Block RAMs (48Kb)	192	0 (0%)
DSP Blocks	384	0 (0%)
LUTs	129024	622 (1%)
Maximum Frequency (CKCPU)(MHz)		91.84
Maximum Frequency (CKIO)(MHz)		79.91

TABLE 3-38: SYNTHESIS RESULTS FOR THE AHBR IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	608 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	576 (0%)
Maximum Frequency (CKCPU)(MHz)		235.8

Maximum Frequency (CKIO)(MHz)		213.0

TABLE 3-39: SYNTHESIS RESULTS FOR THE AHBR IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	81 (0%)
Sequential Cells	151824	608 (0%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	784 (1%)
Maximum Frequency (CKCPU)(MHz)		118.8
Maximum Frequency (CKIO)(MHz)		132.0

3.2.13 FTADDR_v0

FTADDR IP could not be mapped using its default configuration. This IP core contains a huge number of I/O ports, which makes it impossible to fit in the NG-LARGE FPGA. This makes sense, since all the pins will not be directly mapped to the FPGA (the controller is supposed to be connected to a physical interface). After trying to resynthesize the design using the simplest possible configuration (see Table 3-40), mapping was still impossible due to I/O limitations, so a different approach was taken to find a solution. Instead of using NG-LARGE board as a target device, an embedded variant (NG-LARGE-EMBEDDED) was chosen to remove the I/O ring and map HDL I/O signals directly to the I/O internal signals. Obtained mapping results after this are provided in Table 3-41.

TABLE 3-40: CONFIGURATION VALUES FOR MAPPING FTADDR

Parameter	Value	Description
ahbbits	32	Width of AHB read/write data buses
ddrbits	32	Width of DDR data bus
nports	1	Number of implemented AHB ports
nahbmst	1	Number of AHB masters on each bus
numcs	1	Number of chip select signals implemented
ctrldup	1	Number of parallel memory control signals instances
numrwen	1	Width of DFI enable and valid signals
numrdlvlphy	1	Width of DFI read levelling PHY signals
numrdlvlmc	1	Width of DFI read levelling MC signals
numwrlvlphy	1	Width of DFI write levelling PHY signals
numwrlvlmc	1	Width of DFI write levelling MC signals
rdblvlbits	1	Width of DFI read/write levelling delay
rdglvlbits	1	Width of DFI read levelling gate delay

rdgflvlbits	1	Width per byte lane of dfi_rdlvl_gate_fdelay signal
wrlvlbits	1	Width per byte lane of dfi_wrlvl_delay signal
phyimpl	0	PHY implementation ID
genphy_trden	0	Specifies trddata_en parameter for generic DFI implementation
genphy_twrlat	0	Specifies tphy_wrlat parameter for generic DFI implementation
genphy_twrdata	0	Specifies twrdata parameter for generic DFI implementation
dynrst	0	Enable reset values control from input signals
phyctrlbits	0	Number of bits implemented in generic PHY control register

TABLE 3-41: SYNTHESIS RESULTS FOR THE FTADDR IP ON NG-LARGE (I/O PORTS EXCLUDED)

Parameters	Total Resources	Resources utilization
Carry Cells	32256	196 (1%)
Registers	129024	967 (1%)
Block RAMs (48Kb)	192	0 (0%)
DSP Blocks	384	0 (0%)
LUTs	129024	1790 (2%)
Maximum Frequency (dfi_clk)(MHz)		47.75

3.2.14 Packet Telecommand Decoder with AMBA (PDEC3AMBA)

The PDEC3AMBA IP has not been successfully synthesized. Nxmap tool does not allow source files with *.pkg*, *.rtl*, *.bdy* and *.ent* extensions (only *.vhd*), so every file with one of these characteristics was converted to an VHDL file. However, when running synthesis following the compile order defined in the documentation, an internal error is returned. Apparently, Nxmap tool is not able to differentiate between *std_logic_vector* and *std_ulogic_vector*, which makes it unable to detect the body of several functions.

3.2.15 Packet Telecommand Decoder (PTCD)

The PTCD IP has not been successfully mapped on the BRAVE family. After launching the NX Python script, several conflicts appeared between the functions *read* and *write* declared in *std_logic_1164.vhdl* and two constants with the same name (*READ* and *WRITE*) declared in *c161setenv.vhd*. Aiming to solve this issue, both constants were renamed as *READ_CONST* and *WRITE_CONST* and propagated to each module in the design that required them. However, after doing this, an internal error occurred during the mapping, returning the message *Fatal: Unexpected error*. These issues are not related to the mapping process itself but the design instead (out of our scope).

Despite of this, preliminary resources utilization results were obtained during synthesis successfully. A summary of these results can be found in Table 3-42. In addition, results for XQRKU060 and RTG4, shown in Table 3-43 and Table 3-44, respectively, were obtained in Synplify, which does not report any issue during the synthesis process.

TABLE 3-42: SYNTHESIS RESULTS FOR THE PTCD IP ON NG-LARGE

Parameters	Total Resources	Resources utilization
Carry Cells	32256	0 (0%)
Registers	129024	3055 (1%)
Block RAMs (48Kb)	192	160 (84%)
DSP Blocks	384	0 (0%)
LUTs	129024	13024 (11%)

TABLE 3-43: SYNTHESIS RESULTS FOR THE PTCD IP ON XQRKU060

Parameters	Total Resources	Resources utilization
Registers	663360	1052 (0%)
Block RAMs (36Kb)	1080	0 (0%)
DSP Blocks	2760	0 (0%)
LUTs	331680	1876 (1%)
Maximum Frequency (MHz)		147.6

TABLE 3-44: SYNTHESIS RESULTS FOR THE PTCD IP ON RTG4 150

Parameters	Total Resources	Resources utilization
Carry Cells	151824	210 (0%)
Sequential Cells	151824	917 (1%)
Block RAMs (64x18)	209	0 (0%)
DSP Blocks	462	0 (0%)
LUTs	151824	2809 (2%)
Maximum Frequency (MHz)		71.2

4 CONCLUSIONS

In this report, mapping and implementation results on BRAVE FPGAs have been provided for the ESA IP Cores currently integrated in the Abeto framework and listed in [AD-2]. The particularities of each IP have been taken into account, in order to define an alternative configuration if the baseline one does not fit well with the current NanoXplore devices. For each one of those IP cores, Table 4-45 shows the synthesis steps which have been successfully completed, as well as the NanoXMap version used.

TABLE 4-45: SUMMARY OF MAPPING-TO-BRAVE PROGRESS FOR ESA IP CORES

IP core	NXMap version	Compile	Synthesis	Place	Route
dummyIP	3.9.0.5	Yes	Yes	Yes	Yes
EDAC IP	3.9.0.5	Yes	Yes	Yes	Yes
HurriCANe	3.9.0.5	Yes	Yes	Yes	Yes
SpaceWire codec (spwb2-3)	3.9.0.5	Yes	Yes	Yes	Yes
SpaceWire codec (spw v12)	3.9.0.5	Yes	Yes	Yes	Yes
SpaceFibre codec	3.9.0.5	Yes	Yes	Yes	Yes
SHyLoC IP	3.9.0.5	Yes	Yes	Yes	Yes
PTME	3.9.0.5	Yes	Yes	No	No
LEON2FT	3.9.0.5	Yes	Yes	Yes	Yes
NoC IP	3.9.0.5	Yes	Yes	No	No
SpaceWire Node	3.9.0.5	No	No	No	No
AHBR	3.9.0.5	Yes	Yes	Yes	Yes
FTADDR	3.9.0.5	Yes	Yes	No	No
PDEC3AMBA	3.9.0.5	No	No	No	No
PTCD	3.9.0.5	Yes	Yes	No	No

In addition, synthesis results have been obtained for Xilinx Kintex UltraScale XQRKU060 and Microsemi RTG4 150 by using Synopsys Synplify Premier P-2019.09-SP1, providing in this way some numbers to guide future users about the feasibility of using the IP cores offered by ESA for their developments.

The obtained results have been compared with the synthesis reports for other FPGA technologies provided by each IP developer, if available. In this way, it has been possible to verify the correctness of the acquired results in terms of resources utilization and maximum clock frequency, keeping in mind the differences among FPGA technologies.

As it has been reflected, results for PTME were not obtained (only a preliminary estimation at the end of the synthesis stage) for the BRAVE family, since an error message related to the number of I/O pads consumed by the IP was reported by the tool. This issue was analysed in detail, in order to obtain results for a simpler configuration, obtaining the same error by the tool. PTCD could not be mapped either, and the same process of simplification was carried out unsuccessfully. In the case of PDEC3AMBA and SpWNode IPs, synthesis could not be performed correctly, due to problems with the synthesis tool or the design sources.