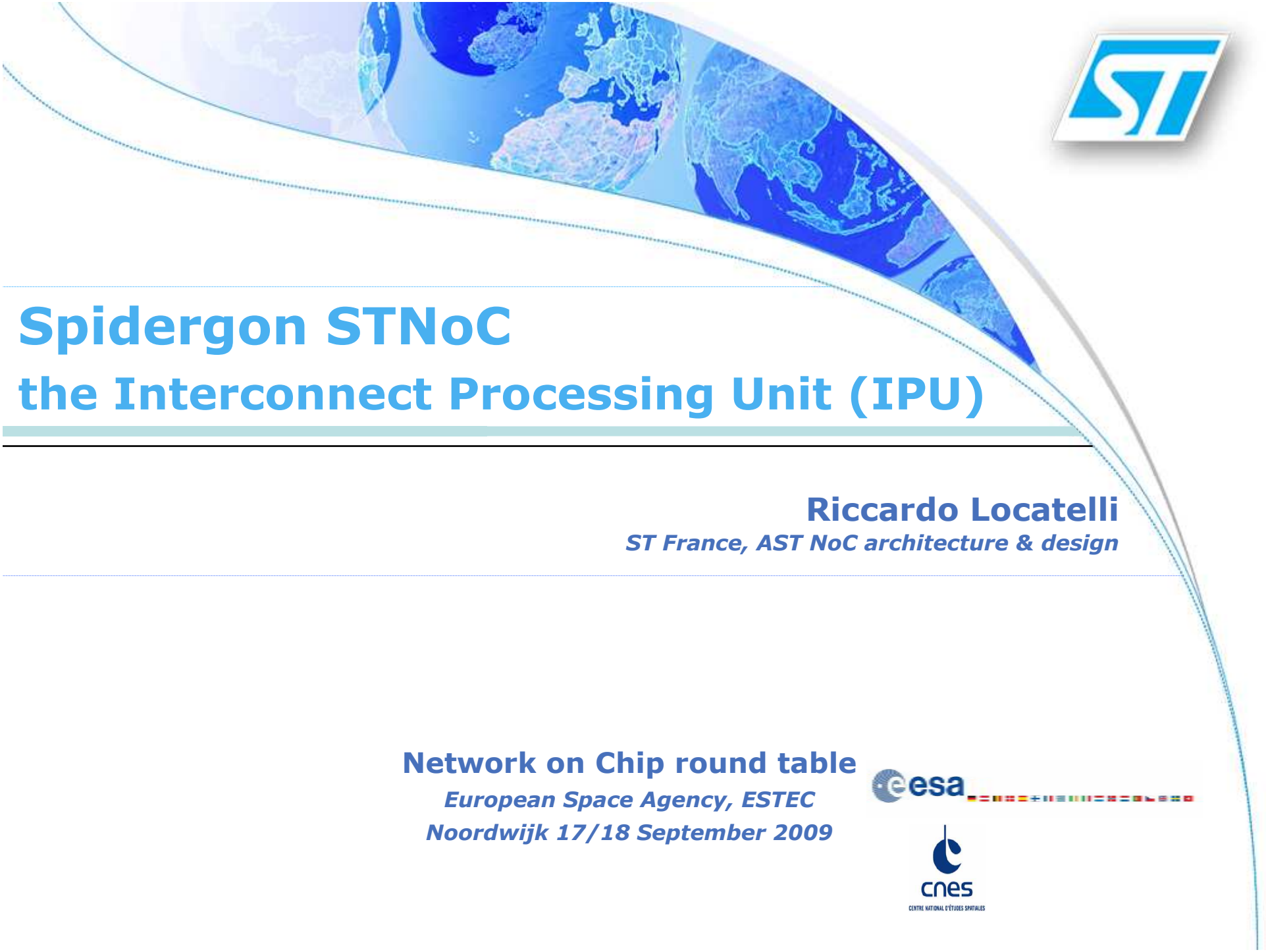

Spidergon STNoC
the Interconnect Processing Unit (IPU)

Riccardo Locatelli
ST France, AST NoC architecture & design

Network on Chip round table
European Space Agency, ESTEC
Noordwijk 17/18 September 2009

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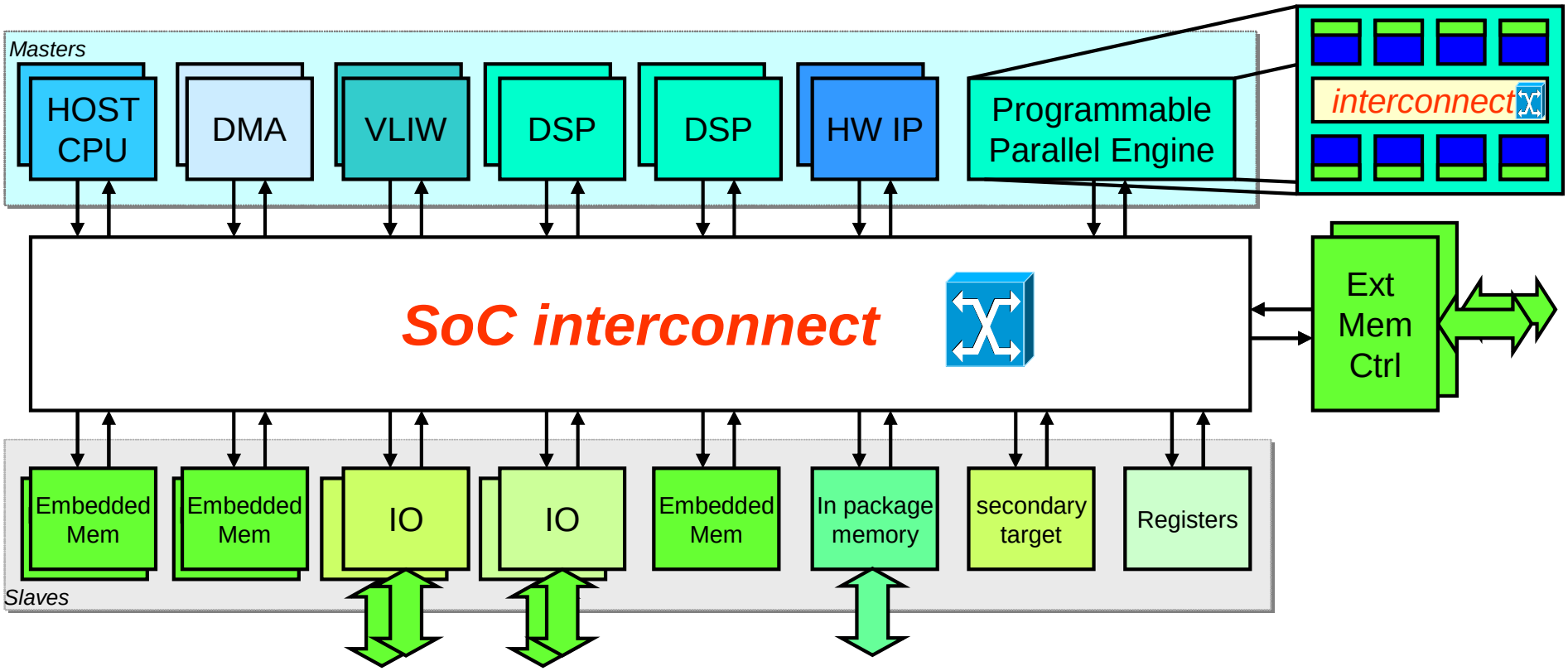
Agenda

- SoC interconnect requirements vision
- Beyond NoC, IPU
- Spidergon STNoC fundamentals:
  - Topology, Routing, Flow control
  - Packet format, Services
- Spidergon STNoC IPU EDA
- Demonstrators

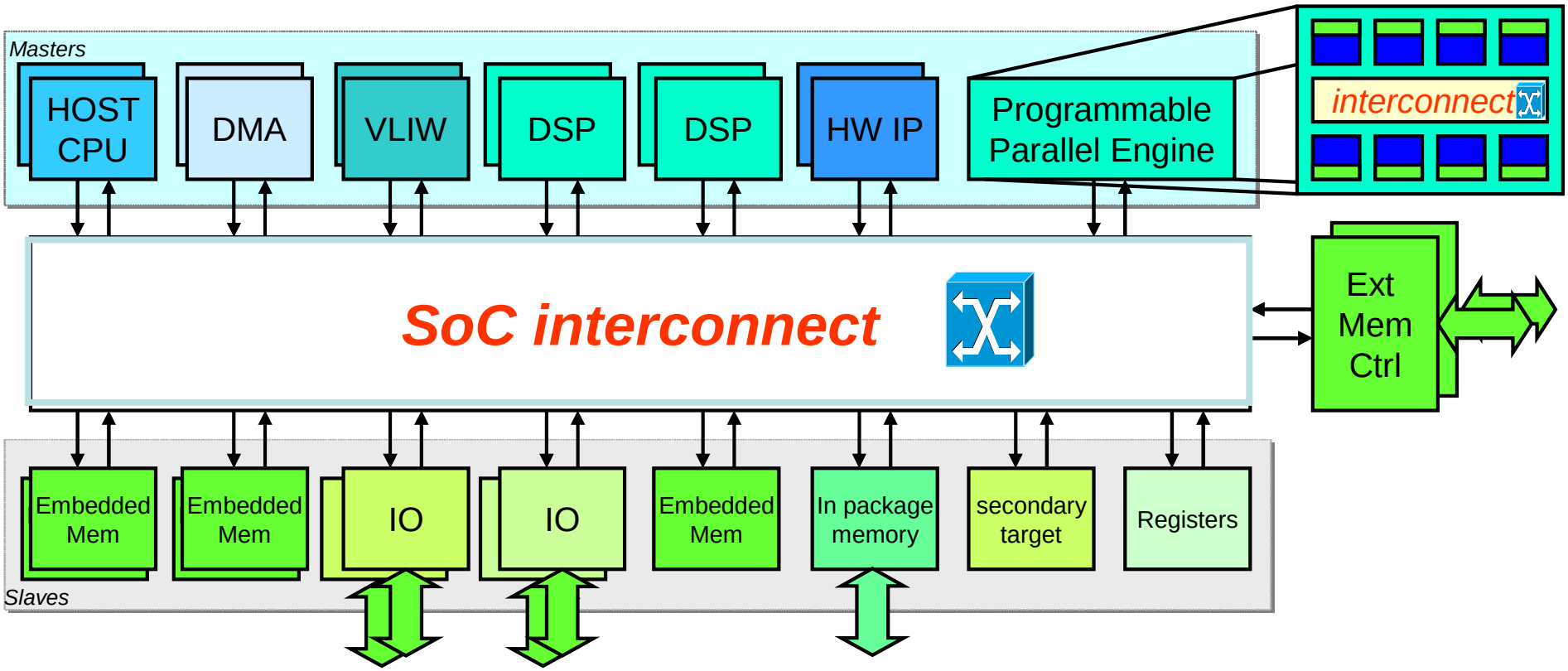
Multicore SoC architecture vision



towards....

Open Configurable Heterogeneous Multicore Platforms

Multicore SoC architecture vision



ON-CHIP COMMUNICATION CENTRIC PLATFORM

On-chip communication centric platform: our vision

- **Physical-aware interconnect in 45, 32 nm**
  - higher distribution, deeper hierarchy, regularity
  - redundancy & fault tolerance
- **Performance scalability on top of a distrib… infrastructure**
  - Higher aggregate band… management
  - Su… …gramming
- **S… …the hardware platform through S… …s Set**
  - Expose system hardware to system software
- **Integration platform**
  - Reuse, EDA, productivity (from architecture to backend)

Shift towards programmable on-chip communication platform built on top of a simple network

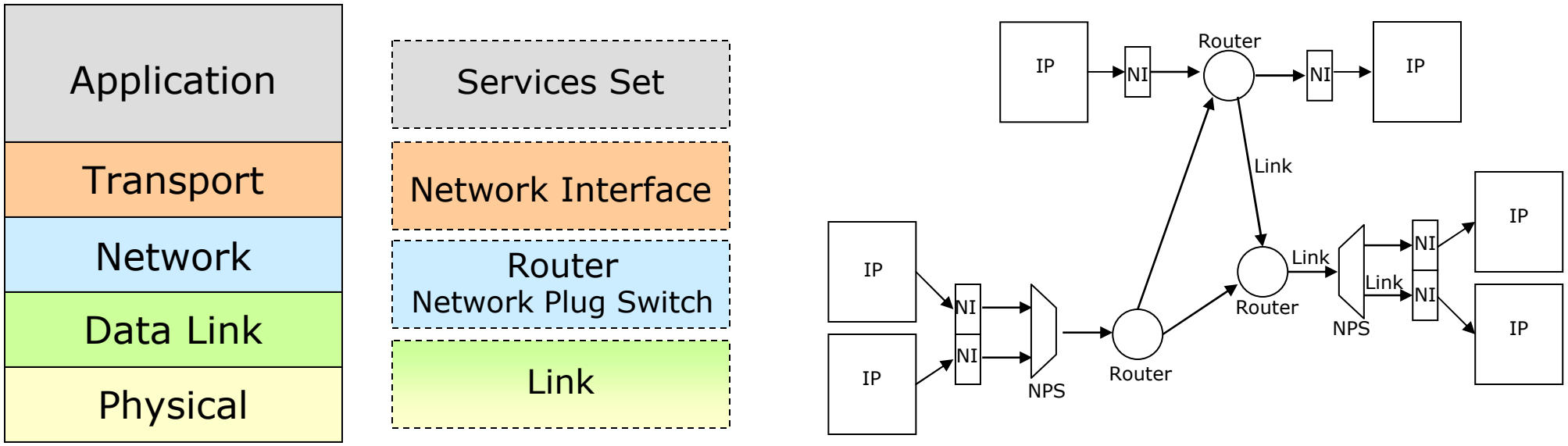
Beyond the NoC: the IPU

The **Interconnect Processing Unit (IPU)** is an on-chip communication network with **hardware** and **software** components

- which implement key functions of different SoC programming models through a set of communication and synchronization primitives
- and provide low-level platform services to enable advanced features in modern heterogeneous applications on a single die.

Spidergon STNoC IPU

Spidergon STNoC is a hardware/software set of Services on top of a distributed on-chip network

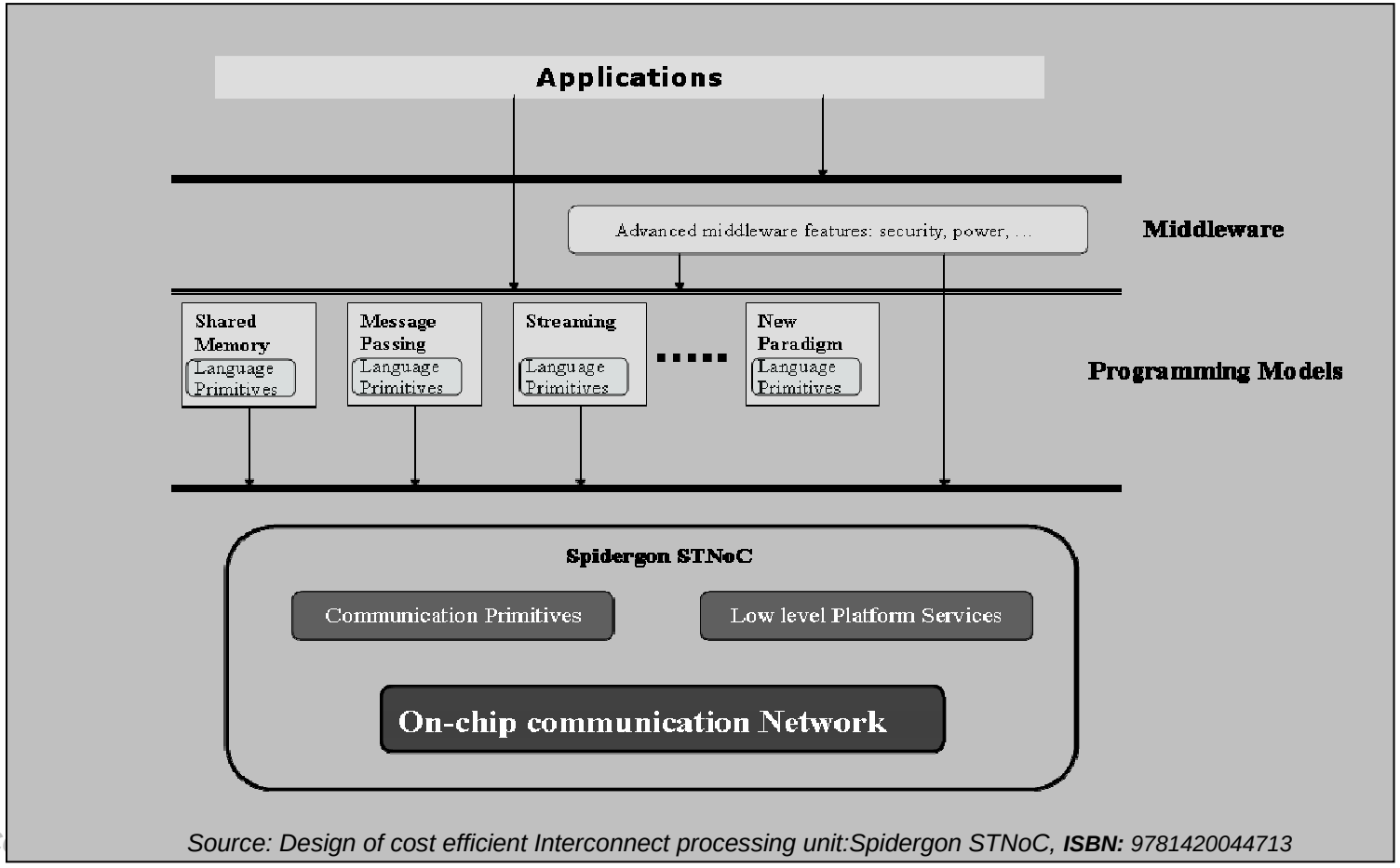


Main hardware building blocks are:

Link, Router, Network Plug Switch, Network Interface

Spidergon STNoC IPU

- IPU Services are implemented in hardware and/or software
  - Communication Primitives
  - Low level Platform Services



Source: Design of cost efficient Interconnect processing unit:Spidergon STNoC, ***ISBN:*** *9781420044713*

Spidergon STNoC IPU fundamentals

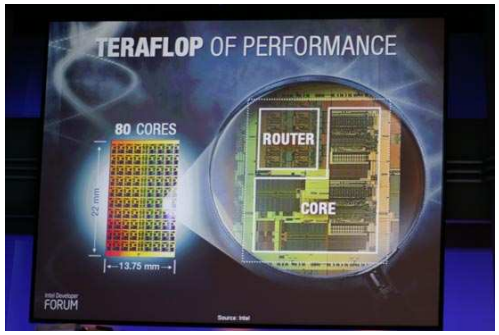
Topology & routing

Flow control

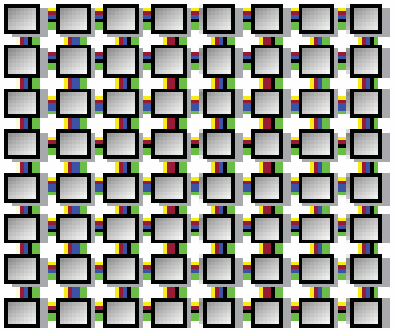
Packet format

Topology trade-off

Challenge is trade-off network benefits of regular topology vs. heterogeneous, irregular Multicore SoC architectures

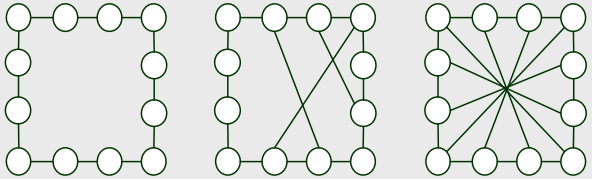


from INTEL

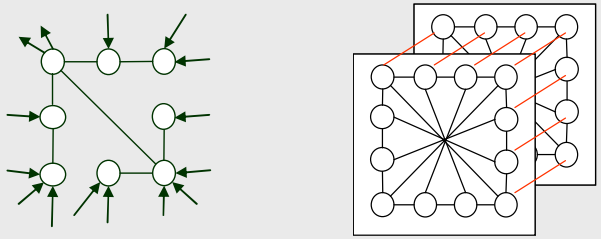


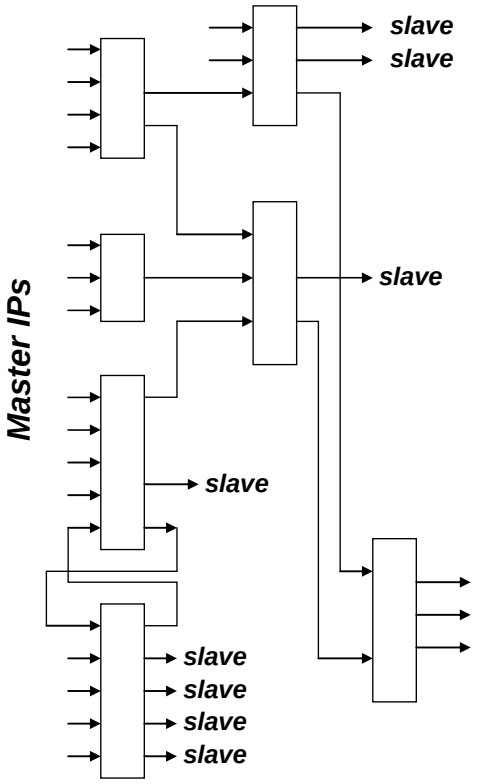
from TILERA

Spidergon STNoC family of topologies



Spidergon STNoC hierarchy & aggregation

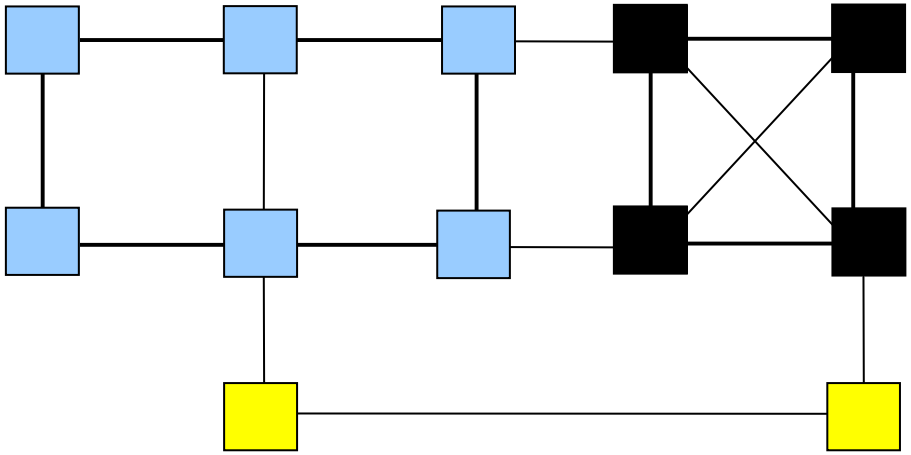




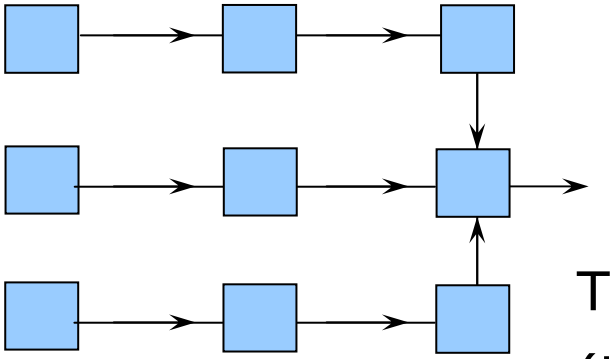
SoC interconnect example

Spidergon STNoC topologies

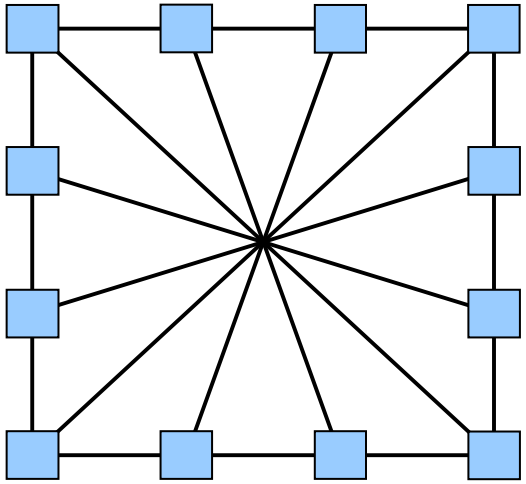
Match application-specific topological requirements of SoCs



Hierarchical interconnect



Tree-like
(to DDR)



Symmetric Spidergon
(point2point in streaming)

Spidergon STNoC routing centric approach

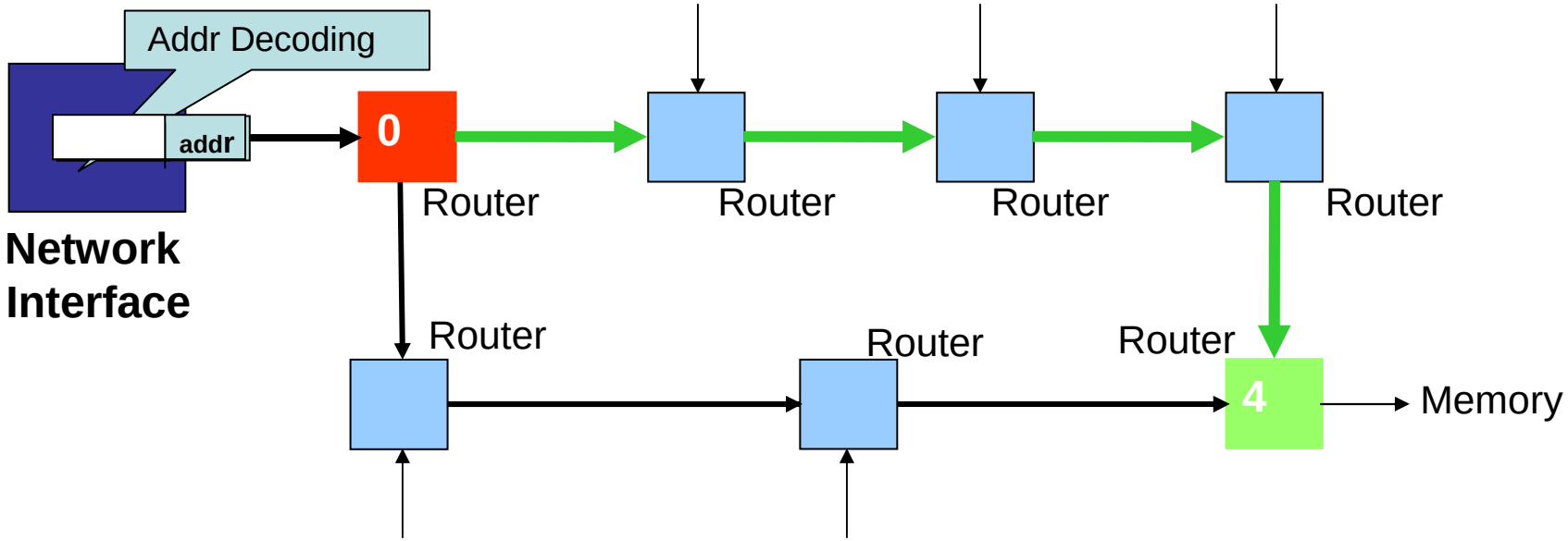
- Spidergon STNoC is based on routing
- No address decoding at each Node, but just once at the injection

Why Routing ?

- To decouple address map / IP socket from the network
  - Fast, simple and protocol agnostic router
  - Post-silicon software re-programmability

Spidergon STNoC routing

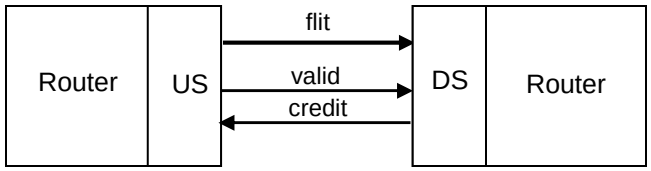
- Several deterministic deadlock free routing schemes
- Two-steps implementation:
  - (i) @ packet generation (programmable)
  - (ii) on the path (zero tables – very simple)

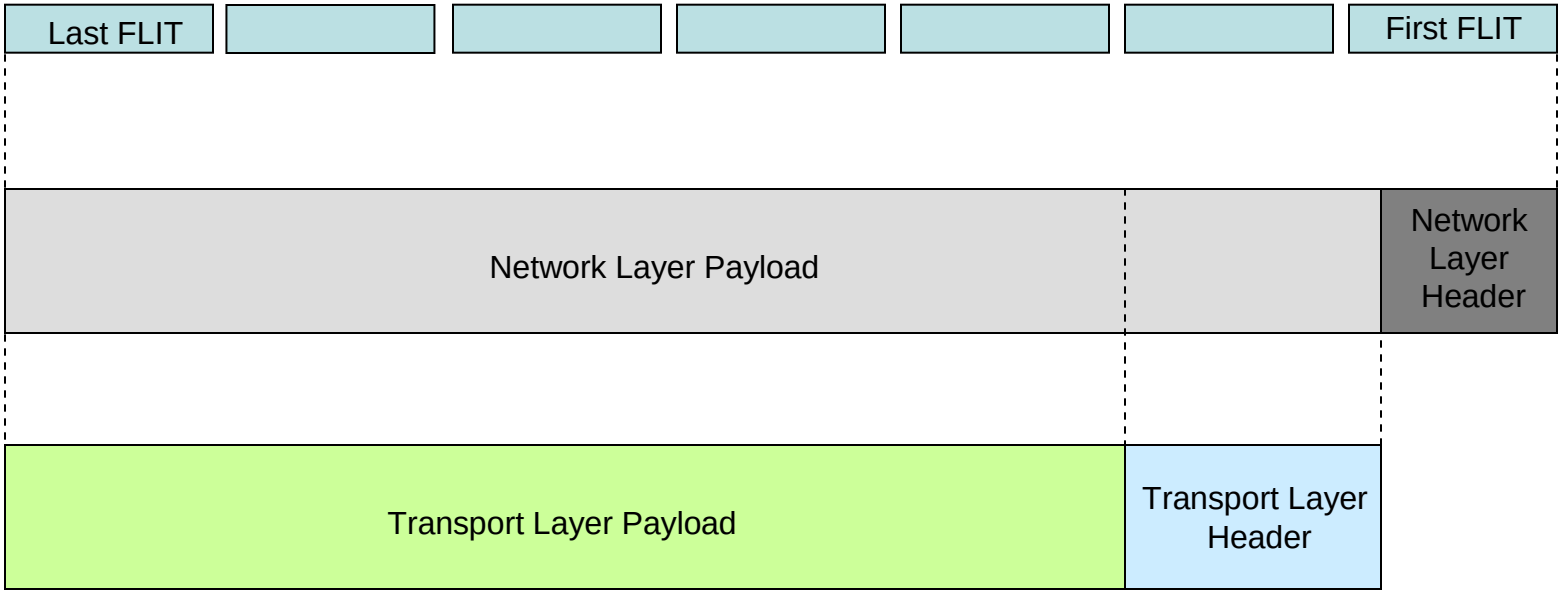


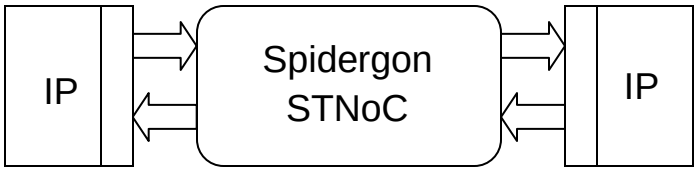
Spidergon STNoC flow control

- Forwarding scheme is wormhole
  - Latency gain and smaller flit level buffers
- Link level flow control is based on credits
  - Most efficient to support virtual channels
- End2end flow control based on virtual connection mechanism
  - Buffer efficient in streaming/message passing

Spidergon STNoC layers







WIRES

FLIT

PACKET

IP Transactions

Spidergon STNoC IPU fundamentals

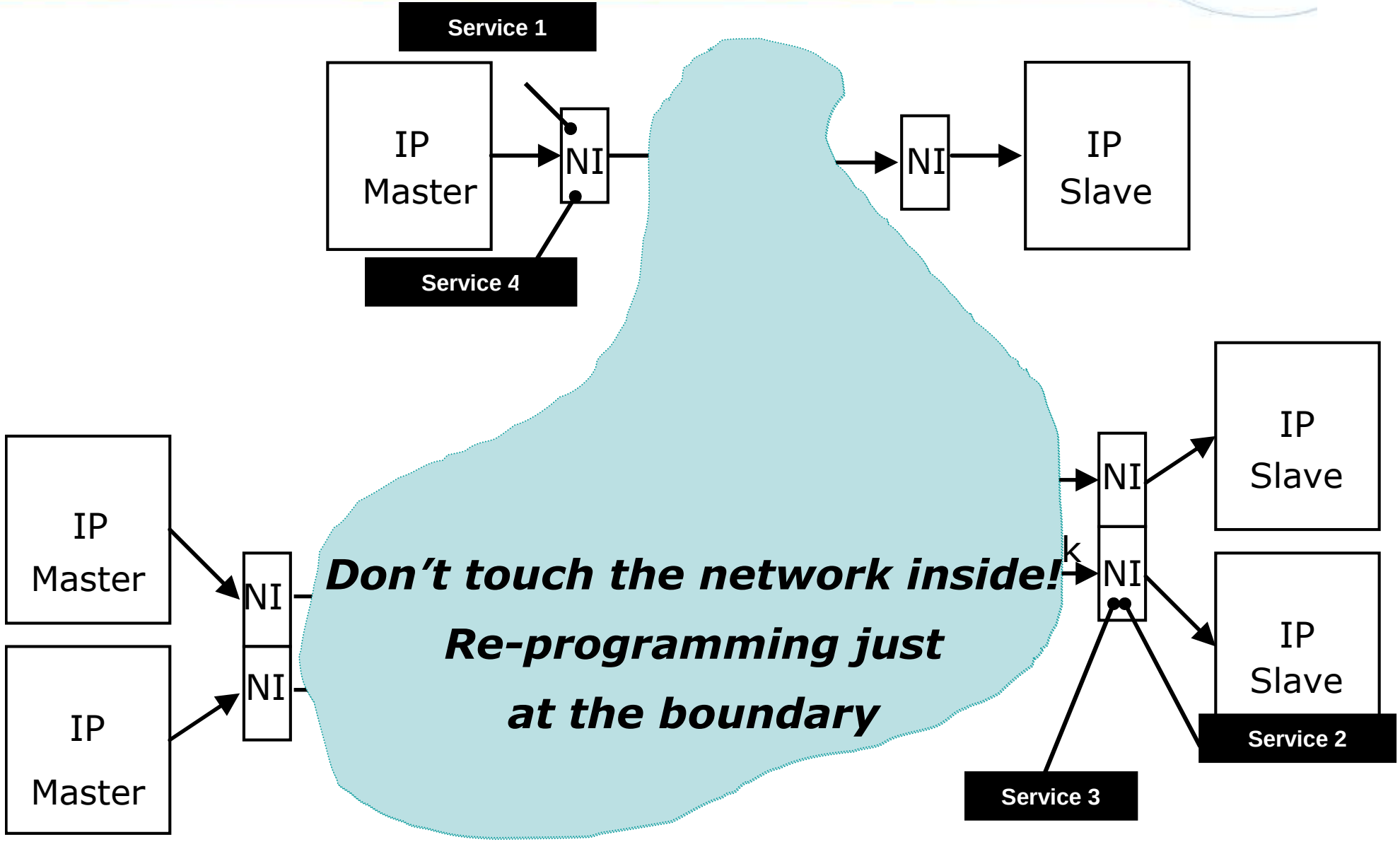
Services

Spidergon STNoC platform services

Spidergon STNoC acts as a programmable distributed hardware/software component that offers a set of services to design advanced application features

- Topology virtualization, QoS, Power management, Security support, Diagnostic and monitoring, …..

Spidergon STNoC platform services: SW view



Spidergon STNoC SW stack

- Export a SW view (API) of the HW interconnect behavior to program the multi-core SoC architecture
- Libraries developed to ease programming and to take advantage of built-in NoC services
- OS network awareness
- A stack portable to different OS (but the API stays put)

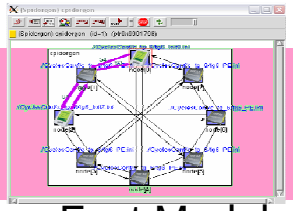
HW SoC can react to different application conditions to improve product user experience

Spidergon STNoC IPU EDA

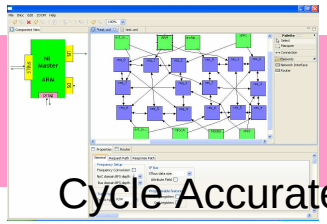
Spidergon STNoC EDA

I-NoC is an integrated interactive EDA framework for Network-on-Chip based platforms from conception to implementation

SoC requirements



Fast Models



Cycle Accurate Models

Architectural exploration

Implementation

Analysis results

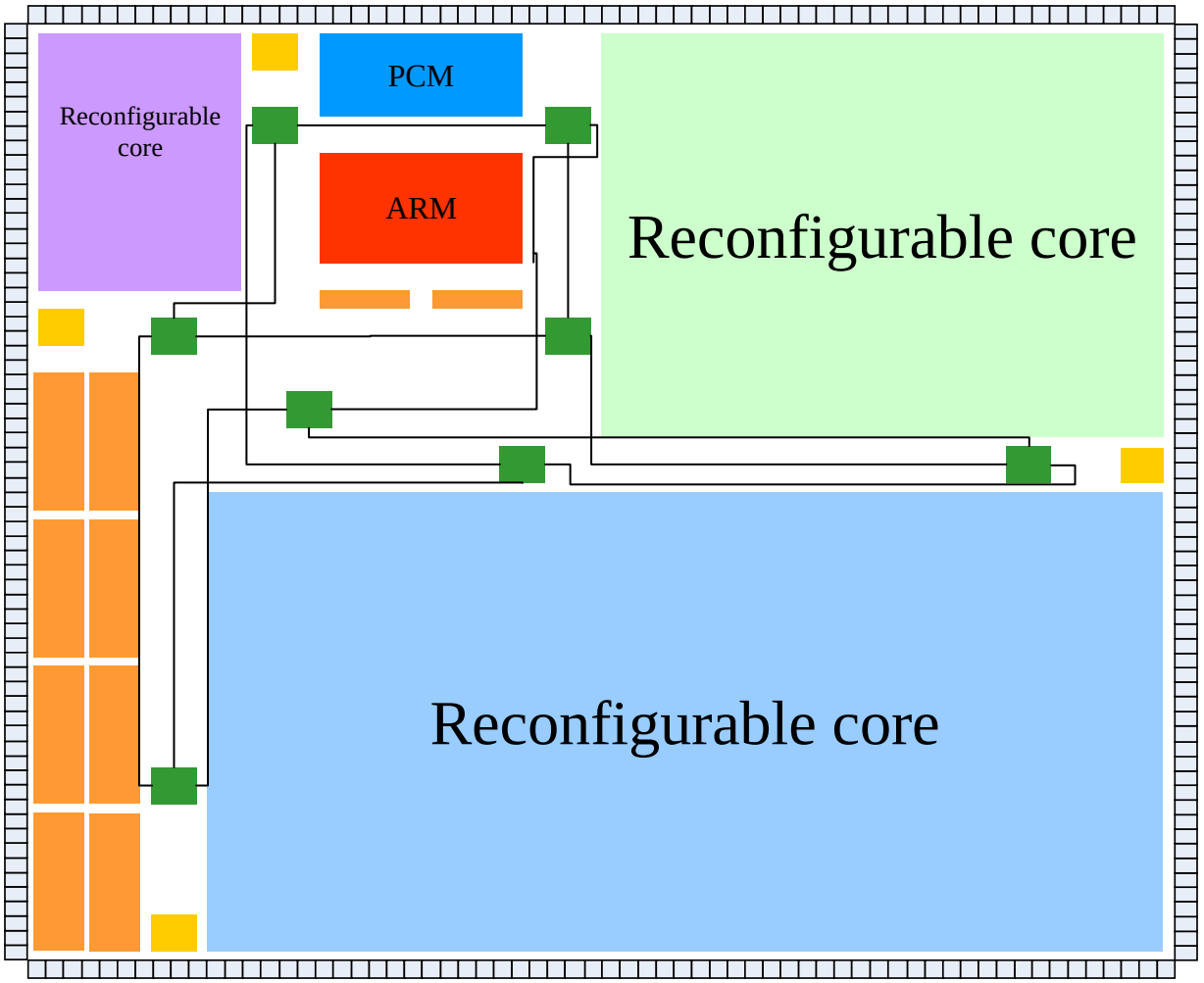
Documentation

RTL

SW device drivers

Spidergon STNoC Demonstrators: examples

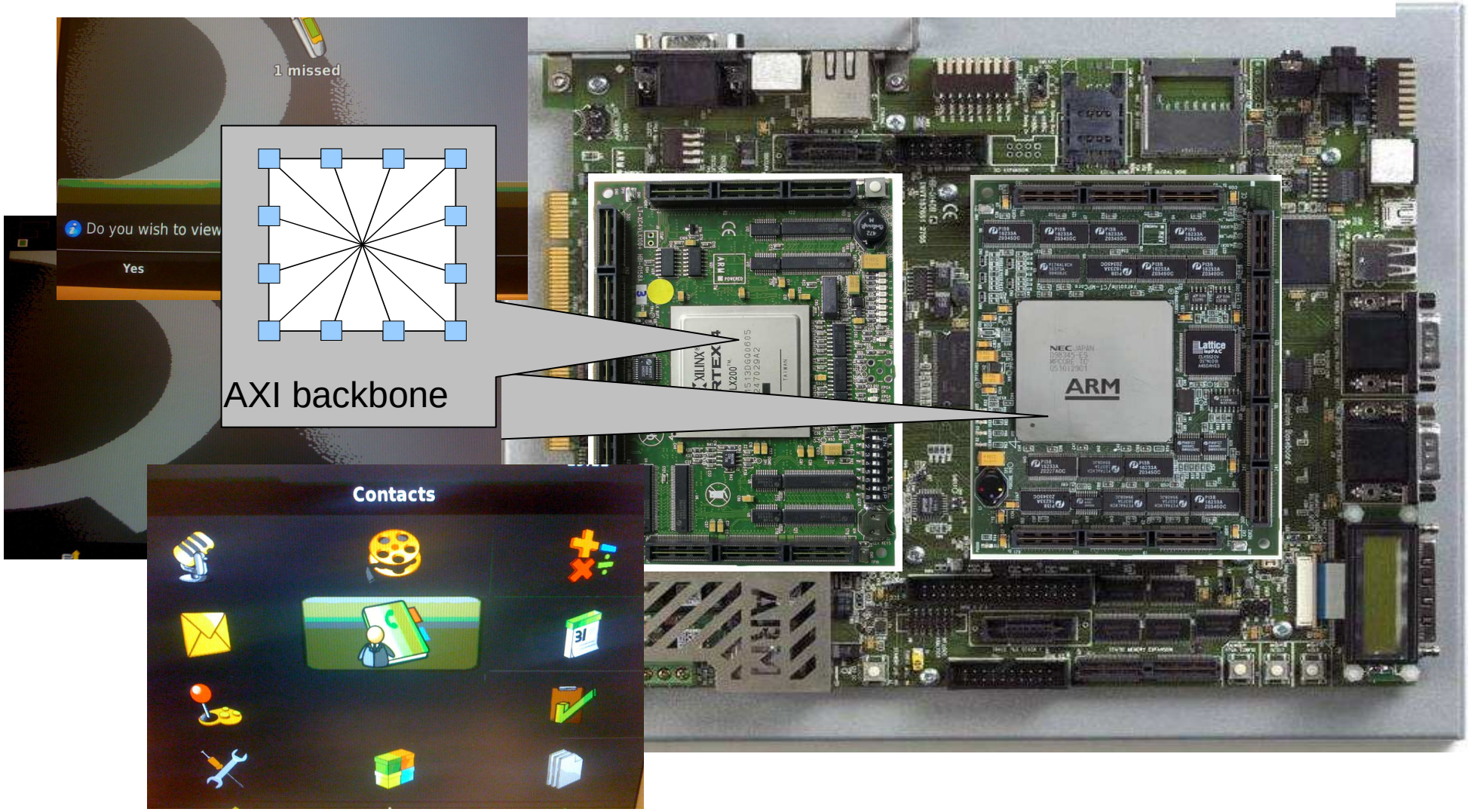
Configurable Multicore test-chip: samples out



Multicore based on reconfigurable logic and Spidergon STNoC IPU

Spidergon STNoC IPU with ARM11 SMP

Emulate an application processor



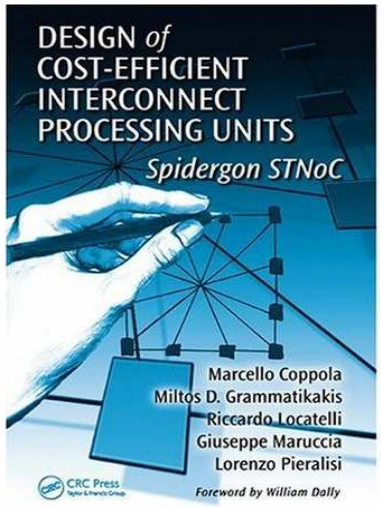
Cambridge ARM Partners Meeting, Aug. 08

Conclusions

beyond NoC…. the IPU

Spidergon STNoC IPU is an innovative technology for next generation Multicore SoCs

- For more info please refer to
  - Spidergon STNOC book
  - **ISBN:** 9781420044713
  - **Publication Date:** September 2008



thanks

riccardo.locatelli@st.com