ESTEC

SCOC3 NoC Round Table

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All the space you need

EADS astrium

Agenda

- **SCOC1 to SCOC3**
- **SCOC3 architecture brief presentation**
- **Interesting NoC points**
- **NoC expectations**

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SCOC3 general requirements

- **SCOC3 shall be able to handle Real Time Software and manage time constraint interfaces (1553, Telecommand,…)**
- **SCOC3 shall have multi purpose uses and so there will be several modes and modules.**
- **SCOC3 shall integrate functions which were on several ASICs before and shall be competitive: improvement in size, weight and power consumption**

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SCOC3 heritage

- **EADS Astrium has been working on SoC for the last ten years:**
  - SCOC3 has an heritage based on SCOC1 which was a study made with ESA funding.
  - SCOC3 benefits also of SCOC2 which was a study made internally to continue the previous one.

- **These studies show several key points like internal bus arbitration, I/O interfaces traffic and memory bandwidth.**

- **SCOC3 solves some of these issues taking into account real needs and putting margin on top of them.**

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SCOC3 space environment

- **3 main causes:**
  - Solar wind, Solar flare and Galactic cosmic rays
- **3 main effects:**
  - TID: Total Ionizing Dose
  - SEL: Single Event Latchup
  - SET/SEU-MBU/SEFI
    - SET : Single Event Transient
    - SEU : Single Event Upset
    - MBU : Multiple Bit Upset
    - SEFI : Single Event Functional Interrupt
- **2 protection modes:**
  - By hardening the technology
  - By hardening the design

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SCOC3 internal busses

- **Several scenarios were studied around arbitration and internal AHB busses.**
- **These studies lead to the choice of using two internal AHB busses allowing LEON3FT to have its own access to memory.**
- **A second bus is dedicated to peripherals.**

COMPUTATION OF PERFORMANCES ON CPU & IO AHB BUS

Global Hypothesis	
Maximum allowed bus load	90%
CPU Bus Frequency	32 MHz
IO Bus Frequency	32 MHz

Slaves Hypotheses	
Memory controller	
CPU/IO clock ratio	1
IO AHB Bus Grant Wait states	5
CPUCTRL AHB WS on first read access	4
CPUCTRL AHB WS on next read access	1
CPUCTRL AHB WS on first write access	4
CPUCTRL AHB WS on next write access	1
IOCTRL AHB WS on first read access	4
IOCTRL AHB WS on next read access	1
IOCTRL AHB WS on first write access	4
IOCTRL AHB WS on next write access	1

Enter the hypothesis on the table (except the marked cells) and then press the button to ajust the slack to 0. The sheet will then compute the CPU usage ratio in order not to exceed the maximum allowed bus load

Ajust slack to 0

CPU bus Masters Hypothesis	
Processor	
CPU usage ratio	**87,5%**
Instruction cache hit ratio	80%
Data cache hit ratio	80%
Load instruction ratio	10%
Store instruction ratio	5%
Instruction cache fill burst length	8
HDMA	
From CPU to IO	0,5 Mbits/s
From IO to CPU	0,5 Mbits/s
Direct access	
Percentage in Load to IO	20%
Percentage in Store to IO	20%

IO Masters Hypothesis	
Spacewire (7)	
Overall Spacewire TX bit rate	45 Mbits/s
Overall Spacewire RX bit rate	45 Mbits/s
CAN/1553	
Number of IPs active	3
TM	
TM rate	1 Mbits/s
TM data size for VCM access	8

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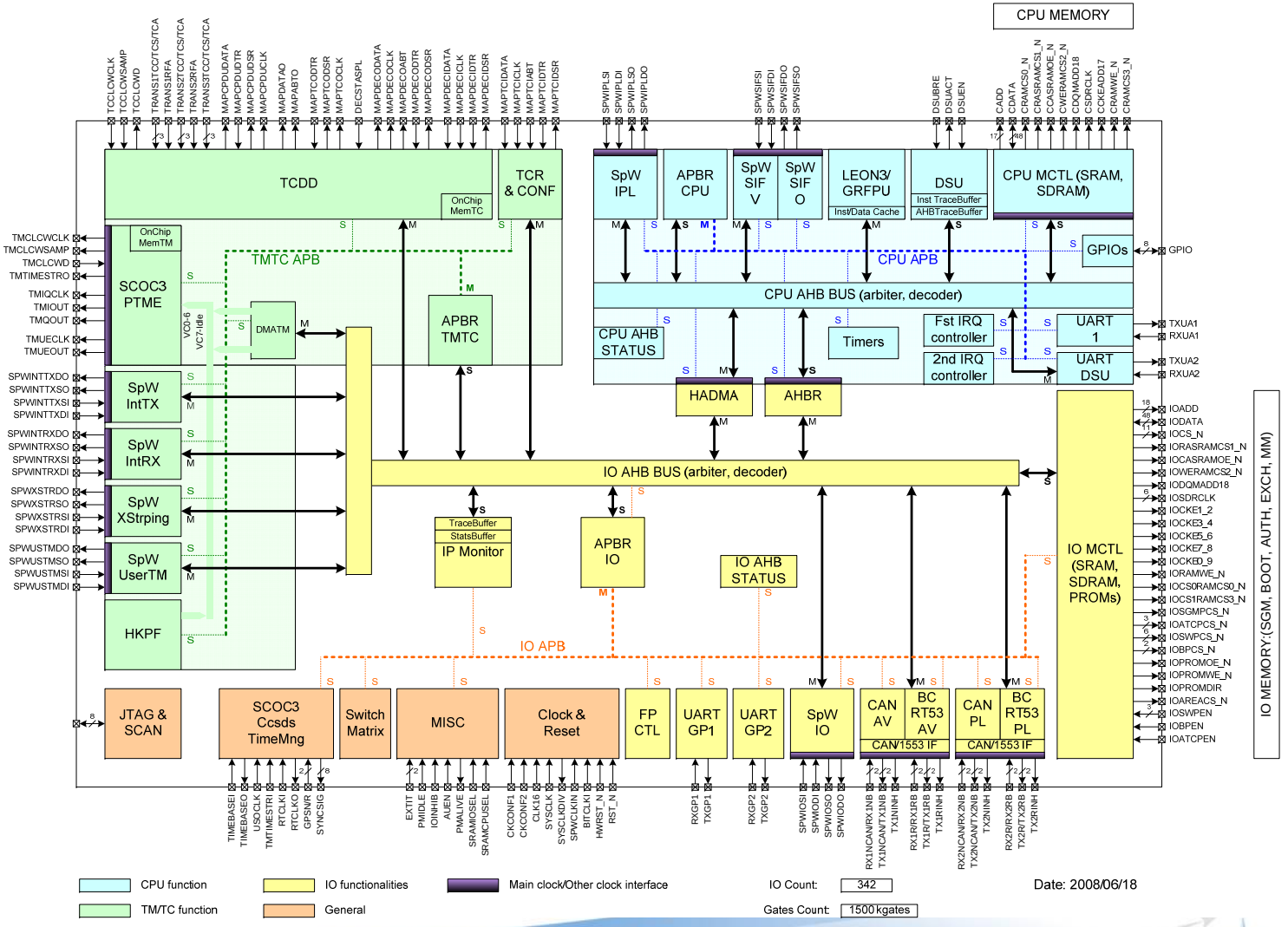
SCOC3 resulting architecture



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Why NoC might be promising?

- **The previous methodology is difficult to master from the beginning because the SCOC3 architecture depends on various standard and worst case applications traffic scenarii. It also depends on available components for space (mainly memories)**
- **As application definition is complex, future SCOC will have to take resources margins by duplication or triplication which leads to a complexity of architecture (local memory, shared memory, local computing) and communication between IPs (safety protocole, real time protocol, multiple access, …)**
- **Complex SoC requests dependability leading to improve specific protections and deterministic protocols within the SoC to guarantee the integrity of data/command transfers**
- **Deep submicron technologies leads to more data protection and potentially to add redundancies to maintain the availability of the global SoC function.**

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Future needs: design and tools

- **Needs:**
  - More autonomous functions
  - Increased instantaneous performance
  - Increased IO requested bandwidth
  - Increased dependability

- **This will request design architecture tool and simulation/validation tool for deeper pre-studies analysis**

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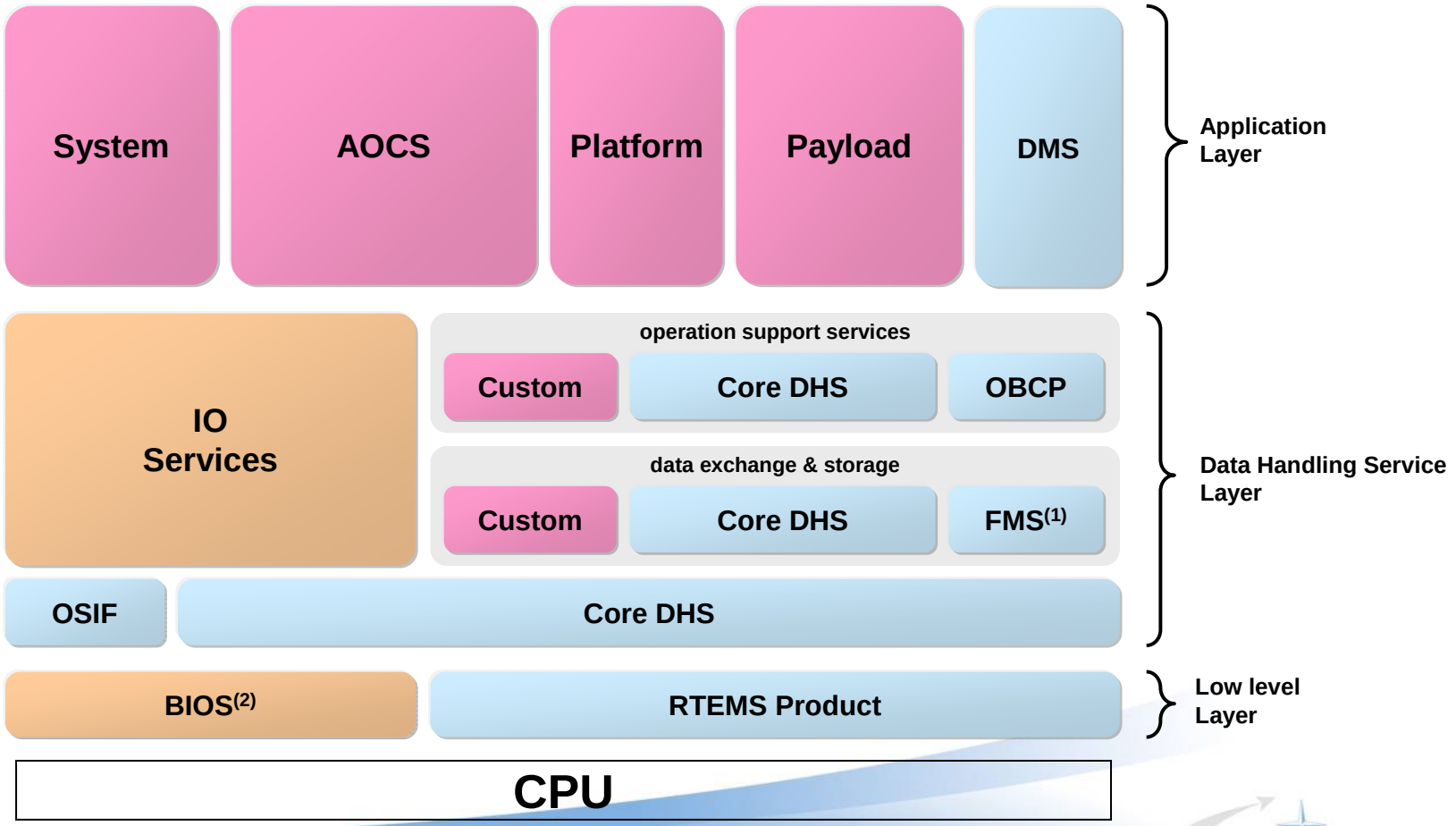
Data Processing (HW&SW) Architecture Status (1)

- **Today: Single Core Leon/multi-master AHB (SCOC3)**



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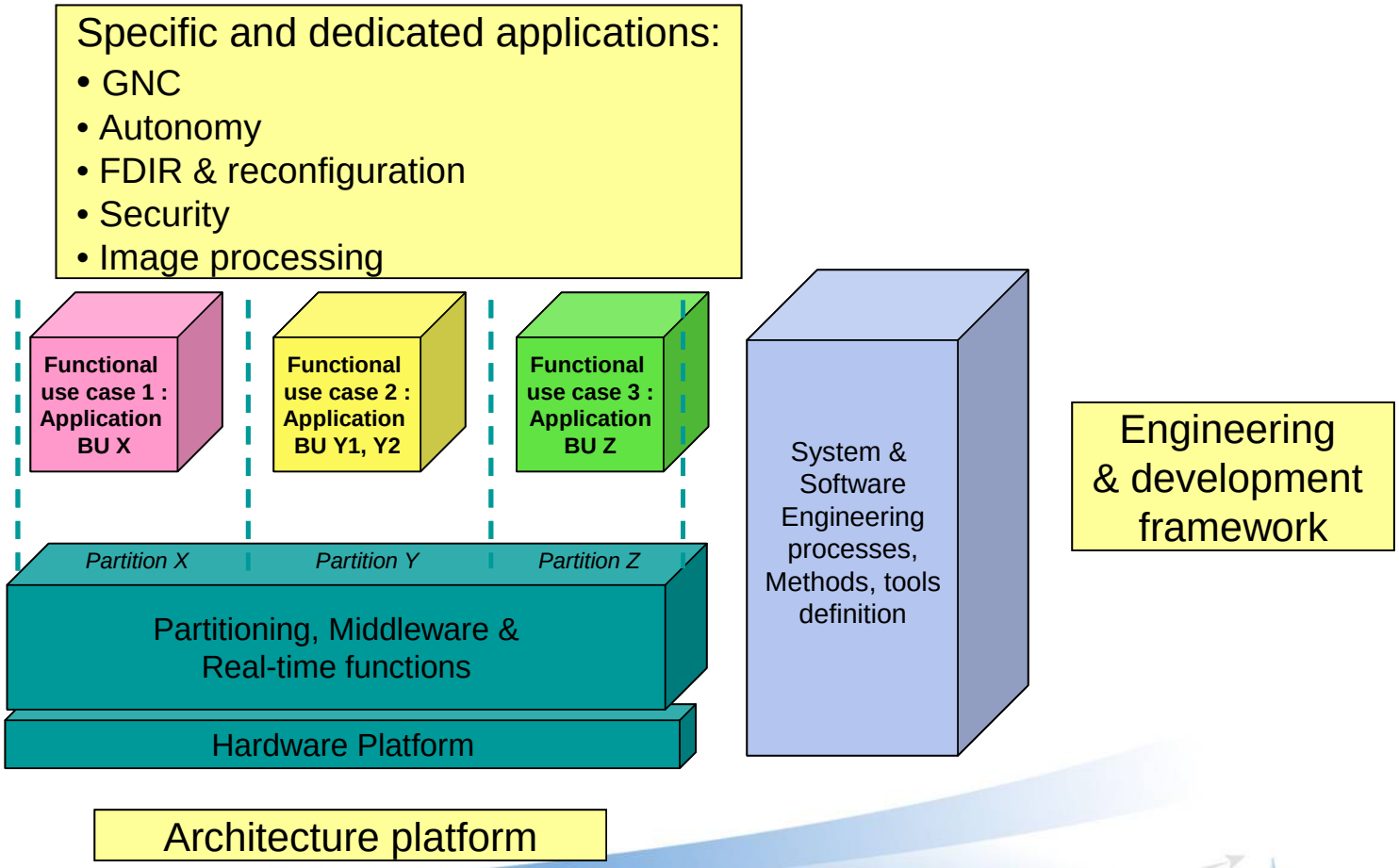
Data Processing (HW&SW) Architecture Status (2)

- **Time & Space Partitioning (Xtratum on LEON2 and SCOC3)**



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Data Processing (HW&SW) Architecture Status (3)

- **Prepare the migration to multi-core architectures**
- **Master the applications partitioning/deployment on them**

HOW:

- **On-going Studies:**
  - Component Base SW Engineering
    - ESA COrDeT “Component Oriented Development Techniques”
      - Derived from Automotive SOFA2 (->SOFA-HI)
  - Multi Core with Bus Interconnect Architecture
    - ESA Study “Next Generation Multi-Purpose Processor”
    - ESA Study “European DSP Trade-Off” including multi-core DIOPSIS one.
    - ESA ITT “HW-SW SystemC SoC co simulation platform” including MPSoCs
    - ESA ITT “System Impact Of Distributed Multicore Systems” including Virtual Machine Monitor
  - SoCKET “SoC Toolkit for Critical Embedded sysTems”

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NoC expectations

- **SoC complexity versus application requirements including margins, failure management / resources allocation (FDIR and Reconfiguration), I/O traffic, multi-core implementation,…**
- **Dependability**
- **NoC Technological Development Monitoring:**
  - Usage?:
    - Pure processing (programmable HW engine)
    - Payload Controller
    - Spacecraft Controller
  - Development Framework maturity:
    - Methods & tools for application partitioning/deployment/dynamic control
    - Application profiling/debugging

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